UNITRODE

High Speed PWM Controller

UCC1829-1/-2
UCC2829-1/-2
UCC3829-1/-2

PRELIMINARY

FEATURES

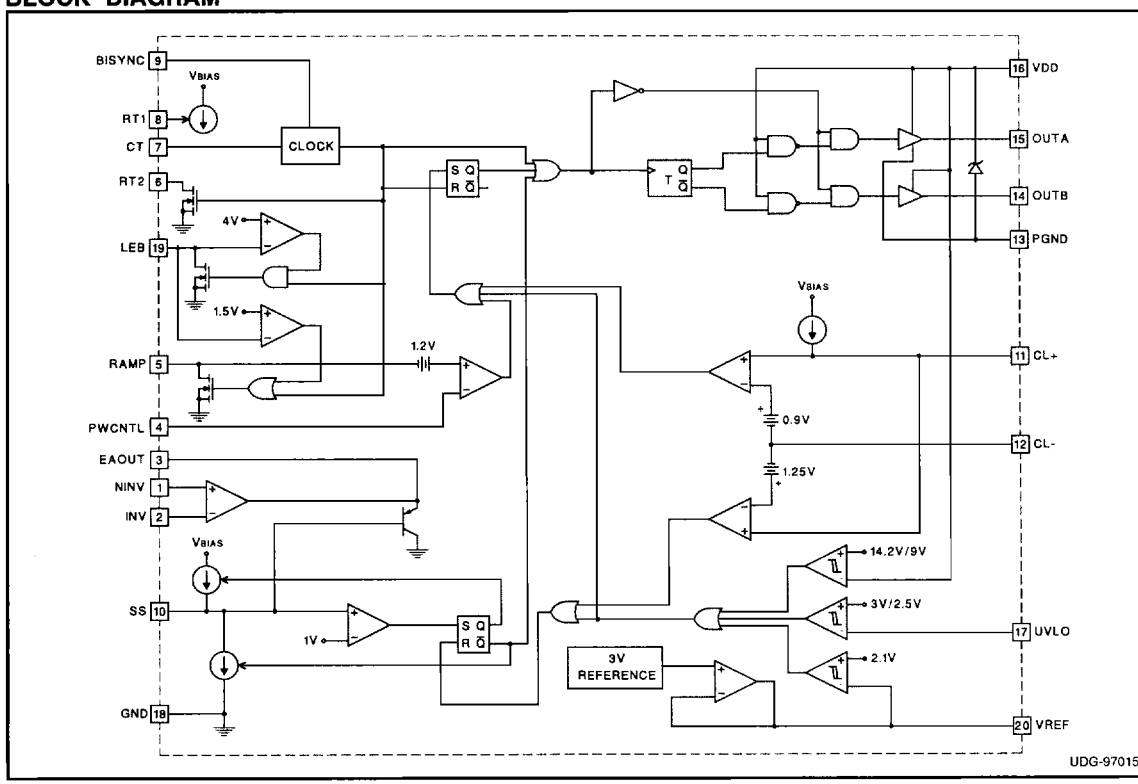
- Compatible with Voltage or Current Mode Topologies
- Practical Operation at Switching Frequencies to 4MHz
- 50ns Propagation Delay to Output
- High Current Complementary Outputs
- Programmable Dead Time and Frequency Oscillator
- Pulse by Pulse Current Limiting
- Latched Overcurrent Comparator with Full Cycle Restart
- Programmable Undervoltage Lockout (UVLO)
- Adjustable Blanking for leading Edge Noise Tolerance

DESCRIPTION

The UCC3829 is a BiCMOS High Speed PWM Controller IC. It is optimized for high frequency switched mode power supply applications. The IC can be used in both voltage mode and current mode control applications. Care was given to minimizing the propagation delays through the comparators and logic circuitry while maximizing the bandwidth and slew rate of the error amplifier. The oscillator frequency and deadtime can be programmed via two external resistors and a capacitor. The undervoltage lockout threshold can be programmed using an external resistor divider. The current limit and overcurrent threshold can be set externally. The chip is available in either single ended or push-pull output configuration.

Fault protection circuitry includes undervoltage detection for the internal bias supply, and overcurrent detection. The fault detection logic sets a latch that ensures full discharge of the soft start capacitor before allowing a restart. While the fault latch is set, the outputs are in a low state. In the event of continuous faults, the soft start capacitor is fully charged before discharging to insure that the fault frequency does not exceed the designed soft start period.

BLOCK DIAGRAM



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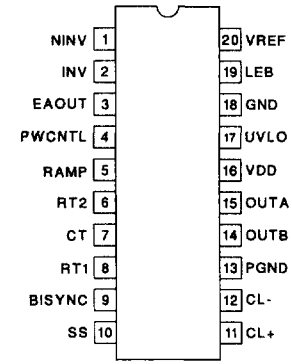
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 15V
Supply Current 25mA
Output Current (OUTA, OUTB, PGND, VCC)
DC 0.5A
Pulsed (0.5µsec) 2.2A
PGND ..... ±0.2V
Analog Inputs
INV, NINV, RAMP, SS ..... –0.3 to 7V
CL+, CL- ..... –1.5V to 6V
Error Amplifier Output Current 5mA
Error Amplifier Output Capacitance 20pF
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

Unless otherwise indicated, voltages are referenced to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-20, SOIC-20 (Top View)
N Package, DW Package



ORDERING INFORMATION

UCC ☐ 829 ☐ - ☐
- ☐ — OUTPUT
- ☐ — PACKAGE
- ☐ — TEMPERATURE RANGE

PART VERSION TABLE

PART NUMBER	OUTPUT	OUT A/B PHASE	OUTPUT FREQUENCY
UCCX829-1	Push-Pull	180°C Out of Phase	Half of -2
UCCX829-2	Single-Ended	In Phase	

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, 0°C to 70°C for the UCC3829-1/-2, –40°C to 85° for the UCC2829-1/-2 and –55°C to 125°C for the UCC1829-1/-2. RT1 = 33.2kΩ, CT = 470pF, RT2 = 392Ω, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C	2.97	3	3.03	V
Line Regulation	4.5V < VDD < 15V	–10		10	mV
Load Regulation	0 < I_{REF} < 5mA			10	mV
Total Output Variation	Line, Load, Temperature	2.94		3.06	V
Short Circuit Current	VREF = 0			25	mA
Oscillator Section					
Initial Accuracy	T_J = 25°C (Note 1)	360	400	440	kHz
Total Variation	Line, Temperature (Note 1)	350		450	kHz
Voltage Stability	12 < VDD < 15			1	%
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note 1)		5	10	%
Initial Accuracy	RT1 = 25.7k, CT = 150pF, T_J = 25°C (Note 1)	0.9	1	1.1	MHz
Total Variation	RT1 = 25.7k, CT = 150pF, Line, Temperature (Note 1)	0.85		1.15	MHz
Ramp Peak		2			V
Ramp Valley				1	V
BISYNC Output Source Current	V_{BISYNC} = VDD – 0.5V		–200	–100	µA
BISYNC Output Sink Current	V_{BISYNC} = 0.5V	2	2.5		mA
BISYNC Input Threshold			1.5		V
Error Amplifier Section					
Input Offset Voltage				5	mV
Input Bias Current		–1		1	µA
Input Offset Current				250	nA
Open Loop Gain		70	80		dB

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, 0°C to 70°C for the UCC3829-1/-2, –40°C to 85° for the UCC2829-1/-2 and –55°C to 125°C for the UCC1829-1/-2. RT1 = 33.2kΩ, CT = 470pF, RT2 = 392Ω, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (cont.)					
CMRR	1.5 < VCM < (VIN – 0.5)	75			dB
PSRR	5 < VDD < 15	75			dB
Output Sink Current	V_{EAOUT} = 1V, 5V < VDD < 15V	300	500		µA
Output Source Current	V_{EAOUT} = 3.5V, 5V < VDD < 15V		500	300	µA
Output High Voltage	I_{EAOUT} = –300µA	3	5		V
Output Low Voltage	I_{EAOUT} = 300µA		0.6	1	V
Gain Bandwidth Product	VDD = 12V, Temperature 25°C	8	10		MHz
Slew Rate		>>1.5	2		V/µs
PWM Comparator Section					
Input Bias Current (RAMP)		–1		1	µA
Minimum Duty Cycle	400kHz			0	%
Maximum Duty Cycle (UCC3829-1)	400 kHz, RT2 Resistor = 1Ω	42.5			%
Maximum Duty Cycle (UCC3829-2)	400kHz, RT2 Resistor = 1Ω	85			%
Delay to Output	T = 25°C T_{YP} = VDD = 12		50	100	ns
Current Limit Fault Section					
Soft Start Charge Current		–30		–10	µA
Full Soft Start Threshold	NINV Voltage		3		V
Restart Discharge Current		10		30	µA
Restart Threshold			1		V
Current Limit Threshold	Relative to CL-		0.875		V
Overcurrent Threshold	Relative to CL-		1.25		V
Current Limit Delay to Output	Over all Temperature, VDD >= 12V		50	100	ns
	Over all Temperature, Supply		100	400	ns
Output Section					
Output Low Saturation	I_{OUT} = 200mA, T_J = 25°C			0.5	V
Output High Saturation	I_{OUT} = –100mA, T_J = 25°C			0.5	V
UVLO Output Low Saturation	At 10mA		0.8	1.5	V
Rise Time	C_{LOAD} = 1nF, TJ = 25°C		20	40	ns
Fall Time	C_{LOAD} = 1nF, TJ = 25°C		10	20	ns
Output Source Current	V_{OUT} = 0, TJ = 25°C, T (Note 1)		–0.75		A
Output Sink Current	V_{OUT} = 12V, TJ = 25°C (Note 1)		1.5		A
Undervoltage Lockout					
UVLO Enable Threshold			3		V
UVLO Hysteresis			0.5		V
VDD UVLO Enable Threshold		13.5		15	V
VDD UVLO Hysteresis		3.5		7	V
Supply Section					
Startup Current	V_{UVLO} = 2, VDD = 13.5			1	mA
ICC	400kHz		8		mA
VDD Range	C_{LOAD} = 0nF	4.25		15	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

BISYNC: Combination clock output/sync input pin. The clock signal can be viewed on this pin. If BISYNC is connected to BISYNC of other UCC3829-1/-2 chips, all the oscillators will run at the highest of all the chips frequencies. The BISYNC pin has a weak pull down and a strong pull up.

CL+: Current sense input for current limiting. The CL+ and CL- pins are used for current sensing. CL+ is the current signal while CL- is the kelvin return for the sensing function.

CL-: Current sense input kelvin common.

CT: Oscillator timing capacitor. A capacitor connected between CT and GND is charged by a current source controlled by RT1. The capacitor is discharged through a resistor connected between CT and RT2.

EAOUT: Error amplifier output. This output is normally connected directly to the RAMP pin. It can also be connected to RAMP through a resistor divider attenuation network to allow more swing of the error amplifier output. A maximum capacitive load of 20pF with respect to ground must be observed to insure stability of the error amplifier.

GND: Logic and analog ground. The GND pin should be used for all signal level returns, except the current sense inputs.

INV: Error amplifier inverting input.

LEB: Leading edge blanking programming pin. Connecting a resistor between VREF and LEB and a capacitor between LEB and GND will program a leading edge blanking time according to the RC of the resistor/capacitor combination. Connecting the LEB pin to VDD disables the Leading Edge Blanking function.

NINV: Error amplifier non-inverting input.

OUTA: Output A. The OUTA pin will pull down with approximately 1.5A and pull up with approximately 0.75A. The UCC3829-1 implements push-pull outputs with OUTA and OUTB active on alternating clock cycles. The UCC3829-2 implements OUTA and OUTB being in phase. The output frequency of the UCC3829-1 is half that of the UCC3829-2 .

OUTB: Output B. The OUTB pin will pull down with approximately 1.5A and pull up with approximately 0.75A. The UCC3829-1 implements push-pull outputs with OUTA and OUTB active on alternating clock cycles. The UCC3829-2 implements OUTA and OUTB being in phase. The output frequency of the UCC3829-1 is half that of the UCC3829-2 .

PGND: Power ground return. The PGND pin should be used as the return for the VDD bypass capacitor and the current sense kelvin CL-.

PWCNTL: Pulse width control input. This is connected to the PWM comparator inverting input.

RAMP: Ramp input . This is connected to the PWM comparator non-inverting input through a level shifting voltage of approximately 1.25V.

RT1: Oscillator charging current programming resistor. A 1V reference at this pin generates a current through a resistor connected between RT1 and GND. This current is mirrored and ratioed to charge the timing capacitor connected to pin CT.

RT2: Oscillator discharge time programming resistor. The oscillator (and output) dead time can be programmed via this pin. The discharge of the timing capacitor C_T is determined by an RC discharge using a resistor connected between RT2 and C_T.

SS: Soft start capacitor pin. A capacitor connected to SS determines the time the IC takes to soft start. The nominal SS pin pull up and pull down current is 20µA. The soft start time delay is approximately calculated as:

$$\frac{Css \bullet 3V}{20\mu A}$$

when charging from 0V. The restart time is approximately:

$$\frac{2 \bullet Css \bullet 3V}{20\mu A}$$

UVLO: Undervoltage lockout programming pin. Connecting a resistor divider between VDD, UVLO, and GND sets a VDD value at which the UCC3829-1/-2 chip will be enabled. When the voltage on the UVLO pin reaches 3V, the chip is enabled. When the voltage on UVLO falls below 2.5V, the chip is disabled.

VDD: Voltage supply to IC.

VREF: Voltage reference output and filtering. The voltage reference output appears on the VREF pin. It is buffered to drive approximately 5mA and short circuit protected at approximately 25mA. A bypass capacitor of at least 0.1µF must be connected from VREF to ground.

DESCRIPTION OF OPERATION

Oscillator

The oscillator uses an external capacitor C_T and two external resistors R_{T1} and R_{T2} to generate the clock frequency and dead time. A precise reference voltage is placed across resistor R_{T1} to generate a current reference. The current is then mirrored and used to charge the capacitor C_T from GND. When a "peak" threshold is reached, an on chip MOSFET connects the RT2 pin to GND, discharging CT to a "valley" threshold through an external resistor R_{T2}. The CT waveform has a linear ramp shape while charging and an exponential (RC) slope while discharging. The slope of the charging ramp is set by the C_T, R_{T1} combination and the slope of the discharging ramp is set by the values of C_T and R_{T2}.

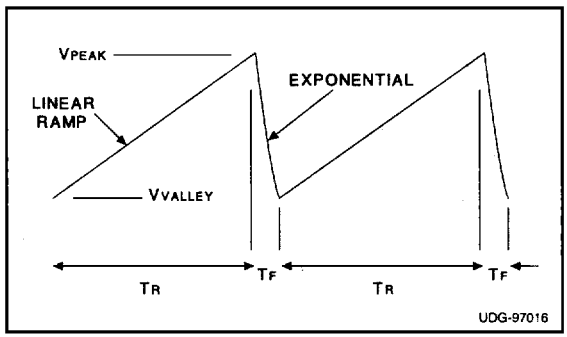


Figure 1.

The approximate equation for the rising edge (T_R) of the C_T waveform (maximum on-time period) is:

$$T_R = C_T R_{T1} \left(\frac{V_{PEAK} - V_{VALLEY}}{9.3} \right)$$

The approximate equation for the falling edge (T_F) of the C_T waveform (deadtime period) is:

$$T_F = R_{T2} C_T 1n \left(\frac{V_{Peak} - \frac{9.3R_{T2}}{R_{T1}}}{V_{VALLEY} - \frac{9.3R_{T2}}{R_{T1}}} \right)$$

Assuming that:

$$\frac{9.3R_{T2}}{R_{T1}} < V_{PEAK} \text{ and } \frac{9.3R_{T2}}{R} T1 << V_{VALLEY}$$

we get a simplified equation:

$$T_F = R_{T2} C_T 1n \left(\frac{V_{PEAK}}{V_{VALLEY}} \right)$$

Given a maximum on-time and frequency and assuming an initial value for either R_{T2} or C_T, you can use the T_F equation to calculate the other. Once you have a value for CT, you can calculate RT1 using the T_R equation .

Error Amplifier Section

The Error Amplifier has both inputs and the output brought out to pins NINV, INV, and EAOUT. The output of the error amplifier can be connected to the inverting input of the PWM comparator via the pin PWCNTL. This allows inserting attenuation which enables using the full output swing of the error amplifier. The output of the error amplifier is forced to follow the soft start waveform during soft start.

PWM and Output Section

The non-inverted input of the PWM comparator is connected to RAMP. The RAMP can be connected to either the C_T capacitor for voltage mode control, to the current sense resistor for current mode control, or to a feed forward capacitor for input voltage feed forward control. The C_T waveform can be coupled to RAMP to provide slope compensation in the current mode case. The MOSFET switch connected to RAMP provides for the discharge of the feedforward capacitor. There is a short time constant (3ns) filter across the inputs of the PWM comparator to reduce noise.

The output of the PWM comparator feeds an OR gate which, together with several other fault signals, sets the PWM latch. The latch is in turn reset on every dead time period of the clock waveform. The output of the PWM latch is OR'ed with the clock and the output of the Fault Latch (described below) to feed into the pulse steering Toggle Flip-Flop (TFF). The resulting signal is then steered to either the A or B output depending on the state of the TFF, enabling use in a push/pull application. The clock output becomes the deadtime between the outputs.

Leading Edge Blanking Section

The Leading Edge Blanking circuit provides a means to insert a blanking period at the beginning of the cycle, providing noise pulse elimination for current mode control applications. This feature is similar to that of the UC3825 and UC3823A/B ICs. When enabled, an external resistor is connected from LEB to VREF. An external capacitor is connected from LEB to either VREF or GND. During the deadtime, LEB is pulled to GND. At the beginning of the cycle, the pin is released and the capacitor charges through the resistor toward VREF. At the threshold VREF/2, a comparator senses the voltage and LEB is re-

DESCRIPTION OF OPERATION

moved. The leading edge blanking function can be disabled by connecting LEB to VDD (> VREF). Leading edge blanking is performed by the same MOSFET switch connected to RAMP that is used for voltage feed forward operation.

Current Sense Section

The current limit and overcurrent functions are accomplished using the pins CL+ and CL-. These two pins provide for differential current level sensing, with the trip points referenced to CL-, rather than GND. The current limit function provides a pulse by pulse current limiting, whereas the overcurrent function is considered a fault condition and initiates a fault logic soft start cycle.

Fault Logic Section

The fault logic detects and handles various fault conditions in the system. The output of the overcurrent comparator is logically ORed with the output combination of the undervoltage detection circuit ORed with the output of the VREF good circuit. The output of the precision reference voltage VREF is compared to a level (approximately 3 V_{BE} voltages) to determine if the reference is alive. The undervoltage circuit either uses a user programmed level with a 16% hysteresis or an on threshold equal to the VDD clamp voltage and an off threshold of 9V.

Once a fault occurs, a soft start cycle takes place. A fault sets the fault latch. The Q output of the fault latch sets the RS delay latch and turns on the 20µA soft start discharge current sink. The Q output of the fault latch is gated, however, by the output of the Ss complete comparator. This insures that a SS cycle cannot start before the previous one has finished. The soft start capacitor then is discharged to 1V which is sensed by the Rs delay comparator. The fault latch is then reset. This in turn resets the Rs delay latch and turns off the 20µA current sink and turns on a 20µA current source to charge the Ss capacitor.

The under voltage detection is set to a default value of 14V turn on (VDD clamp active value) and 9V turn off when the UVLO pin is tied to GND. This default configuration can be overridden by connecting a resistor divider between VDD and GND to the UVLO pin. The hysteresis for the user set threshold is 16%.

Supply Section

The incoming voltage supply VDD is clamped by a shunt VDD Clamp circuit.

APPLICATION INFORMATION

Please see Application Note U-128 for further information.

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