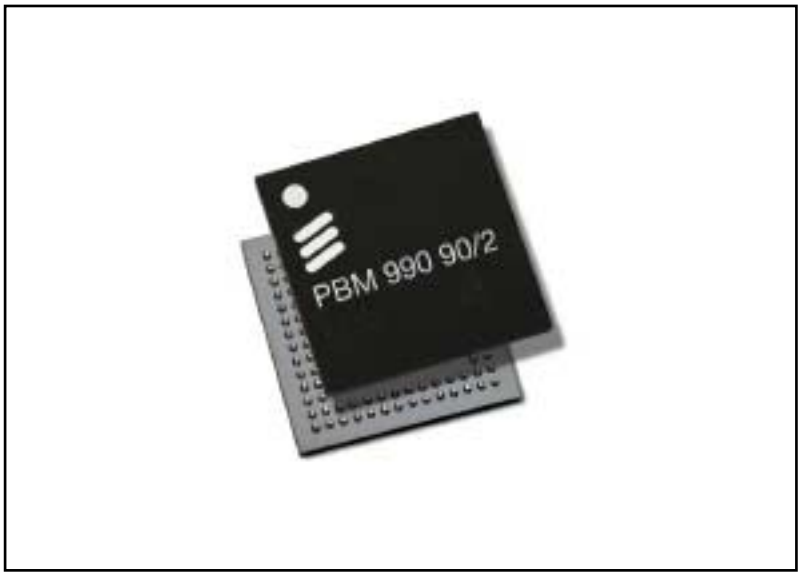
Bluetooth™ Baseband Controller

Key Features

- Variable input clock frequency
- Two 16C550 UART interfaces
- Up to 10 bits general purpose IO
- I^2C interface
- USB 2.0 Full-speed compliant interface
- JTAG Debug & Test interface
- Capability for embedded solutions
- External flexible Flash sizes, 2–16 Mbit
- Point to multipoint, 7 slaves
- Power management, PARK, SNIFF & HOLD
- Qualified for Bluetooth spec. 1.1



Description

The Bluetooth Baseband PBM 990 90 from Ericsson Microelectronics is a generic baseband controller designed to be suitable for both host and embedded applications. The baseband controller will together with a radio module and a Flash memory form a complete Bluetooth system. As the PBM 990 90 is a generic product, it can be used for many different types of applications that require Bluetooth capability such as:

- Data and Voice access points
- Cable replacement
- Ad hoc networking

The PBM 990 90 is based on the scalable Ericsson Bluetooth Core (EBC) architecture.

The system controller is an embedded ARM7 TDMI™ microprocessor communicating with the EBC and peripheral interfaces over an AMBA™ system bus. This configuration allows for embedded stand-alone Bluetooth applications where your target application is embedded within the baseband controller, in addition to traditional host-based applications. This possibility is especially useful in accessory type applications like cordless headsets, industrial sensor and actuator devices. Providing a wide range of external interfaces like USB, I^2C, GPIO, PCM and a pair of UARTS, the PBM 990 90 is ideally suited for access applications in desktop and mobile computing environments, home base stations, and hot spot network access points.

Block diagram

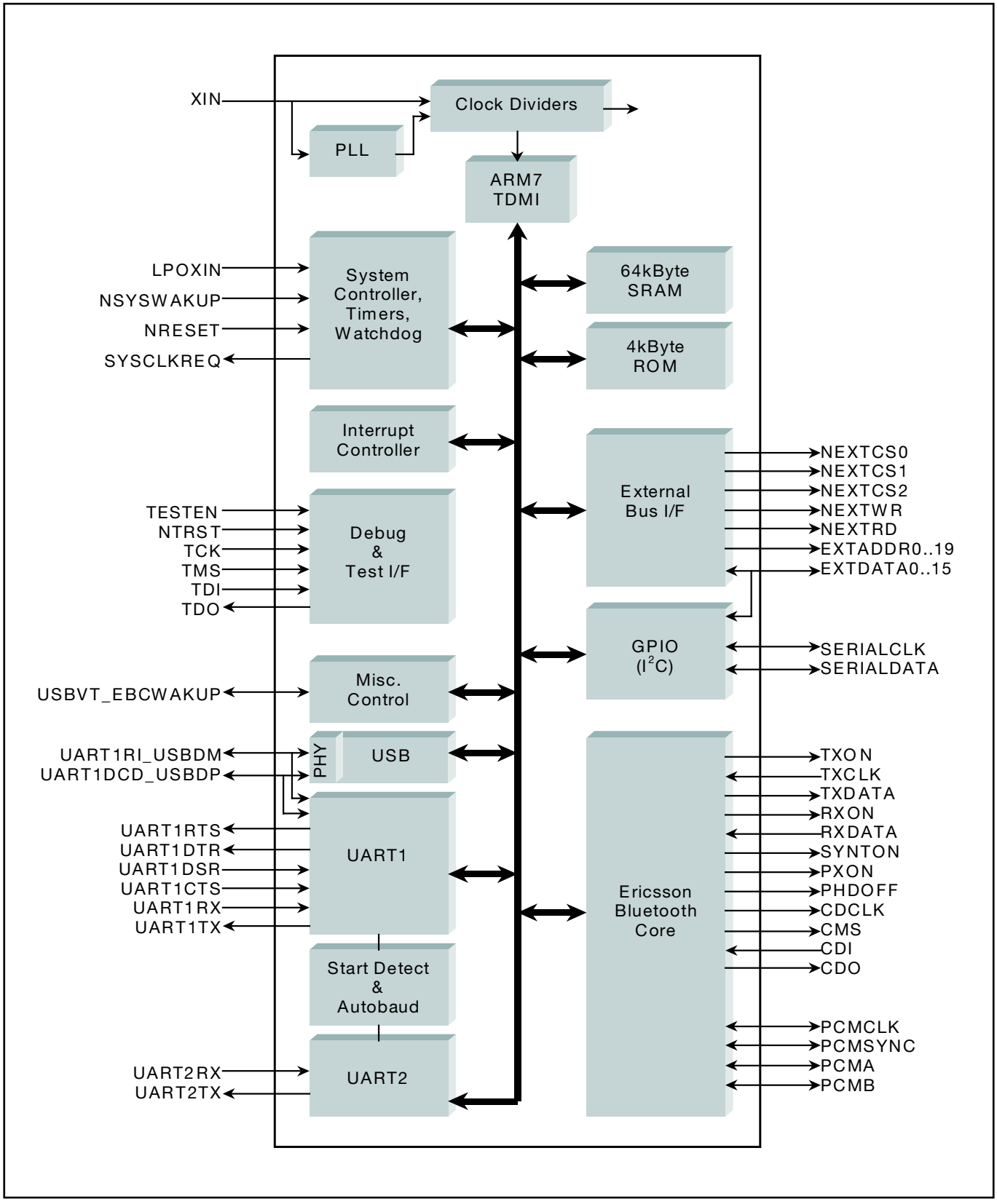


Figure 1. Block diagram.

Absolute Maximum Ratings

Parameter	Condition	Symbol	Min	Typ	Max	Unit
I/O supply range, all groups		V_{DDIO}	-0.3		+3.6	V
Core supply range		V_{DDCORE}	-0.3		+2.8	V
Input voltage range		V_I	-0.3		V_{DDIO} +0.3	V
Output voltage range		V_O	-0.3		V_{DDIO} +0.3	V
Input clamp current $V_O < V_{SSIO}$ or $V_I > V_{DDIO}$		I_{IC}	-20		+20	mA
Output clamp current $V_O < V_{SSIO}$ or $V_I > V_{DDIO}$		I_{OC}	-20		+20	mA
Operating ambient temperature range		T_{Amb}	-40		+85	°C
Storage temperature		T_{Stg}	-40		+125	°C

Characteristic Data

Static data

Unless otherwise stated: V_{DDCORE} & V_{DDIO} = 2.5V ;V_{SS} = 0 V ; T_{Amb} = -40..+85°C

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Supply voltage Core & PLL [1]		V_{DDCORE}	2.3	2.5	2.7	V
Supply voltage IO group 1		V_{DDIO1}	V_{DDCORE} [1]	2.5	3.6	V
Supply voltage IO group 2		V_{DDIO2}	V_{DDCORE} [1]	3.3	3.6	V
Supply voltage IO group 3		V_{DDIO3}	V_{DDCORE} [1]	2.5	3.6	V
Supply voltage IO group 4		V_{DDIO4}	V_{DDCORE} [1]	2.5	3.6	V
Supply current		I_{DD}		TBD		mA
Low level input voltage, digital input	Guaranteed input low	V_{IL}	V_{SSIO} – 0.3		$0.3 \times V_{DDIO}$	V
High level input voltage, digital input	Guaranteed input high	V_{IH}	$0.7 \times V_{DDIO}$		V_{DDIO}+0.3	V
Schmitt trigger input	Min Hysteresis = 0.49	V_T +	1.42	1.45	1.46	V
Schmitt trigger input	Min Hysteresis = 0.49	V_T -	0.92	0.94	0.97	V
Input leakage current	$V_I = V_{SSIO}$ $V_I = V_{DDIO}$	I_{LI}	-1		+1	µA
Low level output voltage	I_{OL} =800 µA	V_{OL}	0		V_{SSIO}+0.1	V
High level output voltage	I_{OH} =-800 µA	V_{OH}	V_{DDIO} -0.1		V_{DDIO}	V
Output leakage current, tri-state	$V_O = V_{SSIO}$ $V_O = V_{DDIO}$	I_{OT}	-10		+10	µA

Notes on static data:

1) If the core voltage is greater than either of the I/O voltages by about 0.5 V or more, then PBM 990 90 will not work. This is because the inputs to the core from the pads will not be sufficiently high level to drive the core gates. The level shifter between core and I/O is only designed to shift from low core to a high I/O.

2) If the core voltage is off, but the the I/O voltage is left on, then this will cause PBM 990 90 to drive out a logic low on all output pins. For example NEXTWR, NEXTRD, EXTDATA and all three NEXTCS signals will be driven low which will result in a Bidirectional clash on the databus if several external units are driving the bus.

3) All PBM 990 90 I/O pins can be connected to any external driving bus of max 3.6 V before turning on the supply, without the chip being damaged. However it cannot be guaranteed that PBM 990 90 does not load the external bus in this case, unless the core supply voltage is completely discharged prior to this event.

Dynamic data

Requirements on all input pins

Conditions:
Rise and fall times are measured between 10% to 90% of the VDDIO level.

Type	Symbol	Parameter	Min	Max	Unit
All input pins	tr	Rise time		10	ns
	tr	Fall time		10	ns

Requirements on XIN pin

Input frequency	Symbol	Parameter	Min	Max	Unit
Without using the PLL:12.40 MHz	facc	Frequency accuracy	-20	+20	ppm
	tj	Jitter	TBD	TBD	ns
	tdc	Duty cycle	TBD	TBD	%
Using the PLL:	facc	Frequency accuracy	-20	+20	ppm
Example frequencies:	tj	Jitter	TBD	TBD	ns
12.60, 12.80, 13.00, 14.40, 16.80, 19.20, or 19.44 MHz	tdc	Duty cycle	TBD	TBD	%

Requirements on LPOXIN pin

Input frequency	Symbol	Parameter	Min	Max	Unit
3.200 kHz	facc	Frequency accuracy		250	ppm
	tj	Jitter	TBD	TDB	µs
	tdc	Duty cycle	TBD	TBD	%
32.000 kHz	facc	Frequency accuracy		250	ppm
	tj	Jitter	TBD	TBD	µs
	tdc	Duty cycle	TBD	TBD	%
32.768 kHz	facc	Frequency accuracy		50	ppm
	tj	Jitter	TBD	TBD	µs
	tdc	Duty cycle	TBD	TBD	%

Digital output pins characteristics

Conditions:
T_{Amb} = -40 .. +85 °C, C_{Load} = 25 pF, V_{DDCORE} = 2.3 V .. 2.7V, V_{DDIO} = 2.3 .. 3.3 V
Rise and fall times are measured between 10 % to 90 % of the VDDIO level.

Type	Symbol	Parameter	Min	Max	Unit
All digital output and bi-directional output	tr	Rise time	3.5	10.0	ns
pins (3x drive, 6 mA)	tf	Fall time	3.5	10.0	ns

USB Transceiver pins characteristics

Conditions:
T_{Amb} = -40 .. +85 °C, C_{Load} = 50 pF, V_{DDCORE} = 2.3 V .. 2.7 V, V_{DDIO2} = 3.3 V

Symbol	Parameter	Min	Typ	Max	Unit
tr, tf	Transition Rise or Fall time	4	10	20	ns
tr/tf	Transition Rise/Fall time ratio	0.9	1.0	1.1	
V_{CR}	Cross-over voltage	1.3		2.0	V
Z_{DRV}	Driver output resistance (See Note)		16	28	Ω

Note:

Excluding external resistor. In order to comply with USB specification, external resistors of 14 Ω ±5 % on each of the D+ and D- branches are recommended.

PLL characteristics

To generate higher internal clock frequencies from the input clock XIN an on-chip PLL is included in PBM 990 90. The PLL can be adapted to different input frequencies by programmable registers. Register values for the following common crystal frequencies have been defined: 12.60, 12.80, 13.00, 14.40, 16.80, 19.20 and 19.44 MHz.

The PLL is fed by an internal current reference block, IREF, which can be disabled when the PLL is not used in order to save power. The start-up time of the PLL is dependent on whether the IREF is enabled prior to start of the PLL or not.

Symbol	Parameter	Min	Typ	Max	Unit
f_{in}	Input frequency		13.00		MHz
t_{st1}	Start-up time, IREF enabled before start			100	µs
t_{st2}	Start-up time, IREF disabled before start			140	µs

Connection

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	EXT DATA1	EXT DATA0	NEXTRD	EXT ADDR0	NEXT CS0	EXT DATA6	EXT ADDR16	VDDIO1	VDD CORE	UART2 RX	NRESET	PCMA	PCMB	PCM CLK
B	EXT DATA10	EXT DATA9	EXT DATA8	EXT DATA3	EXT DATA11	VSSIO3	XIN	VSS CORE	UART2 TX	VSSIO1	USBVT_ EBC WAKUP	PCM SYNC	UART1 RTS	UA RT1 DTR
C	EXT DATA4	EXT DATA2											UART1 DSR	UART1 CTS
D	VDDIO3	VSSIO3											VSSIO2	VDDIO2
E	EXT DATA13	EXT DATA12											UART1 RX	UART1 TX
F	EXT DATA7	EXT DATA15											UART1 RI_ USBDM	UART1 DCD_ USBDP
G	EXT ADDR15	EXT ADDR9											PHDOFF	TXDATA
H	EXT ADDR14	EXT DATA14											SYNT ON	CDCLK
J	EXT ADDR13	EXT ADDR17											CMS	CDO
K	VDDIO3	VSSIO3											CDI	LPOXIN
L	EXT ADDR11	EXT ADDR6											PXON	SYSCLK REQ
M	EXT ADDR8	EXT ADDR3											TXCLK	TXON
N	NEXT WR	EXT ADDR1	EXT ADDR2	EXT ADDR5	EXT DATA5	EXT ADDR12	NEXT CS1	VSS CORE	SERIAL CLK	VSSIO4	TESTEN	TCK	RXDATA	RXON
P	EXT ADDR19	EXT ADDR7	EXT ADDR4	EXT ADDR18	EXT ADDR10	VDD CORE	NEXT CS2	NSYS WAKUP	SERIAL DATA	VDDIO4	NTRST	TMS	TDI	TDO

	Core supply pins
	I/O group 1 pins
	I/O group 2 pins
	I/O group 3 pins
	I/O group 4 pins

Figure 2. Pin configuration (top view, balls face down).

Pin description

Pin no.	Pin name	IO direction	Pad type	Reset state	IO group	Functional description
Input clock interface (1 pin)						
B7	XIN	I	DI		1	System input clock (square wave)
System controller interface (4 pins)						
A11	NRESET	I	DIS		1	System reset (active low)
K14	LPOXIN	AI	ANA		4	Low power operation clock (square wave)
P8	NSYSWAKUP	I	DI		4	System external wakeup (active low)
L14	SYSCLKREQ	O	DO3T	H	4	System clock request (tri-stateable)
USB Vterm & EBC wakeup interface (1 pin)						
B11	USBVT_EBCWAKUP	I/O	BD3	Z	2	USB Vterm or EBC wakeup
External bus interface (41 pins)						
A5	NEXTCS0	O	DO3	H	3	External bus chip select 0
N7	NEXTCS1	O	DO3	H	3	External bus chip select 1
P7	NEXTCS2	O	DO3	H	3	External bus chip select 2
A3	NEXTRD	O	DO3	H	3	External bus read strobe
N1	NEXTWR	O	DO3	H	3	External bus write strobe
A4	EXTADDR0	I/O	BD3	L	3	External bus address line 0
N2	EXTADDR1	I/O	BD3	L	3	External bus address line 1
N3	EXTADDR2	I/O	BD3	L	3	External bus address line 2
M2	EXTADDR3	I/O	BD3	L	3	External bus address line 3
P3	EXTADDR4	I/O	BD3	L	3	External bus address line 4
N4	EXTADDR5	I/O	BD3	L	3	External bus address line 5
L2	EXTADDR6	I/O	BD3	L	3	External bus address line 6
P2	EXTADDR7	I/O	BD3	L	3	External bus address line 7
M1	EXTADDR8	I/O	BD3	L	3	External bus address line 8
G2	EXTADDR9	I/O	BD3	L	3	External bus address line 9
P5	EXTADDR10	I/O	BD3	L	3	External bus address line 10
L1	EXTADDR11	I/O	BD3	L	3	External bus address line 11
N6	EXTADDR12	I/O	BD3	L	3	External bus address line 12
J1	EXTADDR13	I/O	BD3	L	3	External bus address line 13
H1	EXTADDR14	I/O	BD3	L	3	External bus address line 14
G1	EXTADDR15	I/O	BD3	L	3	External bus address line 15
A7	EXTADDR16	I/O	BD3	L	3	External bus address line 16
J2	EXTADDR17	I/O	BD3	L	3	External bus address line 17
P4	EXTADDR18	O	DO3	L	3	External bus address line 18
P1	EXTADDR19	O	DO3	L	3	External bus address line 19
A2	EXTDATA0	I/O	BD3	L	3	External bus data line 0
A1	EXTDATA1	I/O	BD3	L	3	External bus data line 1
C2	EXTDATA2	I/O	BD3	L	3	External bus data line 2
B4	EXTDATA3	I/O	BD3	L	3	External bus data line 3
C1	EXTDATA4	I/O	BD3	L	3	External bus data line 4
N5	EXTDATA5	I/O	BD3	L	3	External bus data line 5
A6	EXTDATA6	I/O	BD3	L	3	External bus data line 6
F1	EXTDATA7	I/O	BD3	L	3	External bus data line 7
B3	EXTDATA8	I/O	BD3	L	3	External bus data line 8 or GPIOB0
B2	EXTDATA9	I/O	BD3	L	3	External bus data line 9 or GPIOB1

Pin no.	Pin name	IO direction	Pad type	Reset state	IO group	Functional description
B1	EXTDATA10	I/O	BD3	L	3	External bus data line 10 or GPIOA2
B5	EXTDATA11	I/O	BD3	L	3	External bus data line 11 or GPIOA3
E2	EXTDATA12	I/O	BD3	L	3	External bus data line 12 or GPIOA4
E1	EXTDATA13	I/O	BD3	L	3	External bus data line 13 or GPIOA5
H2	EXTDATA14	I/O	BD3	L	3	External bus data line 14 or GPIOA6
F2	EXTDATA15	I/O	BD3	L	3	External bus data line 15 or GPIOA7
I²C interface (2 pins)						
N9	SERIALCLK	I/O	BD3	I	4	I2C serial clock (GPIOA0)
P9	SERIALDATA	I/O	BD3	I	4	I2C serial data (GPIOA1)
PCM interface (4 pins)						
A12	PCMA	I/O	BD3	I	2	PCM digital serial audio channel A
A13	PCMB	I/O	BD3	I	2	PCM digital serial audio channel B
A14	PCMCLK	I/O	BD3	I	2	PCM digital serial audio clock
B12	PCMSYNC	I/O	BD3	I	2	PCM digital serial audio sync pulse
Radio interface (12 pins)						
M13	TXCLK	I	DI		4	Radio transmit data clock, 1 MHz
G14	TXDATA	O	DO3	X	4	Radio transmit data
M14	TXON	O	DO3	L	4	Radio transmitter on
G13	PHDOFF	O	DO3	L	4	Radio phase detector loop off
L13	PXON	O	DO3	L	4	Radio packet on
H13	SYNTON	O	DO3	L	4	Radio synthesizer on
N13	RXDATA	I	DI		4	Radio receive data
N14	RXON	O	DO3	L	4	Radio receiver on
H14	CDCLK	O	DO3	H	4	Radio serial control clock
K13	CDI	I	DI		4	Radio serial control data input
J14	CDO	O	DO3	L	4	Radio serial control data output
J13	CMS	O	DO3	L	4	Radio serial control mode select
UART1 & USB interface (8 pins)						
C14	UART1CTS	I	DI		2	UART1 clear to send
C13	UART1DSR	I	DI		2	UART1 data set ready
B14	UART1DTR	O	DO3	H	2	UART1 data terminal ready
B13	UART1RTS	O	DO3	H	2	UART1 request to send
E13	UART1RX	I	DI		2	UART1 receive data
E14	UART1TX	O	DO3	H	2	UART1 transmit data
F14	UART1DCD_USB DP	I/O	BD3, PHY	I	2	UART1DCD or USBDP
F13	UART1RI_USBDM	I/O	BD3, PHY	I	2	UART1RI or USBDM
UART2 interface (2 pins)						
A10	UART2RX	I	DI		1	UART2 receive data
B9	UART2TX	O	DO3	H	1	UART2 transmit data

Pin no.	Pin name	IO direction	Pad type	Reset state	IO group	Functional description
Debug & Test interface (6 pins)						
N11	TESTEN	I	DID		4	Test enable (pull-down, active high)
N12	TCK	I	DIU		4	JTAG clock (pull-up)
P13	TDI	I	DIU		4	JTAG data in (pull-up)
P14	TDO	O	DO3T	Z	4	JTAG data out
P12	TMS	I	DIU		4	JTAG mode select (pull-up)
P11	NTRST	I	DID		4	JTAG reset (pull-down)
Power (15 pins)						
A9	VDDCORE		CP, ANA			Core & PLL VDD supply
P6	VDDCORE		CP			Core VDD supply
A8	VDDIO1		IOP		1	IO1 group VDD supply
D14	VDDIO2		IOP		2	IO2 group VDD supply
K1	VDDIO3		IOP		3	IO3 group VDD supply
D1	VDDIO3		IOP		3	IO3 group VDD supply
P10	VDDIO4		IOP		4	IO4 group VDD supply
B8	VSSCORE		GND, ANA			Core & PLL ground
N8	VSSCORE		GND			Core ground
B10	VSSIO1		GND		1	IO1 group ground
D13	VSSIO2		GND		2	IO2 group ground
K2	VSSIO3		GND		3	IO3 group ground
D2	VSSIO3		GND		3	IO3 group ground
B6	VSSIO3		GND		3	IO3 group ground
N10	VSSIO4		GND		4	IO4 group ground

Notes on the pin description:

IO direction:

I = Input, O = Output, I/O = Bi-directional, AI = Analog input

Reset state:

H = High, L = Low, Z = Tri-state, X = High or Low

Pad types:

DI	=	Input pad
DIU	=	Input pad with pull-up (Resistor: Min 30 kΩ, Typ 50 kΩ, max 80 kΩ)
DID	=	Input pad with pull-down (Resistor: Min 10 kΩ, Typ 20 kΩ, max 30 kΩ)
DIS	=	Schmitt trigger input pad
ANA	=	Analog pad
DO3	=	3x drive, 6 mA output pad
DO3T	=	Tri-stateable 3x drive, 6 mA output pad
BD3	=	3x drive, 6 mA bi-directional output pad
CP	=	Core VDD power supply pad
IOP	=	I/O VDD power supply pad
GND	=	VSS power supply pad
PHY	=	USB transceiver pad shared with UART1 RI and DCD pins.

Other information:

All pins which are defined as inputs in the application and are not connected to any driving external circuit must be pulled to either VDDIO or VSS i.e. must not be floating. The only pins that have on-chip pull resistors are the Debug & Test Interface input pins. All pin names that start with an “N” are active low.

Mechanical description, 96 pin BGA package

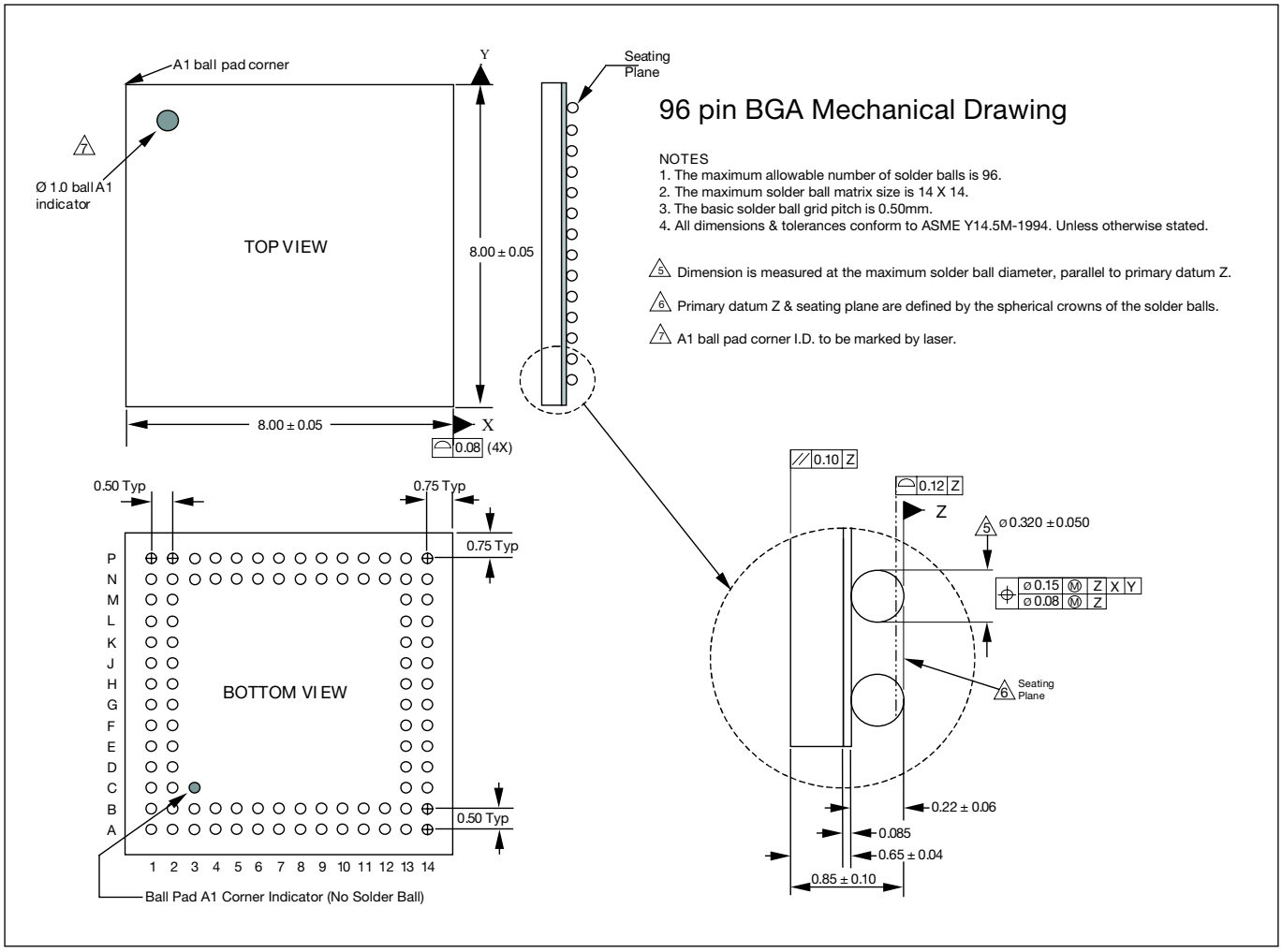


Figure 3. Mechanical Drawing.

Functional Description

Overview

The purpose of this section is to give a brief description of the features and functions in the PBM 990 90 product and how it can work in a system. See figure 4.
PBM 990 90 is a one-chip solution, packaged into a 96 pin BGA package, 8×8 mm footprint with 0.50 mm pin pitch and 0.85 mm building height.
PBM 990 90 handles the baseband functionality in a Bluetooth radio link, i.e. the digital controller logic. The baseband functionality is partitioned in one hardware and one software part. The software part is executed by an on-chip microprocessor ARM7 TDMI. To increase the ease of use, standard interfaces like USB 2.0 Full-speed, UARTs, PCM and I^2C are integrated on the chip. The PBM 990 90 philosophy is to provide a scalable solution with a high level of flexibility. The goal is to offer a solution that can be easily added to an existing system thus enabling Bluetooth capabilities. The solution offers designers:

- Power versus performance trade-offs
- Reduced need for external components (osc's, USB PHY etc)

To save power, all interfaces can individually be turned off and the processor speed can be adapted to produce a suitable capacity depending on what application is running. The radio part requires a crystal or a clock frequency with 20 ppm accuracy. The PBM 990 90 is designed to be flexible in this matter and can re-use a square clock signal for a wide spectrum of frequencies depending on the kind of reference signal used by the radio. The PBM 990 90 software is also able to offer flexibility in the choice of brand and size for the Flash memory.

Architecture

The Bluetooth functionality is based on both hardware and software, forming an embedded system design targeting both flexibility and scalability. The system architecture is based around an ARM7 TDMI processor, executing the Bluetooth stack drivers, and a Hardware block: Ericsson Bluetooth Core supporting Bluetooth Standard 1.1. The supported interfaces: USB 2.0 Full-speed and UARTs are used to access the chip from a host system.
Peripheral components such as Flash, RAM, ROM, etc. can be connected through the External Bus Interface. The External Bus Interface is configurable to fit a variety of peripheral components. The PBM 990 90 together with a Bluetooth radio and a Flash holding the firmware, forms a Bluetooth radio link, see figure 5.

Ericsson Bluetooth Core (EBC)

EBC is the name of the Bluetooth dedicated hardware designed to offload the processor by taking care of heavy calculation tasks such as whitening, CRC check, ciphering of data, forward error correction and Bluetooth packet segmentation & reassemble. EBC is compliant with the Bluetooth specification revision 1.1 and includes the following key features:

- ACL link support giving data rates up to 721 kbit/s over the air interface.
- SCO link with support for up to three voice channels over the air interface.
- HW support for all packet types.
- Support for one PCM-channel.
- Architecture designed for low power consumption.
- Hold, sniff, parked modes
- Ciphering keys up to 128 bits
- High quality filtering of voice packets enables excellent audio quality.
- Flexible voice formats to host and over air (CVSD, PCM, 16/8 bit 1st and 2nd complement, signed, A-law, μ-law).
- Point to multipoint with support for up to 7 slaves.
- Master/Slave switch capability
- Radio interface is compliant with BlueRF interface V0.9, Unidirectional mode, RXMODE2.

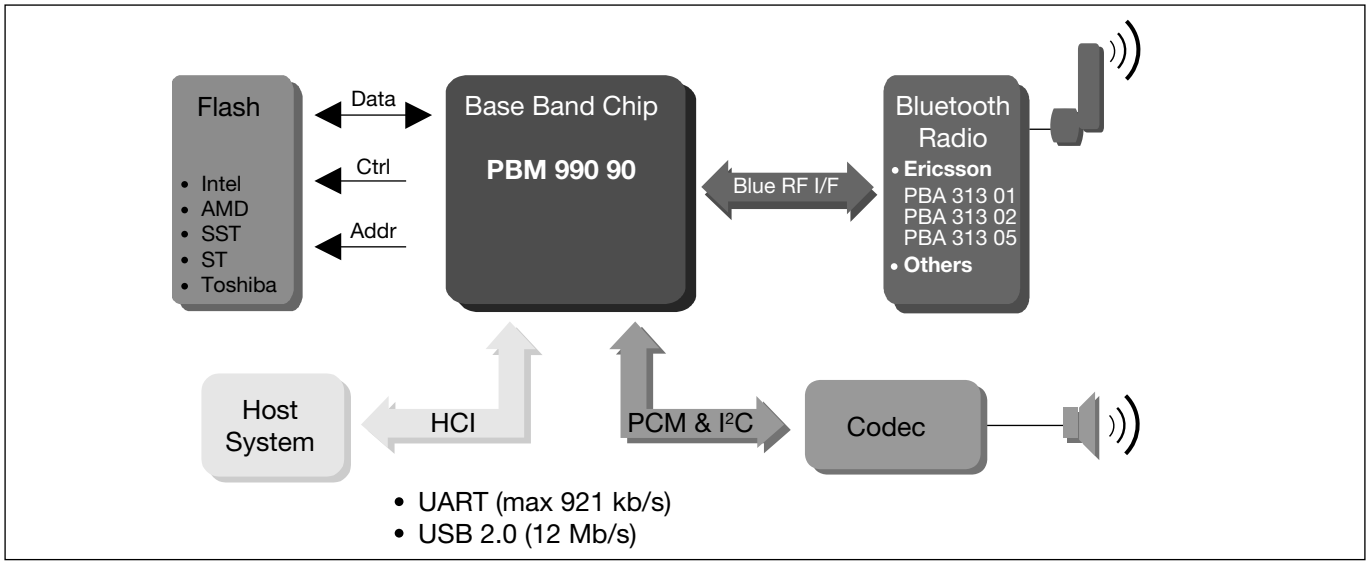


Figure 4. Example system using PBM 990 90.

Host interfaces

To enable a host system to access the Bluetooth radio link, a Host Controller Interface (HCI) has been defined. The host system controls and distributes data to and from the Bluetooth Link Manager with a set of commands. These commands are carried physically on either the USB or UART interface.

USB 2.0 Full-speed

USB is a serial interface supporting a 12 Mbit/s. The interface is “Plug and Play” – to its nature and is therefore easy to use for equipment that is constantly moved around. The USB interface implemented in PBM 990 90 is based on the 2.0 Full-speed version of the USB standard and is configured for 6 endpoints:

- Control endpoint with 8 bytes buffer.
- 2 Isochronous endpoints (Rx/Tx) – Double buffered with 64 bytes in each buffer.
- 2 Bulk transfer endpoints (Rx/Tx) – Double buffered with 64 bytes in each buffer.
- Interrupt endpoint with 16 bytes buffer.

The USB is divided into three parts, USB PHY, USB core, and USB driver software integrated in the firmware. PBM 990 90 has an integrated PHY, the necessary analog line driver for USB signalling, thus avoiding an external component. The simplified USB pin configuration where only D+ and D- are used, means that the interface does not require to be fed power from the USB host. The USB core is the digital hardware part handling packet transmission and reception. It also handles low level control. The USB software driver is integrated in the firmware delivered with the chip.

Measured throughput (USB-airlink-USB)

Packet type	Full Duplex	Half Duplex
DH5	420/420 kbit/s	705 kbit/s

UARTs

There are two on-chip UART 16C550 compatible interfaces, UART1 and UART2.

UART1 has 128 byte FIFOs and full modem control support and is used for data transmission at bit rates up to 921 kbit/s.
UART1 is setup to a DTE configuration as default. It can be changed to a DCE configuration by software. RI and DCD then become outputs, CTS is swapped with RTS and DSR is swapped with DTR externally.

Pin Name	DTE configuration	DCE configuration
UART1CTS	Clear To Send input	Request To Send input
UART1DSR	Data Set Ready input	Data Terminal Ready input
UART1DCD	Data Carrier Detect input	Data Carrier Detect output
UART1RI	Ring Indicator input	Ring Indicator output
UART1RTS	Request To Send output	Clear To Send output
UART1DTR	Data Terminal Ready output	Data Set Ready output

The other UART, UART2 has 16 byte FIFOs and is used for control and/or boot. UART2 has only the TX and RX pins available and can support bit rates up to 230 kbit/s. Start-detect and Auto-baud functionality is available for both UARTs.

Default Settings UART1, UART2	
Speed	57600 bit/s
Data bit	8 bit
Stop bit	One
Parity	None
Flow	CTS/RTS (Not applicable for UART2)

Note: These settings can be changed from the HCI level using Ericsson specific commands.

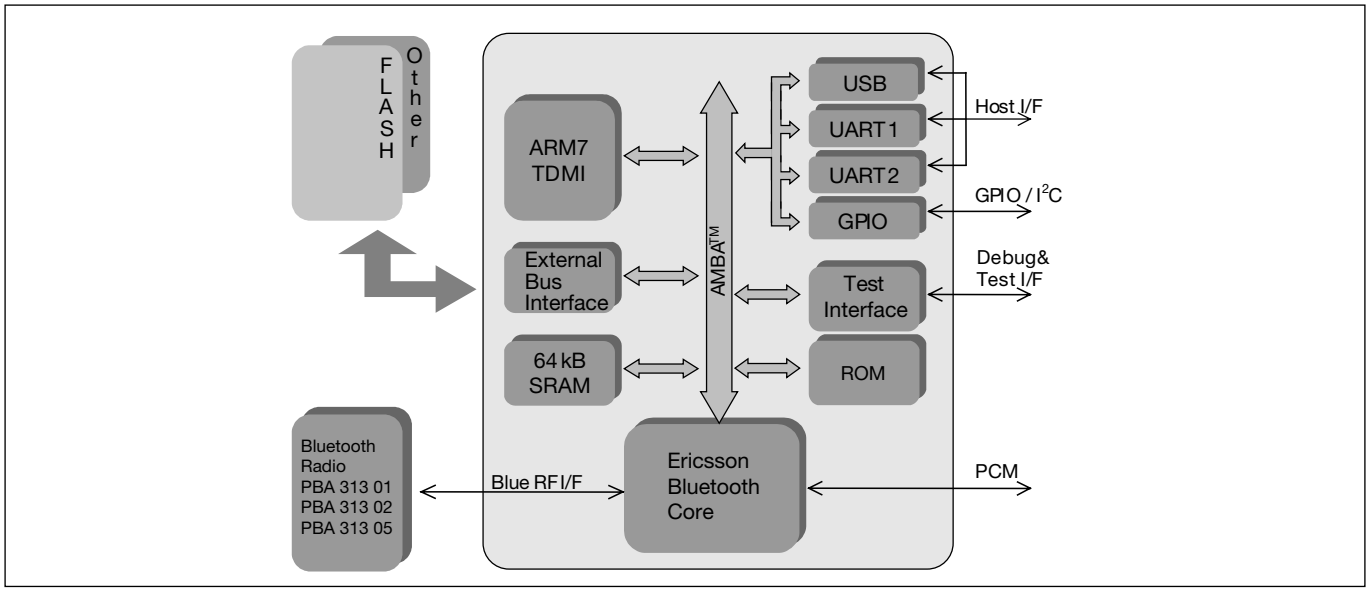


Figure 5. Architecture.

Other interfaces

External Bus Interface

The External Bus Interface allows the designer to add peripheral circuits included in the PBM 990 90 memory map. It has support for three memory banks each offering an address range of 1024 k positions and individually configurable by memory mapped registers as described below.
Memory bank 0 is used by the Flash memory holding the firmware executing on the processor. Bank 1 and 2 can be used to expand the RAM or to add other components.
Each memory bank can be configured according to the table to the right:

Configuration type	Options
Access type	No retry, Retry after every access or Retry after every four memory accesses
Memory width	8- or 16-bit
Burst mode	Non-burst devices or burst ROM
Write protect	On / Off
Write protect error status flag	Error, No error or Clear flag
Bus transfer error status flag	Error, No error or Clear flag
Wait state for write accesses	1..32 internal system clock cycles wait state(s) (SRAM) or 0..31 clock cycles wait state(s) (burst ROM)
Wait state for read accesses	1..32 internal system clock cycles wait state(s)
Bus turnaround cycles between read & write	1..16 internal system clock cycles wait state(s) access

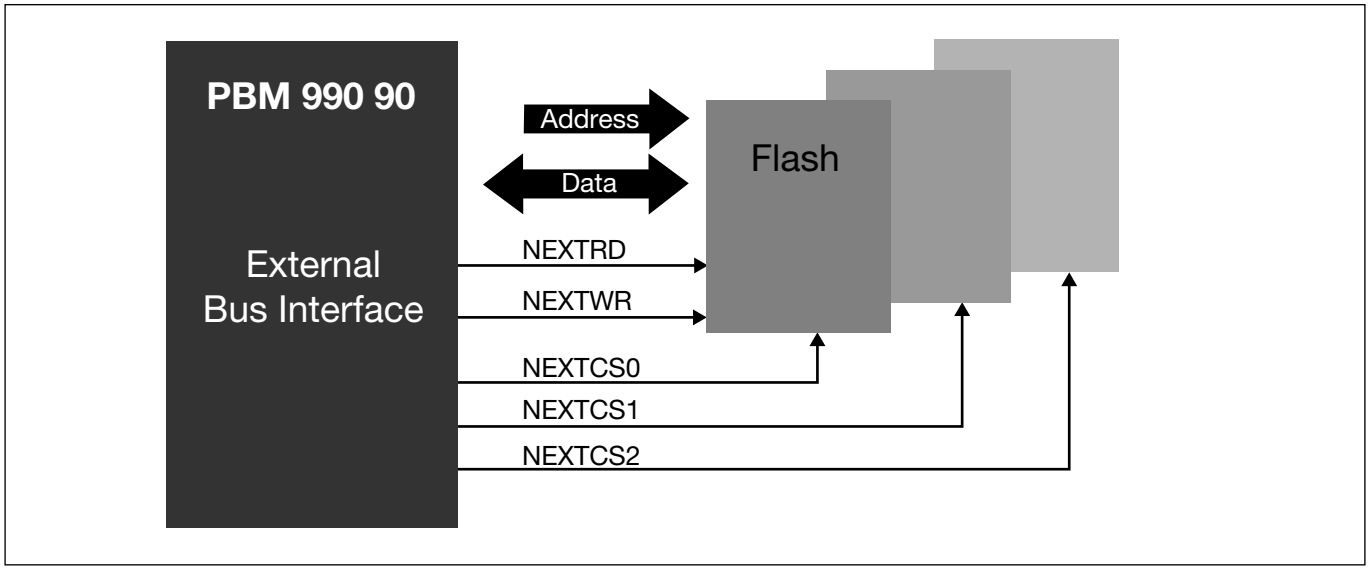


Figure 6. External bus interface.

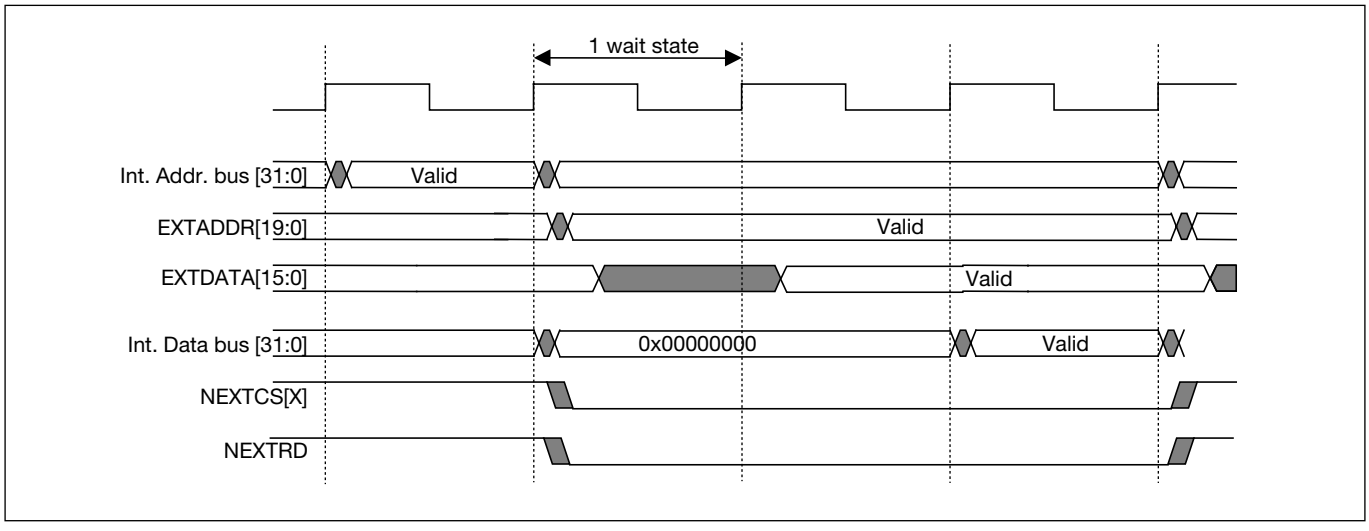


Figure 7. Example of an external bus one wait state read access.

GPIO / I²C

PBM 990 90 supports up to 10 bit General Purpose I/O's. 2 bits GPIO are available by default and these are also used as the I²C interface. 8 bits extra GPIO can be obtained by using the 8 most significant bits of the 16 bit data bus. The I²C interface function is based on software using two GPIO's. The interface has a capacity of handling approximately 100 kbit/s.

The different configurations of GPIO is controlled by the memory mapped registers described below.

GPIO register name	Function
GPIOACCEN	Select between 16 bit external data bus or 8 bit external data bus + 8 extra GPIO.
GPIOPADDR	Data direction register for GPIOA bits. Each GPIOA bit can be setup to either an input or output.
GPIOPBDDR	Data direction register for GPIOB bits. Each GPIOB bit can be setup to either an input or output.
GPIOPADR	Data register for GPIOA bits. This register is used to apply or read data from the GPIOA bits.
GPIOPBDR	Data register for GPIOB bits. This register is used to apply or read data from the GPIOB bits.
GPIOINTC1	Interrupt control register 1. This register selects one of the available GPIO bits to be connected to GPIO interrupt 1. It also sets up the polarity and edge properties, enable and clear for the interrupt.
GPIOINTC2	Interrupt control register 2. This register selects one of the available GPIO bits to be connected to GPIO interrupt 2. It also sets up the polarity and edge properties, enable and clear for the interrupt.

PCM

The PCM Interface (PIF) in the EBC block provides an interface between the serial PCM transfer lines and the Receive and Transmit voice blocks inside the EBC. This interfacing task involves:

- Synchronization between two asynchronous clock domains
- Direction switching of the bi-directional PCM data and control signals
- Synchronous serial data to parallel data conversion.

The EBC supports one PCM channel on the PCM interface.

The PCM line interface can act either as slave or master. When the PCM line interface is slave the frequency range of PCMCLK (in) is 200 kHz to 2 MHz. When the PCM line interface is master PCMCLK (out) is always 2 MHz.
Each PCM symbol received on the PCMA or PCMB in line is organized as an 8 or 16-bit sequence of bits, arriving synchronous to PCMCLK in (if the PCM line interface is slave) or PCMCLK out (if the PCM line interface is master). The symbol starts with its most significant bit arriving after a positive edge on the PCMCLK in (or out), one clock cycle after a PCMSYNC in (or out) positive transition. The symbol is then transferred by one bit each PCMCLK in (or out) clock cycle until the least significant bit is transferred. The EBC then samples the arriving bit at falling edges of PCMCLK in (or out).
The PCM symbols are transmitted bit by bit starting with the MSB, one clock cycle after a positive edge on the PCMCLK in (if the PCM line interface is slave) or PCMCLK out (if the PCM line interface is master), one clock cycle after an PCMSYNC (in or out) positive transition. The rest of the bits are then transferred by one bit each PCMCLK (in or out) cycle, and are synchronized with the rising edge of this clock.

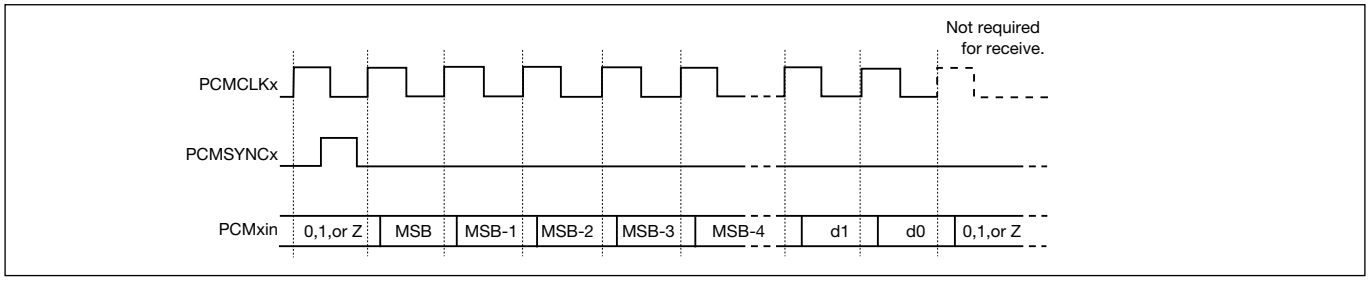


Figure 8. PCM interface receive timing diagram.

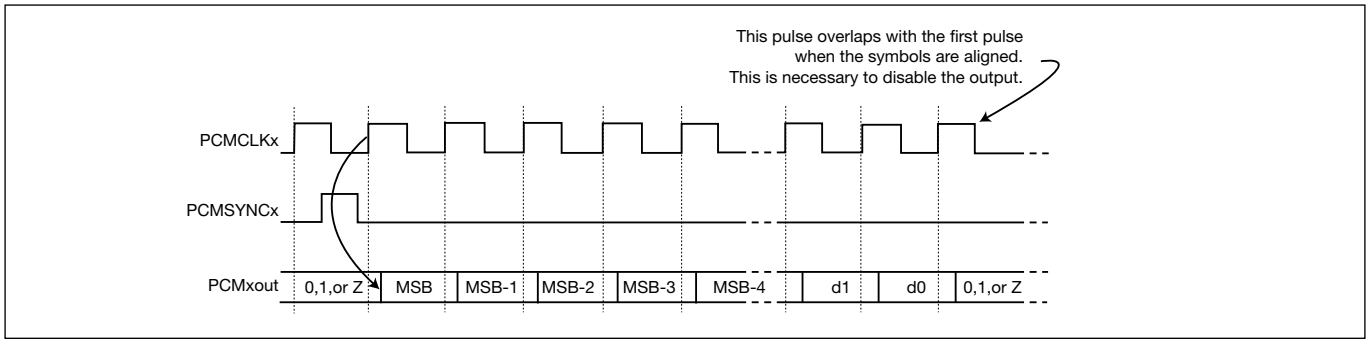


Figure 9. PCM interface transmit timing diagram.

Debug interface

To support development of smaller applications, PBM 990 90 has a JTAG based debug interface. The debug interface opens the possibility to access the processor system via Multi-ICE™ using a debug environment such as the ADS 1.1™ from ARM Ltd.

ARM7 TDMI processor

This system is based around an ARM7 TDMI microprocessor. The ARM, together with ROM, RAM, System controller, External Bus Interface and an external Flash forms the processor system, which executes the Bluetooth firmware. The system offers some flexibility in terms of system performance, power management and scalability. The configuration of PBM 990 90 is done by writing to memory mapped registers.

System controller & Miscellaneous control

These functions handle all system configuration and power management. They configure the built-in PLL, deactivate blocks that are not used, adjust the system frequency to match the performance needed for the application, etc. This flexibility is important for power management.
Figure 10 below illustrates how the clock generation is built up from the input clock.

PLL feedback divider

This block controls the feedback divider for the Phase Locked Loop. In combining an input clock, the PLL and the programmable divider, PBM 990 90 is able to operate with a wide variety of input clock frequencies. The aim is that a designer will be able to re-use an existing system clock and is not constrained by frequency requirements, thus reducing the need for additional discrete components (such as an oscillator). The following formula can be used to derive the input frequencies that can be supported by PBM 990 90:

$1 \le m \le 31;\ 80 \le n \le 137;\ p = 0, 1, 2$

$$\frac{f_{XIN}}{m}\left(n - \frac{p}{3}\right) = 96\ \text{MHz}$$

Writing to a memory mapped register sets the value of n, p, and m.

System clock X/Y divider

The System clock defines the speed for the ARM processor. It is important to have enough capacity when using USB or the UART at 921 kb/s. The frequency can be changed from HCI level by writing to a memory mapped register to change the value of the divider parameters (SYSCLKXDIV, SYSCLKYDIV), which have the following relation:

$$SYSCLK = CLKMAIN\left(\frac{SYSCLKXDIV}{SYSCLKYDIV}\right)$$

Note: X and Y can be set to values between 1 and 255. The X-value must be less than or equal to the Y-value.

UART clock X/Y divider

The frequency of the UART clock depends on what bit rate is required. For 921.6 kbit/s a frequency of 14.7456 MHz is required. The relation between UARTCLK and CLKMAIN is programmed by setting the X/Y divider parameter values (UARTXDIV, UARTYDIV) according to the expression below:

$$CLKBAUD = CLKMAIN\left(\frac{UARTXDIV}{UARTYDIV}\right)$$

Note: X and Y can be set to values between 1 and 255. The X-value must be less than or equal to the Y-value.

Bluetooth clock, CLK4M, X/Y divider

The Bluetooth part of the chip, EBC, needs a 4 MHz clock frequency. This clock has to be trimmed using the X/Y divider to suit the frequency available as SYSCLK. It is important to notice that CLK4M is a function of SYSCLK and therefore a function of SYSCLK X and Y parameter values.

$$CLK4M = SYSCLK\left(\frac{CLK4MXDIV}{CLK4MYDIV}\right)$$

$$CLK4M = CLKMAIN\left(\frac{SYSCLKXDIV}{SYSCLKYDIV}\right)\left(\frac{CLK4MXDIV}{CLK4MYDIV}\right)$$

Note: X and Y can be set to values between 1 and 255. The X-value must be less than or equal to the Y-value.

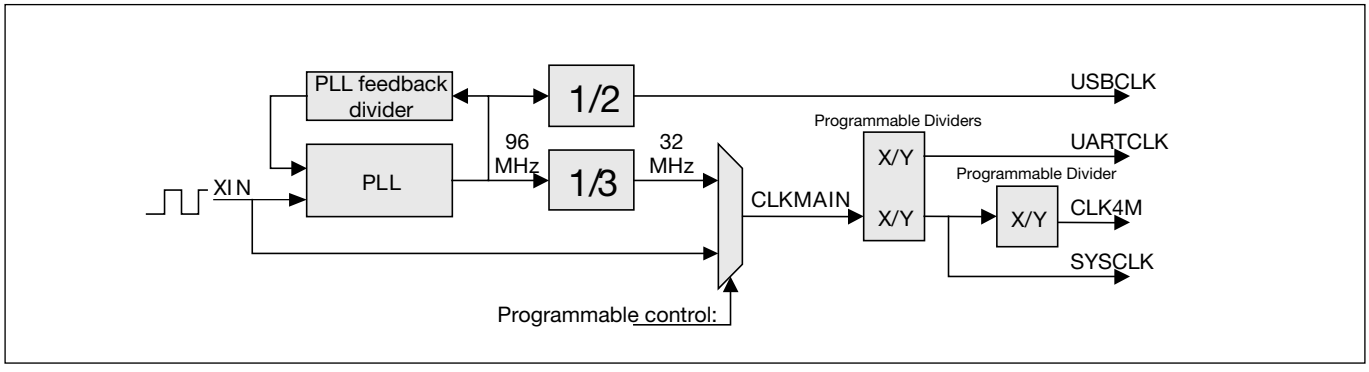


Figure 10. Clock generation.

Low power operation (LPO) clock support

This function is essential for the wake up function. When the radio link is unused, the circuit will go in to a power saving mode inactivating all other blocks including the PLL. At this time the LPO clock and a small number of gates are the only active logic in the circuit. The LPO associated logic activates the processor periodically for page- and inquiry-scan.
The LPO clock input, LPOXIN requires an external 3.2 or 32 or 32.768 kHz square wave.

USB Vterm & EBC wakeup support

These functions are shared on the same USBVT_EBCWAKUP pin and are selected by a memory mapped register. Only one of the functions can be used for a given system configuration.

USBVT functionality:

The default state after reset is a USB Vterm output pin. The USB Vterm output is used to either connect or disconnect an external 1.5 kΩ termination resistor between USB_DP and VDDIO2 (3.3 V in this case). A connect indicates that a high speed USB unit is attached to the USB line. A disconnect indicates that the USB unit is detached from the line. The default state after reset is disconnect, i.e. USBVT is tri-stated.

EBCWAKUP functionality:

The alternative function is an active high EBC wakeup input pin. This can be used by an external unit to order the EBC to start a Bluetooth scan procedure.

System wakeup in low power operation

NSYSWAKUP is an active low unconditional system wakeup input pin. It has to be connected to VDDIO4 if this functionality is not to be used.

Software

The Bluetooth link is partitioned into a hardware part and a software part. The software relates to the Bluetooth protocol stack. Depending on the level of integration, there will be two different firmware models available, including hardware specific drivers for the Bluetooth core, USB, UARTs, GPIO and I^2C. The level of integration follows the two scenarios:

- LM & HCI firmware
- Embedded Bluetooth stack firmware

LM & HCI firmware

In this configuration the customer will access the LM through a Host Controller Interface (HCI) protocol distributed over USB or UART. See figure 11.

Embedded Bluetooth stack firmware

This configuration opens up the possibility for the customer to build small applications based on the PBM 990 90 chip, using the ARM processor in PBM 990 90 as the main processor. See figure 12.

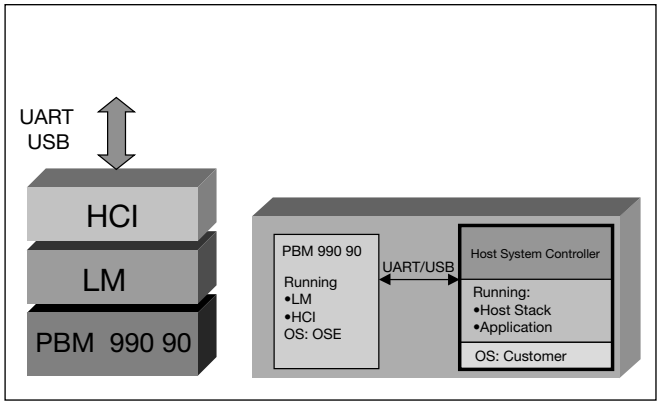


Figure 11. LM & HCI firmware.

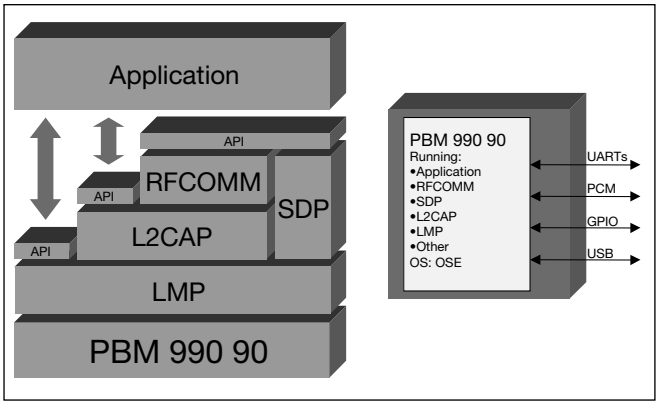


Figure 12. Embedded Bluetooth stack firmware.

Information given in this data sheet is believed to be accurate and reliable. No responsibility is assumed for the consequences of its use nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Ericsson Microelectronics. These products are sold only according to Ericsson Microelectronics' general conditions of sale, unless otherwise confirmed in writing. Specifications subject to change without notice.

Ericsson Microelectronics
SE-164 81 Kista, Sweden
+46 8 757 50 00
www.ericsson.com/microelectronics

For local sales contacts, please refer to our website
or call: Int + 46 8 757 47 00, Fax: +46 8 757 47 76

Preliminary Data Sheet

EN/LZT 146 128 R1A
© Ericsson Microelectronics AB, December 2001