

Description

BL7432SM is an IC for Chip Card made by 0.35um CMOS EEPROM process. It has 256 bytes EEPROM with write protect function .It can be operated at low voltage. With its contact configuration in accordance to ISO standard 7816.BL7432SM can be widely used in different types of IC memory cards.

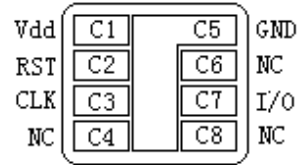


Figure 1

Features

- 256 x 8 bit EEPROM organization
- Byte-wise addressing
- Irreversible byte-wise write protection of lowest 32 addresses (Byte 031)
- 32 x1 bit organization of protection memory
- Two-wire link protocol
- End of processing indicated at data output
- Answer-to-Reset according to ISO standard 7816-3
- Programming time 2.5 ms per byte for both erasing and writing
- Minimum of 100,000 write/erase cycles
- Data retention time :>10 years
- Contacts configuration and serial interface according to ISO 7816 standard (synchronous transmission)

Pin Description

Pin No.	Parameter	Symbol	Function Description
1	C1	V _{dd}	Supply Voltage
2	C2	RST	Reset signal
3	C3	CLK	Clock input
4	C4	N.C.	Not connected
5	C5	GND	Ground
6	C6	NC	Not connected
7	C7	I/O	Bidirectional data line (open drain)
8	C8	NC	Not connected

Function Description

- Block Diagram

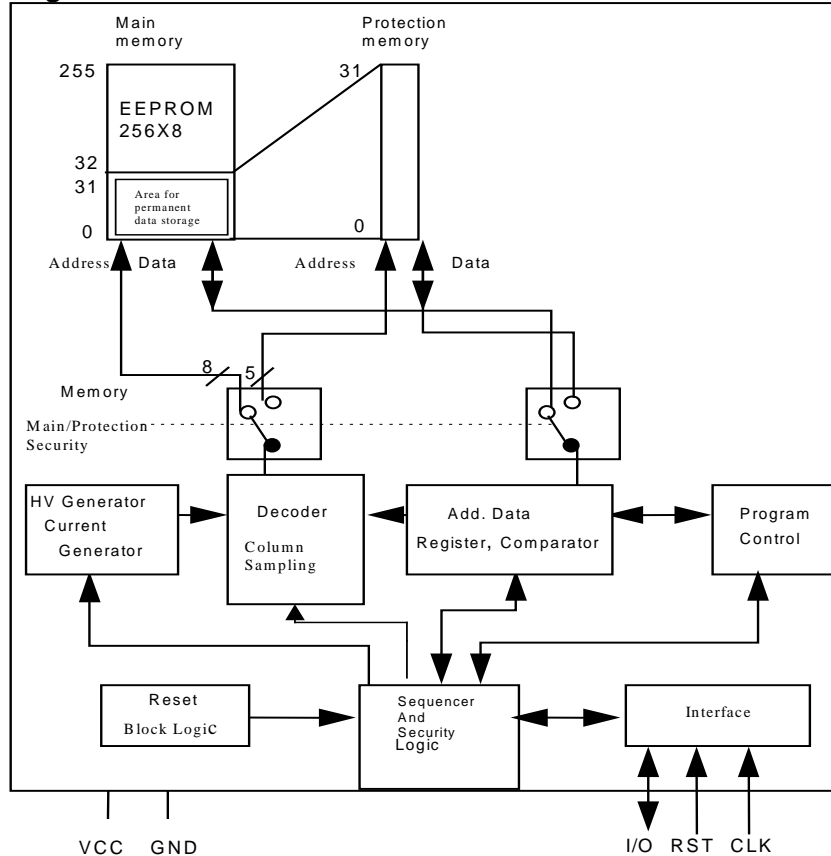


Figure 2

The BL7432SM consists of 256 x 8 bit EEPROM main memory (figure 2) and a 32-bit protection-memory with PROM functionality. The main memory is erased and written byte by byte. When erased, all 8 bits of a data byte are set to logical one. When written, the information in the individual EEPROM cells is to the input data, altered bit by bit to logical zeros (logical AND between the old and the new data in the EEPROM).

Normally a data change consists of an erase and write procedure. It depends on the contents of the data byte in the main memory and the new data byte whether the EEPROM is really erased and/or written. If none of the 8 bits in the addressed byte requires a zero-to-one transition the erase access will be suppressed. Vice versa the write access will be suppressed if no one-to-zero transition is necessary. The write and the erase operation takes at least 2.5 ms each. The first 32 bytes can be irreversibly protected against data change by writing the corresponding bit in the protection memory. Each data byte in this address range is assigned to one bit of the protection memory and has the same address as the data byte in the main memory which it is assigned to. Once written the protection bit cannot be erased.

- Transmission Protocol

The transmission protocol is a two wire link protocol between the interface device IFD and the integrated circuit IC. It is identical to the protocol type "S=10". All data changes on I/O are initiated by the falling edge on CLK.

The transmission protocol consists of the 4 modes:

- 1) Reset and Answer-to-Reset
- 2) Command Mode
- 3) Outgoing Data Mode
- 4) Processing Mode

(1) Reset and Answer-to-Reset

Answer-to-Reset takes place according to ISO standard 7816-3. The reset can be given at any time during operation. In the beginning, the address counter is set to zero together with a clock pulse and the first data bit (LSB) is output to I/O when RST is set from state H to state L. Under a continuous input of additional 31 clock pulses the contents of the first 4 EEPROM addresses can be read out. The 33rd clock pulse switches I/O to state H (figure 3). During Answer-to-Reset any start and stop condition is ignored.

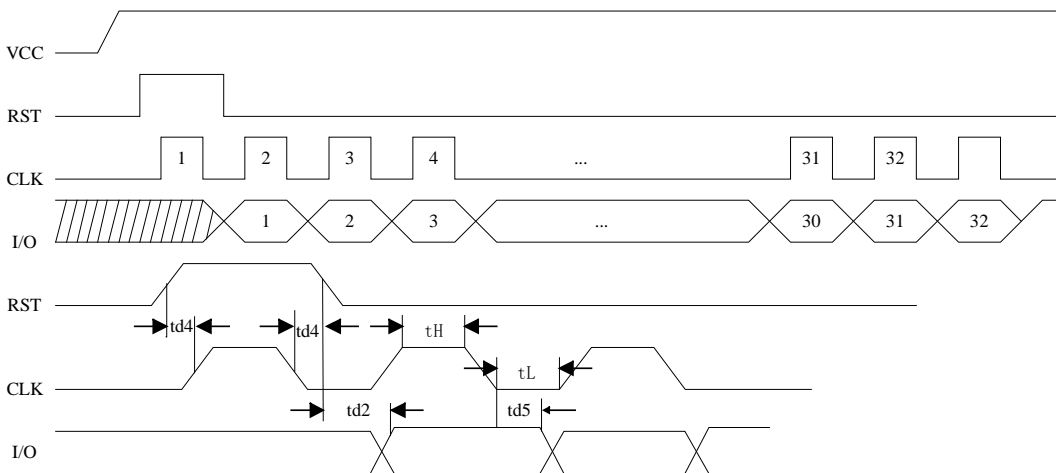


Figure 3 Reset and Answer-to-Reset

(2) Command Mode

After the Answer-to-Reset the chip waits for a command. Every command begins with a start condition, includes a 3 bytes long command entry followed by an additional clock pulse and ends with a stop condition (figure 4).

- Start condition: Falling edge on I/O during CLK in state H
- Stop condition: Rising edge on I/O during CLK in state H

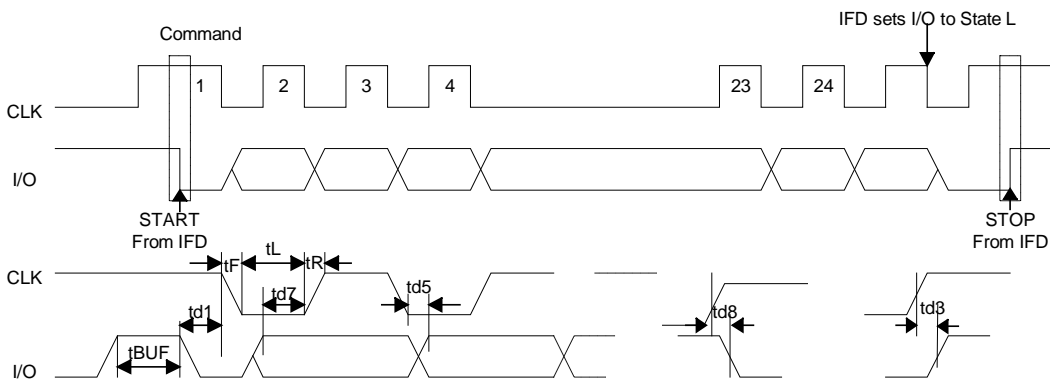


Figure 4 Command Mode

After the reception of a command there are two possible modes:

- Outgoing data mode for reading
- Processing mode for writing and erasing

(3) Outgoing Data Mode

In this mode the IC sends data to the IFD. Figure 5 shows the timing diagram. The first bit becomes valid on I/O after the first falling edge on CLK. After the last data bit an additional clock pulse is necessary in order to set I/O to state H and to prepare the IC for a new command entry. During this mode any start and stop condition is discarded.

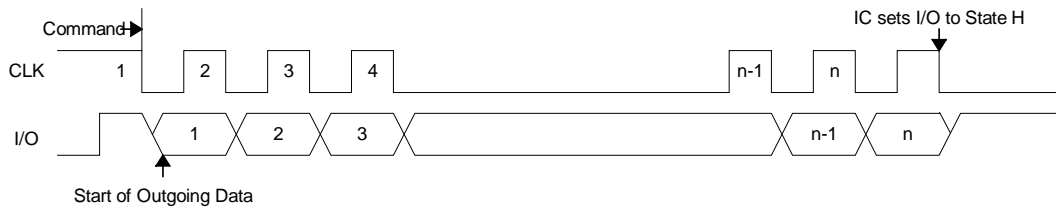


Figure 5 Outgoing Data Mode

(4) Processing Mode

In this mode the IC processes internally. Figure 6 shows the timing diagram. The IC has to be clocked continuously until I/O which was switched to state L after the first falling edge of CLK is set to state H. Any start and stop condition is discarded during this mode.

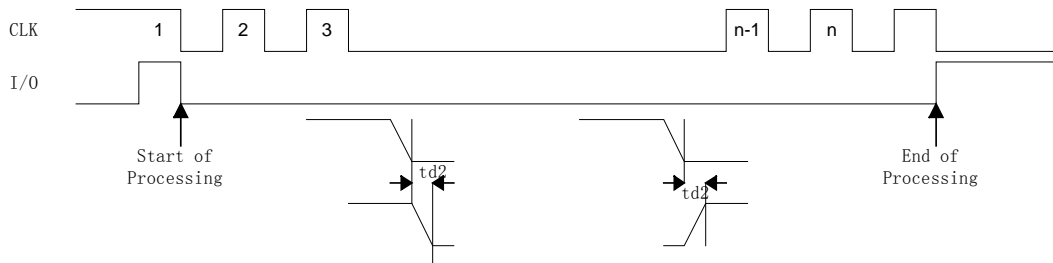


Figure 6 Processing Mode

• Commands

(1) Command Format

Each command consists of three byte:

MSB	Control	LSB	MSB	Address	LSB	MSB	Data	LSB															
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Beginning with the control byte LSB is transmitted first.

Byte 1 Control	Byte 2 Address	Byte 3 Data	Operation	Mode
B7 B6 B5 B4 B3 B2 B1 B0	A7-A0	D7-D0		
0 0 1 1 0 0 0 0	Address	No effect	Read Main Memory	Outgoing data
0 0 1 1 1 0 0 0	Address	Input data	Update Main Memory	Processing
0 0 1 1 0 1 0 0	No effect	No effect	Read Protection Memory	Outgoing Data
0 0 1 1 1 1 0 0	Address	Input data	Write Protection Memory	Processing

(2) Description of Command

Read Main Memory

The command reads out the contents of the main memory(with LSB first)starting at the given byte address(N) UP TO THE END MEMORY. After the command entry the IFD has to supply sufficient clock pulses. The number of clocks is $m=(256-N)*8+1$.The read access to the main memory is always possible.

Read Protection Memory

The command transfers the protection bits under a continuous input of 32 clock pulses to the output. I/O is switched to state H by an additional pulse. The protection memory can always be read.

Update Main Memory

The command programs the address EEPROM byte with the data byte transmitted. Depending on the old and new data, one of the following sequences will take place during the processing mode:

- erase and write (5.0ms) corresponding to $m = 255$ clock pulses
 - write without erase (2.5ms) corresponding to $m = 124$ clock pulses
 - erase without write (2.5ms) corresponding to $m = 124$ clock pulses
- (all values at 50 kHz clock rate)

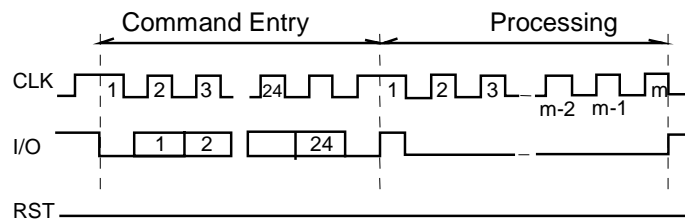


Figure 7 Update Main Memory

Write Protection Memory

The execution of this command contains a comparison of the entered data byte with the assigned byte in the EEPROM .In case of identity the protection bit is written thus making the data information unchangeable. If the data comparison results in data differences writing of the protection bit will be suppressed. Execution times and required clock pulses see Update Main Memory.

• **Reset Modes**

(1) Power-on-Reset

After connecting the operating voltage to VCC ,I/O is state H. By all means, a read access to an address or an Answer-to-Reset must be carried out before data can be altered.

(2) Break

If RST is set to high during CLK in state L any operation is aborted and I/O is switched to state H. Minimum duration of $t_{res}=5\mu s$ is necessary to trigger a defined valid reset(figure 9).After Break the chip is ready for further operations.

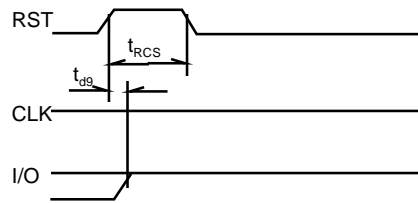


Figure 9 Break

• **Failures**

Behavior in case of failures:

In case of one of the following failures, the chip sets the I/O to state H after 8 clock pulses at the latest.

Possible failures:

- Comparison unsuccessful
- Wrong command
- Wrong number of command clock pulses
- Write/erase access to already protected bytes
- Rewriting and erasing of a bit in the protection memory

• **Coding of the Chip**

Due to security purposes every chip is irreversibly coded by a scheme. By this way fraud and misuse is excluded. As an example, figures 10 and 11 show ATR and Directory Data of structure 1. When delivered, ATR header, ICM and ICT are programmed. Depending on the agreement between the customer and Shanghai Belling CO. LTD. ICCF, the chip type and other content can be also programmed before delivery.

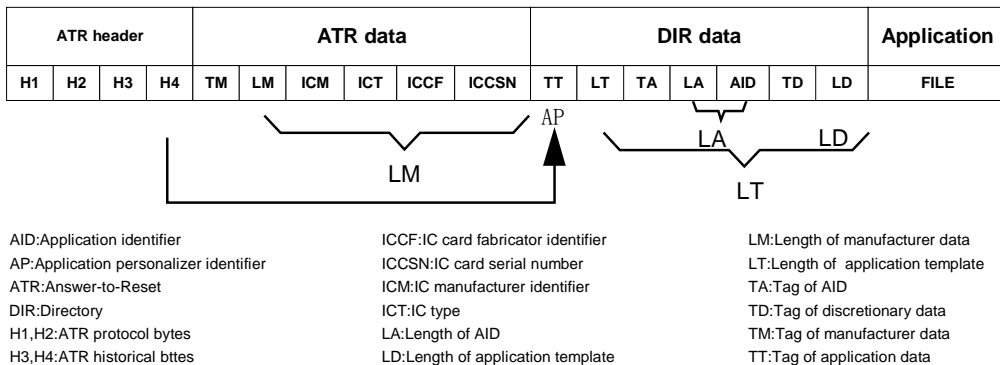


Figure 10 Synchronous Transmission ATR and Directory Data of Structure1

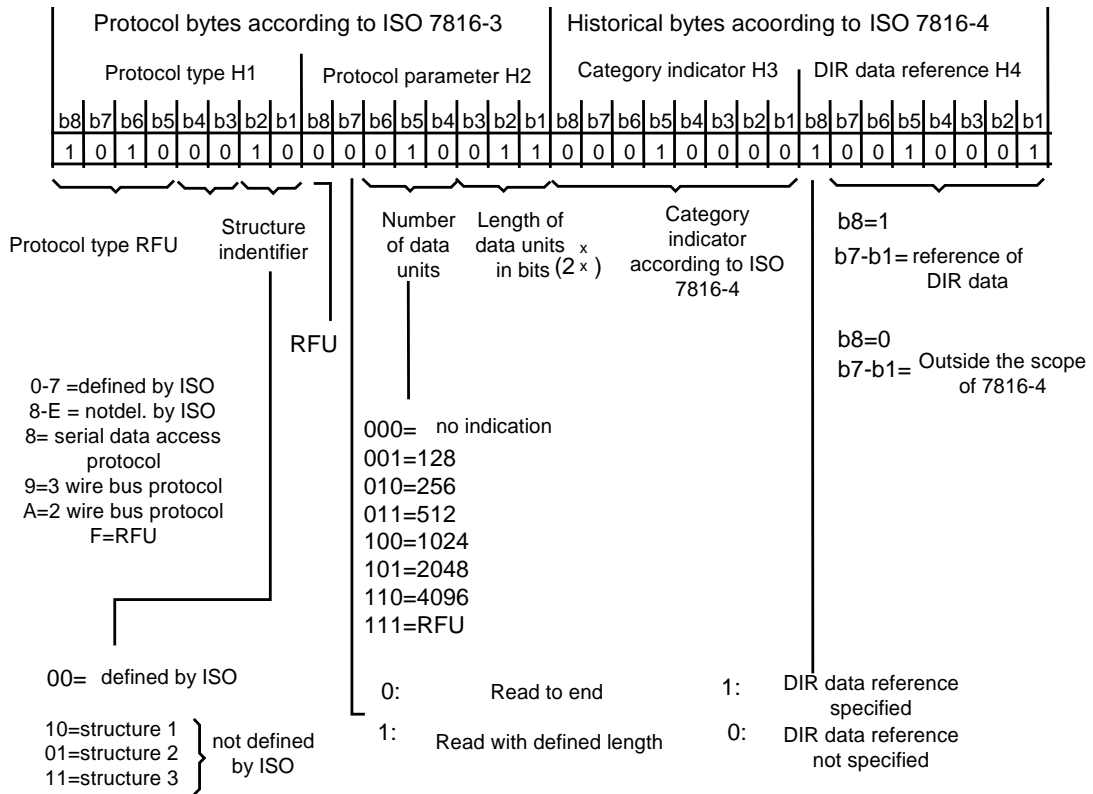


Figure 11 Answer-to-Reset for Synchronous Transmission Coding of Structure

Chip and Package

Electrical Parameter
• Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	Max		
Supply voltage	V_{CC}	-0.3		6.0	V	
Input voltage (any pin)	V_I	-0.3		6.0	V	
Storage temperature	T_S	-40		125	°C	
Power consumption	PT	-		70	mw	
Operation temperature		-35		70	°C	

• DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	Max		
Supply voltage	V_{CC}	3.0	5.0	5.5	V	
Supply current	I_{CC}		3	10	mA	
High-level input voltage (I/O,CLK,RST)	V_{IH}	$V_{CC}-1$	-	$V_{CC}+0.3$	V	
Low-level input voltage (I/O,CLK,RST)	V_{IL}	$V_{GND}-0.2$	-	$V_{GND}+0.8$	V	
High-level input current (I/O,CLK,RST)	I_H	-	-	50	μA	
Low-level output current (I/O)	I_{OL}	1	-	-	mA	$V_{OL}=0.4V$, open drain
High-level leakage current (I/O)	I_{OH}	-	-	50	A	$V_{OH}=V_{CC}$, open drain
Input capacitance	C_I	-	-	10	pF	

• AC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	Max		
Clock frequency	CLK	7		50		
Clock high period	t_H	9			μs	
Clock low period	t_L	9			μs	
Rise time	t_R			1	μs	
Fall time	t_F			1	μs	
Hold time start condition	t_{d1}	4			μs	
Delay time	t_{d2}			2.5	μs	
Setup time for stop condition	t_{d3}	4			μs	
Setup time	t_{d4}	4			μs	
Hold time data	t_{d5}	1			μs	
Answer to reset	t_{d6}	20			μs	
Setup time data	t_{d7}	1			μs	
Setup time for start condition	t_{d78}	4			μs	
Reset	t_{RES}	5			μs	
Delay time	t_{dg}	2.5			μs	
Eraser time	T_{ER}	2.5*			ms	
Write time	t_{WR}	2.5*			ms	
Time before new start condition	T_{BUF}	10			μs	

*f =50 kHz