

LOW VOLTAGE CMOS HEX D-TYPE FLIP-FLOP WITH CLEAR WITH 5V TOLERANT INPUTS

- HIGH SPEED:
 $f_{MAX} = 180\text{MHz (TYP.) at } V_{CC} = 3.3\text{V}$
- 5V TOLERANT INPUTS
- INPUT VOLTAGE LEVEL:
 $V_{IL}=0.8\text{V, } V_{IH}=2\text{V at } V_{CC}=3\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A=25^\circ\text{C}$
- LOW NOISE:
 $V_{OLP} = 0.3\text{V (TYP.) at } V_{CC} = 3.3\text{V}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2\text{V to } 3.6\text{V (1.2V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 174
- IMPROVED LATCH-UP IMMUNITY
- POWER DOWN PROTECTION ON INPUTS

DESCRIPTION

The 74LVX174 is a low voltage CMOS HEX D-TYPE FLIP FLOP WITH CLEAR NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.



Table 1: Order Codes

| PACKAGE | T & R |
|---------|-------------|
| SOP | 74LVX174MTR |
| TSSOP | 74LVX174TTR |

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the CLEAR input is held low, the Q outputs are held low independently of the other inputs.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

This device can be used to interface 5V to 3V system. It combines high speed performance with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

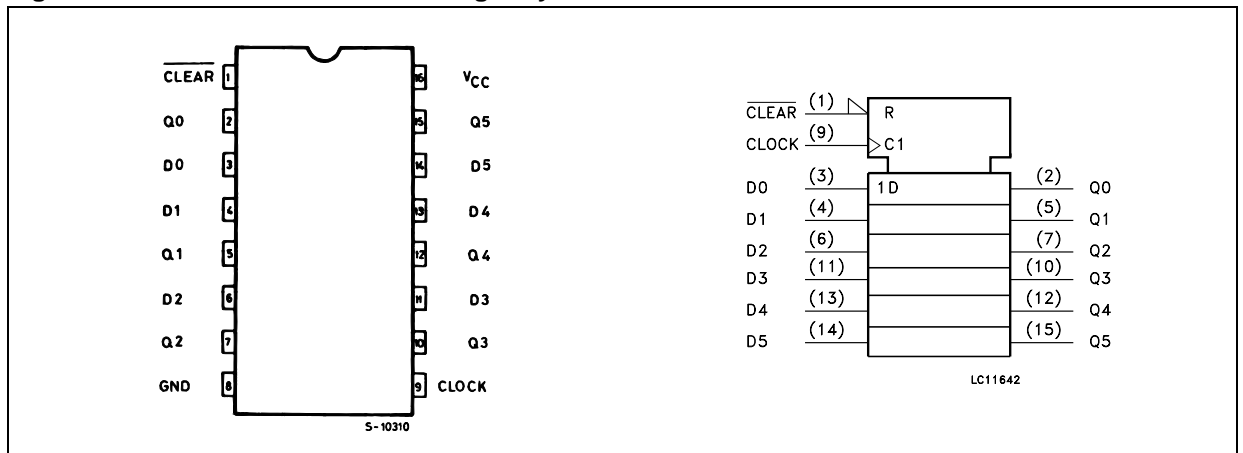


Figure 2: Input Equivalent Circuit

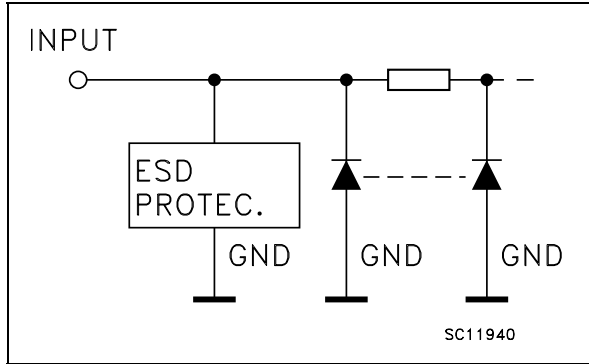


Table 2: Pin Description

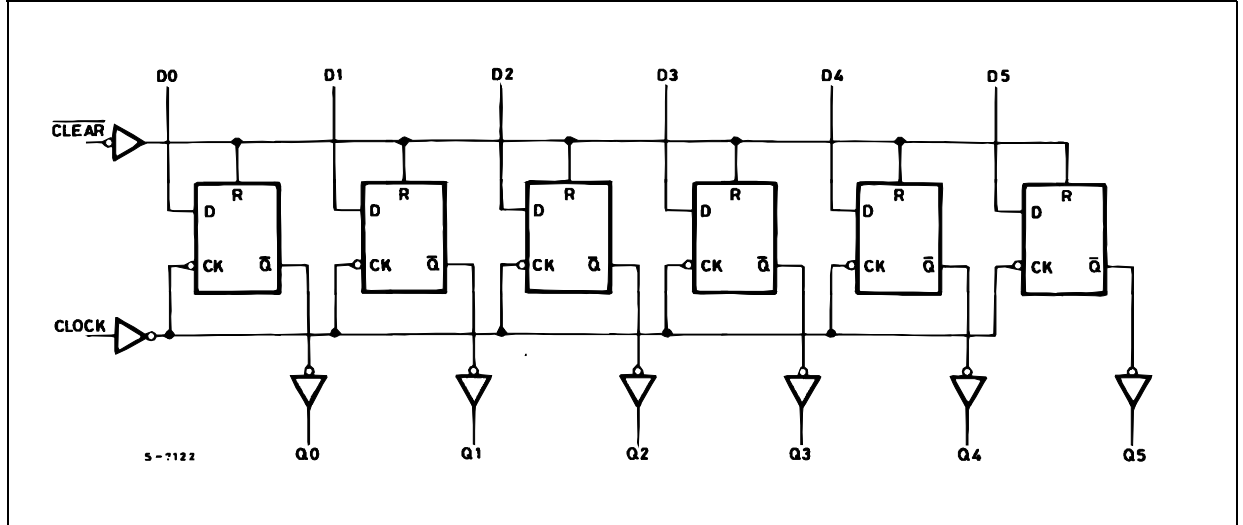
| PIN N° | SYMBOL | NAME AND FUNCTION |
|---------------------|-----------------|---|
| 1 | CLEAR | Asynchronous Master Reset (Active LOW) |
| 2, 5, 7, 10, 12, 15 | Q0 to Q5 | Flip-Flop Outputs |
| 3, 4, 6, 11, 13, 14 | D0 to D5 | Data Inputs |
| 9 | CLOCK | Clock Input (LOW-to-HIGH, Edge Triggered) |
| 8 | GND | Ground (0V) |
| 16 | V _{CC} | Positive Supply Voltage |

Table 3: Truth Table

| INPUTS | | | OUTPUTS | FUNCTION |
|---------------------------|---|-------|----------------|-----------|
| $\overline{\text{CLEAR}}$ | D | CLOCK | Q | |
| L | X | X | L | CLEAR |
| H | L | | L | |
| H | H | | H | |
| H | X | | Q _n | NO CHANGE |

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 4: Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-----------------------|-------------------------------|------------------------|------|
| V_{CC} | Supply Voltage | -0.5 to +7.0 | V |
| V_I | DC Input Voltage | -0.5 to +7.0 | V |
| V_O | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | - 20 | mA |
| I_{OK} | DC Output Diode Current | ± 20 | mA |
| I_O | DC Output Current | ± 25 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current | ± 50 | mA |
| T_{stg} | Storage Temperature | -65 to +150 | °C |
| T_L | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5: Recommended Operating Conditions

| Symbol | Parameter | Value | Unit |
|----------|---|---------------|------|
| V_{CC} | Supply Voltage (note 1) | 2 to 3.6 | V |
| V_I | Input Voltage | 0 to 5.5 | V |
| V_O | Output Voltage | 0 to V_{CC} | V |
| T_{op} | Operating Temperature | -55 to 125 | °C |
| dt/dv | Input Rise and Fall Time (note 2) ($V_{CC} = 3.3V$) | 0 to 100 | ns/V |

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2.0V

Table 6: DC Specifications

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|----------|---------------------------|----------------|-----------------------|--------------------|------|-----------|-------------|---------|--------------|---------|---------|
| | | | | $T_A = 25^\circ C$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V_{IH} | High Level Input Voltage | V_{CC} | | 1.5 | | | 1.5 | | 1.5 | | V |
| | | 3.0 | | 2.0 | | | 2.0 | | 2.0 | | |
| | | 3.6 | | 2.4 | | | 2.4 | | 2.4 | | |
| V_{IL} | Low Level Input Voltage | V_{CC} | | | | 0.5 | | 0.5 | | 0.5 | V |
| | | 3.0 | | | | 0.8 | | 0.8 | | 0.8 | |
| | | 3.6 | | | | 0.8 | | 0.8 | | 0.8 | |
| V_{OH} | High Level Output Voltage | V_{CC} | $I_O = -50 \mu A$ | 1.9 | 2.0 | | 1.9 | | 1.9 | | V |
| | | 3.0 | $I_O = -50 \mu A$ | 2.9 | 3.0 | | 2.9 | | 2.9 | | |
| | | 3.0 | $I_O = -4 mA$ | 2.58 | | | 2.48 | | 2.4 | | |
| V_{OL} | Low Level Output Voltage | V_{CC} | $I_O = 50 \mu A$ | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | 3.0 | $I_O = 50 \mu A$ | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 3.0 | $I_O = 4 mA$ | | | 0.36 | | 0.44 | | 0.55 | |
| I_I | Input Leakage Current | 3.6 | $V_I = 5V$ or GND | | | ± 0.1 | | ± 1 | | ± 1 | μA |
| I_{CC} | Quiescent Supply Current | 3.6 | $V_I = V_{CC}$ or GND | | | 4 | | 40 | | 40 | μA |

Table 7: Dynamic Switching Characteristics

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|------------------|--|------------------------|------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | C _L (pF) | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V _{OLP} | Dynamic Low Voltage Quiet Output (note 1, 2) | 3.3 | C _L = 50 pF | | 0.3 | 0.8 | | | | | V |
| V _{OLV} | | | | -0.8 | -0.3 | | | | | | |
| V _{IHD} | Dynamic High Voltage Input (note 1, 3) | 3.3 | | 2 | | | | | | | |
| V _{ILD} | Dynamic Low Voltage Input (note 1, 3) | 3.3 | | | | 0.8 | | | | | |

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Table 8: AC Electrical Characteristics (Input t_r = t_f = 3ns)

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|--|--|------------------------|------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | C _L (pF) | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| t _{PLH} t _{PHL} | Propagation Delay Time CLOCK to Q | 2.7 | 15 | | 7.6 | 14.5 | 1.0 | 17.5 | 1.0 | 18.5 | ns |
| | | 2.7 | 50 | | 10.1 | 18.0 | 1.0 | 21.0 | 1.0 | 22.0 | |
| | | 3.3 ^(*) | 15 | | 5.9 | 9.3 | 1.0 | 11.0 | 1.0 | 12.0 | |
| | | 3.3 ^(*) | 50 | | 8.4 | 12.8 | 1.0 | 14.5 | 1.0 | 15.5 | |
| t _{PLH} t _{PHL} | Propagation Delay Time CLEAR to Q | 2.7 | 15 | | 7.9 | 15.0 | 1.0 | 18.5 | 1.0 | 19.5 | ns |
| | | 2.7 | 50 | | 10.4 | 18.5 | 1.0 | 22.0 | 1.0 | 23.0 | |
| | | 3.3 ^(*) | 15 | | 6.2 | 9.7 | 1.0 | 11.5 | 1.0 | 12.5 | |
| | | 3.3 ^(*) | 50 | | 8.7 | 13.2 | 1.0 | 15.0 | 1.0 | 16.0 | |
| t _{WL} | CLEAR pulse Width, HIGH | 2.7 | | | 6.5 | | | 7.5 | | 7.5 | ns |
| | | 3.3 ^(*) | | | 5.0 | | | 5.0 | | 5.0 | |
| t _W | CLOCK pulse Width | 2.7 | | | 6.5 | | | 7.5 | | 7.5 | ns |
| | | 3.3 ^(*) | | | 5.0 | | | 5.0 | | 5.0 | |
| t _S | Setup Time Q to CLOCK HIGH or LOW | 2.7 | | | 7.5 | | | 8.5 | | 8.5 | ns |
| | | 3.3 ^(*) | | | 5.0 | | | 6.0 | | 6.0 | |
| t _h | Hold Time Q to CLOCK HIGH or LOW | 2.7 | | | 0.0 | | | 0.0 | | 0.0 | ns |
| | | 3.3 ^(*) | | | 0.0 | | | 0.0 | | 0.0 | |
| t _{REM} | Recovery Time CLEAR to Q | 2.7 | | | 4.5 | | | 4.5 | | | ns |
| | | 3.3 ^(*) | | | 3.0 | | | 3.0 | | | |
| f _{MAX} | Maximum Clock Frequency | 2.7 | 15 | | 65 | 130 | | 55 | | | MHz |
| | | 2.7 | 50 | | 45 | 60 | | 40 | | | |
| | | 3.3 ^(*) | 15 | | 115 | 180 | | 95 | | | |
| | | 3.3 ^(*) | 50 | | 65 | 95 | | 55 | | | |
| t _{OSLH} t _{OSHL} | Output To Output Skew Time (note 1, 2) | 2.7 | 50 | | 0.5 | 1.0 | | 1.5 | | 1.5 | ns |
| | | 3.3 ^(*) | 50 | | 0.5 | 1.0 | | 1.5 | | 1.5 | |

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

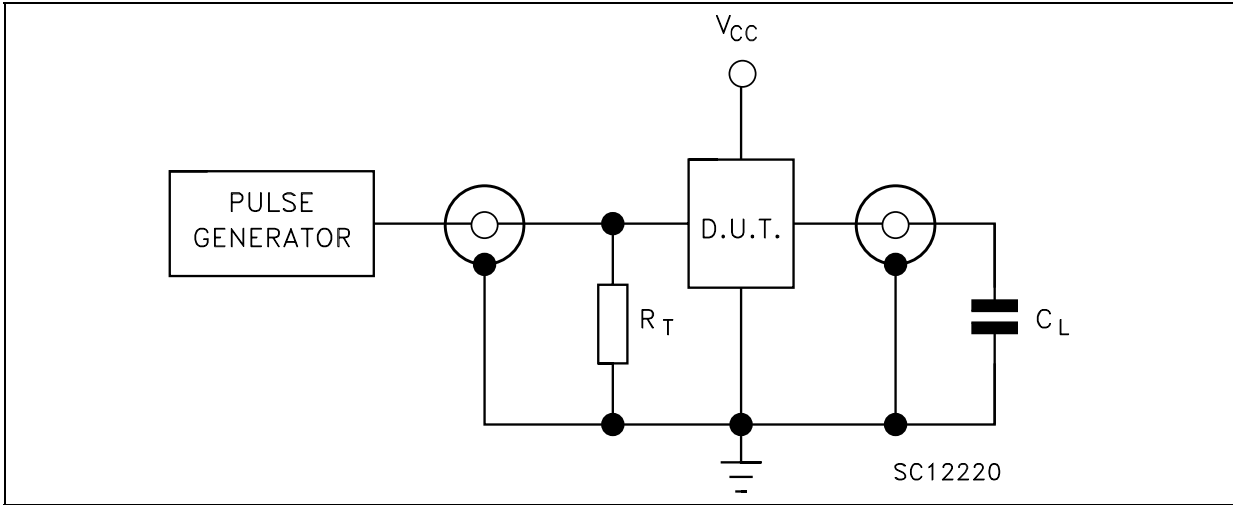
2) Parameter guaranteed by design (*) Voltage range is 3.3V ± 0.3V

Table 9: Capacitive Characteristics

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|-----------------|--|---------------------|-------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| C _{IN} | Input Capacitance | 3.3 | | | 5 | | | 10 | | 10 | pF |
| C _{PD} | Power Dissipation Capacitance (note 1) | 3.3 | f _{IN} = 10MHz | | 23 | | | | | | pF |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(OPR)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/n (per circuit)

Figure 4: Test Circuit



C_L = 15/50pF or equivalent (includes jig and probe capacitance)
 R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 5: Waveform - Propagation Delays (f=1MHz; 50% duty cycle)

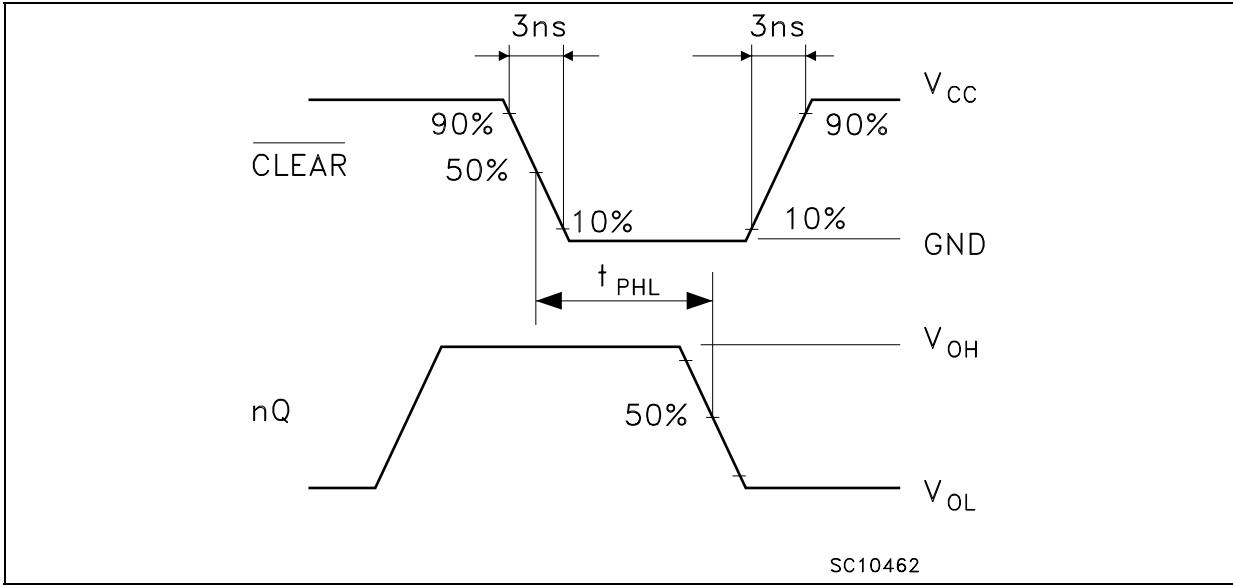


Figure 6: Waveform - Propagation Delays, Setup And Hold Times (f=1MHz; 50% duty cycle)

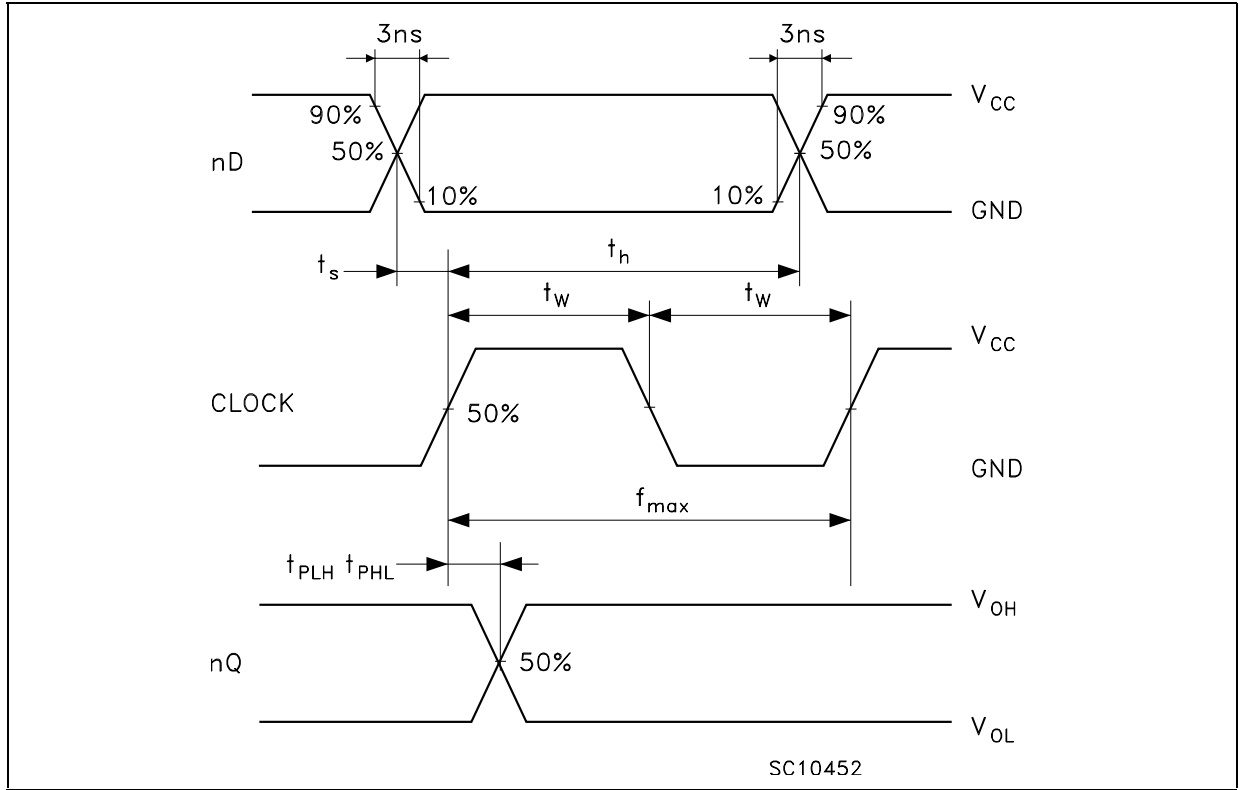
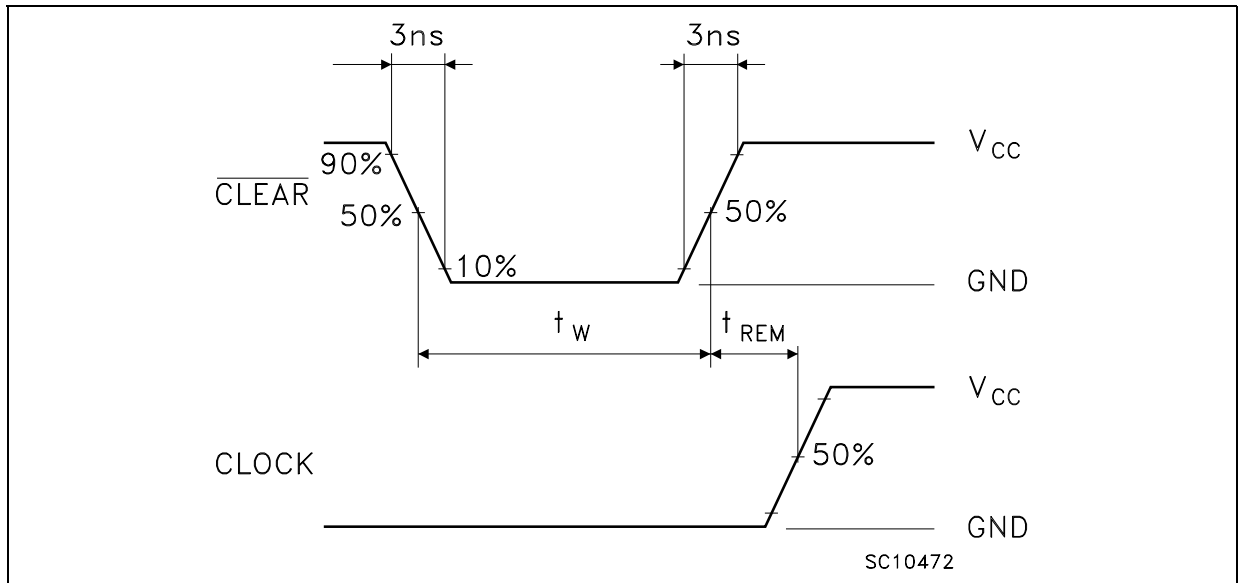
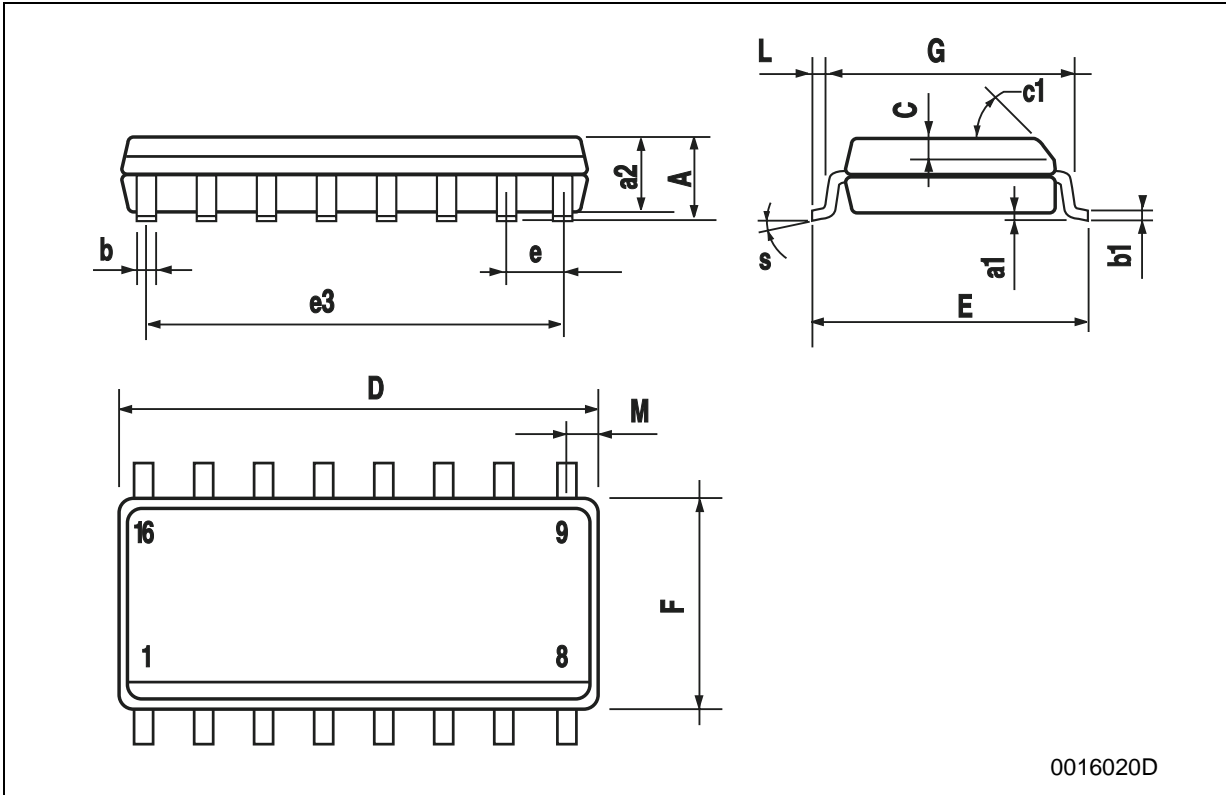


Figure 7: Waveform - Recovery Time, Minimum Pulse Width (f=1MHz; 50% duty cycle)



SO-16 MECHANICAL DATA

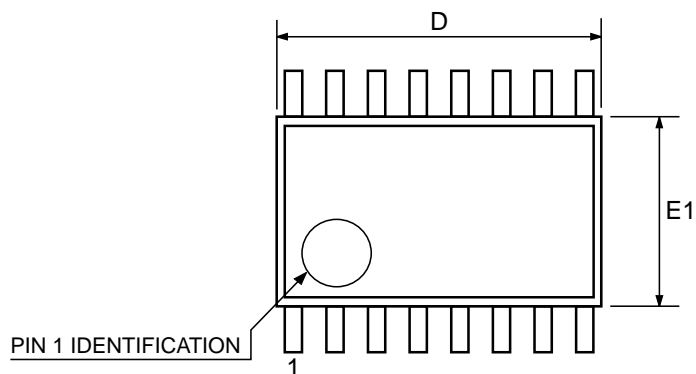
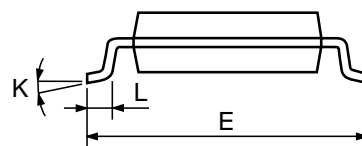
| DIM. | mm. | | | inch | | |
|------|------------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.64 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 9.8 | | 10 | 0.385 | | 0.393 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8° (max.) | | | | | |



0016020D

TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|----------|------|-------|------------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0079 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



0080338D

Tape & Reel SO-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.45 | | 6.65 | 0.254 | | 0.262 |
| Bo | 10.3 | | 10.5 | 0.406 | | 0.414 |
| Ko | 2.1 | | 2.3 | 0.082 | | 0.090 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



Tape & Reel TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.7 | | 6.9 | 0.264 | | 0.272 |
| Bo | 5.3 | | 5.5 | 0.209 | | 0.217 |
| Ko | 1.6 | | 1.8 | 0.063 | | 0.071 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



Table 10: Revision History

| Date | Revision | Description of Changes |
|-------------|----------|-----------------------------------|
| 27-Aug-2004 | 3 | Ordering Codes Revision - pag. 1. |

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