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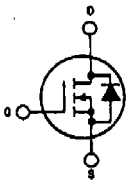
RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 180 V and 200 V
$r_{DS(on)}$: 3.5 Ω and 3.65 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



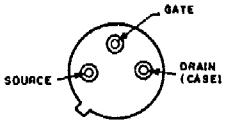
N-CHANNEL ENHANCEMENT MODE

The RFL1N18L and RFL1N20L and the RFP2N18L and RFP2N20L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

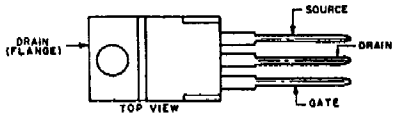
TERMINAL DESIGNATIONS

RFL1N18L
RFL1N20L



JEDEC TO-205AF

RFP2N18L
RFP2N20L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL1N18L	RFL1N20L		RFP2N18L	RFP2N20L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) .... V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D	1	1		2	2	A
Pulsed .... I_{DM}			4			A
POWER DISSIPATION @ T_C=25°C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25°C	0.0667	0.0667		0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS RFL1N18L RFP2N18L MIN.	LIMITS RFL1N18L RFP2N18L MAX.	LIMITS RFL1N20L RFP2N20L MIN.	LIMITS RFL1N20L RFP2N20L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0		180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA		1	2	1	2	V
*Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V		—	1	—	—	μA
		V_{DS}=160 V		—	—	—	1	
		T_C=125° C, V_{DS}=145 V		—	50	—	—	
		V_{DS}=160 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V, V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$*	I_D=1 A, V_{GS}=5 V	RFP	—	3.5	—	3.5	V
			RFL	—	3.65	—	3.65	
		I_D=2 A, V_{GS}=5 V	RFP	—	9	—	9	
			RFL	—	9.3	—	9.3	
Static Drain-Source On Resistance	$r_{DS}(on)$*	I_D=1 A, V_{GS}=5 V	RFP	—	3.5	—	3.5	Ω
			RFL	—	3.65	—	3.65	
Forward Transconductance	g_{fs}*	V_{DS}=10 V, I_D=1 A		800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V, V_{GS}=0 V, f=1MHz		—	200	—	200	pF
Output Capacitance	C_{oss}			—	60	—	60	
Reverse-Transfer Capacitance	C_{rss}			—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V, I_D=1 A, R_{gen}=∞, R_{gs}=6.25 Ω, V_{GS}=5 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r			10(typ)	30	10(typ)	30	
Turn-Off Delay Time	$t_d(off)$			25(typ)	40	25(typ)	40	
Fall Time	t_f		RFP	20(typ)	25	20(typ)	25	
			RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N18L, RFL1N20L		—	15	—	15	°C/W
		RFP2N18L, RFP2N20L		—	5	—	5	

*Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N18L RFP2N18L MIN.	LIMITS RFL1N18L RFP2N18L MAX.	LIMITS RFL1N20L RFP2N20L MIN.	LIMITS RFL1N20L RFP2N20L MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A, di_F/dt=50 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.