THE1008

THE1008 0.8 Micron Embedded Array Series

Description

The THE1008 0.8 Micron Embedded Array is a 2 layer metal HCMOS array product targeted at high performance and high complexity applications. The concept of the embedded array is to allow designers to embed high density custom RAM and ROM blocks into their designs, while maintaining the flexibility and fast turnaround of a standard gate array.

Applications not possible or not economically viable with gate arrays due to RAM or ROM requirements can be realized using THE1008 embedded arrays. 22 masterslices with raw gate counts of between 440 and 573,240 are available. The THE1008 proprietary cell architecture offers a gate delay of 325 picoseconds; the higher density also results in higher chip level performance due to lower parasitic and fanout loadings.

The THE1008 is designed for cost sensitive applications which also demand high circuit performance. The series eliminates the necessity of fighting the time-to-market versus production cost decision, because the THE1008 design philosophy addresses both of these issues.

The THE1008 design kits support most popular design platforms and environments, and allows State-of-the-art design methodology through top-down design techniques.

Features

- ❑ Very high density RAM and ROM structures
- ❑ Up to 145,000 usable gates depending on the sizes of embedded RAM and ROM blocks
- ❑ Up to 472 I/O pads
- ❑ 0.8 micron drawn HCMOS technology (0.65 micron effective)
- ❑ Typical gate delay of 325 ps
- ❑ Power dissipation of < 5 µW/gate/MHz
- ❑ Low noise output buffers with up to 24 mA drive
- ❑ CMOS/TTL level input drivers
- ❑ Extensive macrocell, logic function libraries
- ❑ RAM, ROM and logic compilers
- ❑ ESD protection in accordance with MIL-STDs
- ❑ Latch-up resist

Master	Total Gates	Usable Gates [1]	No. Pads	No. I/Os [2], [3]
THE8001	440	210	32	16
THE8002	2,116	1,000	46	30
THE8005	5,472	2,500	66	50
THE8010	9,858	4,500	80	64
THE8013	13,671	6,200	92	76
THE8018	18,000	8,100	100	84
THE8024	24,360	9,600	116	100
THE8031	31,872	13,000	128	112
THE8040	40,500	16,500	144	128
THE8052	52,521	21,000	160	144
THE8063	63,045	24,000	176	160
THE8077	77,850	27,500	192	176
THE8094	94,786	33,500	208	192
THE8110	109,114	38,500	224	208
THE8140	140,592	50,000	252	236
THE8170	171,487	58,500	276	260
THE8210	215,750	70,000	308	292
THE8260	260,150	78,000	336	320
THE8320	320,860	93,000	368	352
THE8390	393,700	110,000	408	392
THE8450	453,750	118,000	436	420
THE8570	573,240	145,000	488	472

Notes: [1] Usable Gates is an estimation and will vary, depending on design
[2] I/O pads can be used as VDD / VSS pads
[3] Minimum 2 I/O pads must be applied as VDD/VSS for core logic