International
IOR Rectifier

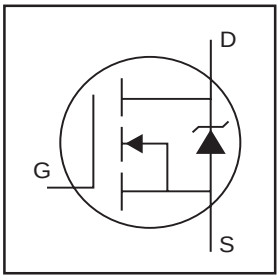
PD-91840

PRELIMINARY

IRL1104S/L

HEXFET® Power MOSFET

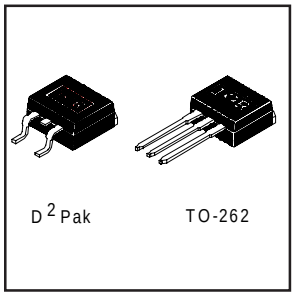
- Logic-Level Gate Drive
- Advanced Process Technology
- Surface Mount (IRL1104S)
- Low-profile through-hole (IRL1104L)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 40V

$R_{DS(on)}$ = 0.008Ω

I_D = 104A⑥



Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRL1104L) is available for low-profile applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑤	104⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑤	74⑥	
I_{DM}	Pulsed Drain Current ①⑤	416	
P_D @T_A = 25°C	Power Dissipation	2.4	W
P_D @T_C = 25°C	Power Dissipation	167	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS}	Single Pulse Avalanche Energy②⑤	340	mJ
I_{AR}	Avalanche Current①	62	A
E_{AR}	Repetitive Avalanche Energy①	17	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient(PCB Mounted,steady-state)**	——	62	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/°C	Reference to 25°C, I_D =1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.008	W	V_{GS} = 10V, I_D = 62A ④
		—	—	0.012		V_{GS} = 4.5V, I_D = 52A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—		V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	53	—	—	S	V_{DS} = 25V, I_D = 62A⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} =40V, V_{GS} = 0V
		—	—	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	68	nC	I_D =62A
Q_{gs}	Gate-to-Source Charge	—	—	24		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	34		V_{GS} = 4.5V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	18	—		V_{DD} = 20V
t_r	Rise Time	—	257	—		I_D =54A
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		R_G = 3.6Ω , V_{GS} = 4.5V
t_f	Fall Time	—	64	—		R_D = 0.4Ω, See Fig. 10 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	3445	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1065	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	270	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	104⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	416		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S =62A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	84	126	ns	T_J = 25°C, I_F =62A
Q_{rr}	Reverse Recovery Charge	—	223	335	nC	di/dt = 100A/µs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 15V, starting T_J = 25°C, L = 0.18mH R_G = 25Ω, I_{AS} = 62A. (See Figure 12)

③ I_{SD} ≤ 62A, di/dt ≤ 217A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRL1104 data and test conditions.

⑥ Calculated continuous current based on maximum allowable junction temperature;for recommended current-handling of the package refer to Design Tip # 93-4

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

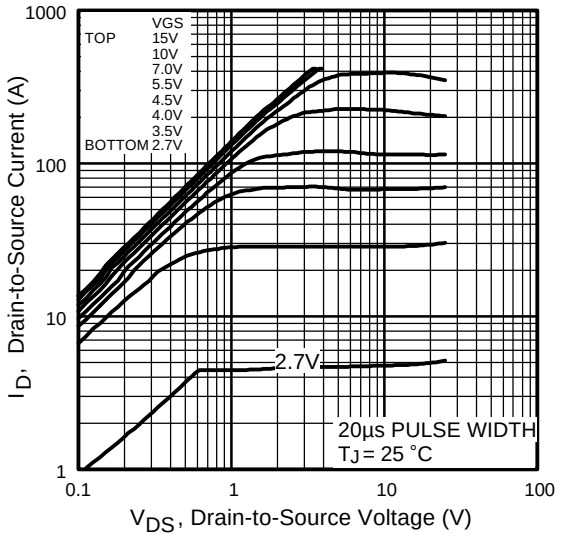


Fig 1. Typical Output Characteristics

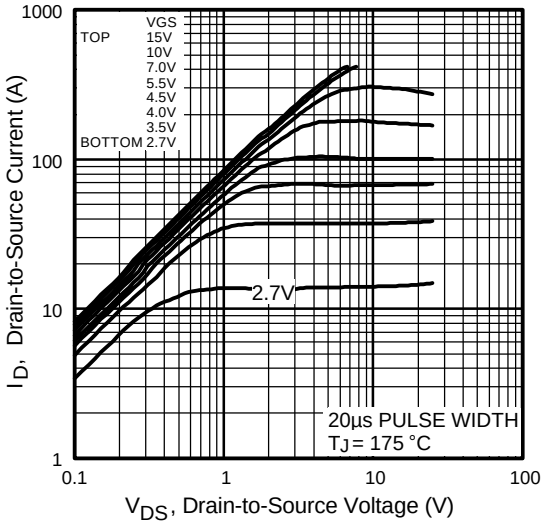


Fig 2. Typical Output Characteristics

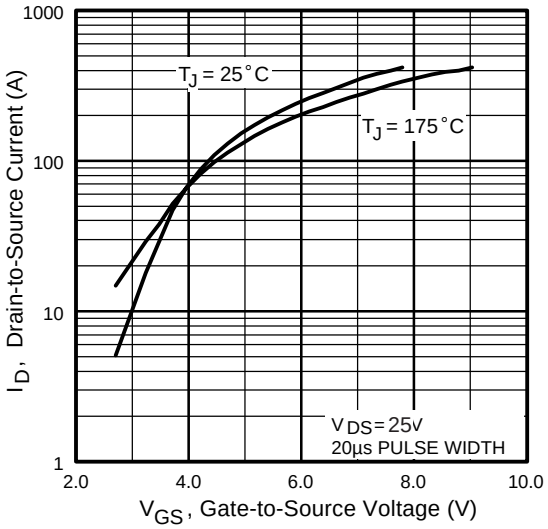


Fig 3. Typical Transfer Characteristics

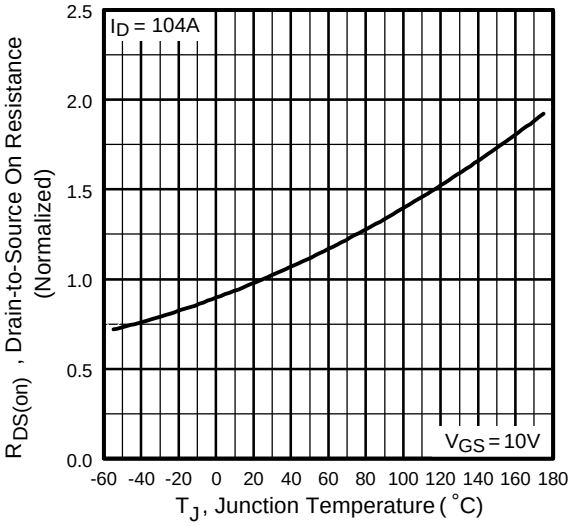


Fig 4. Normalized On-Resistance Vs. Temperature

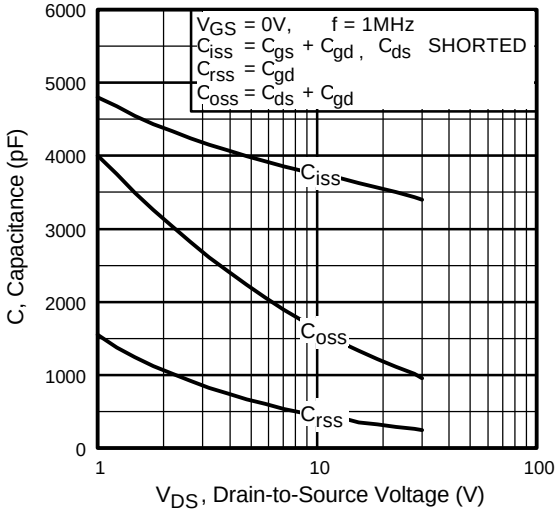


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

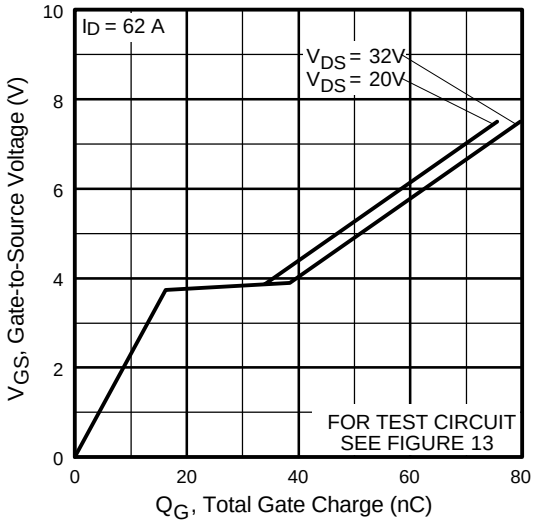


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

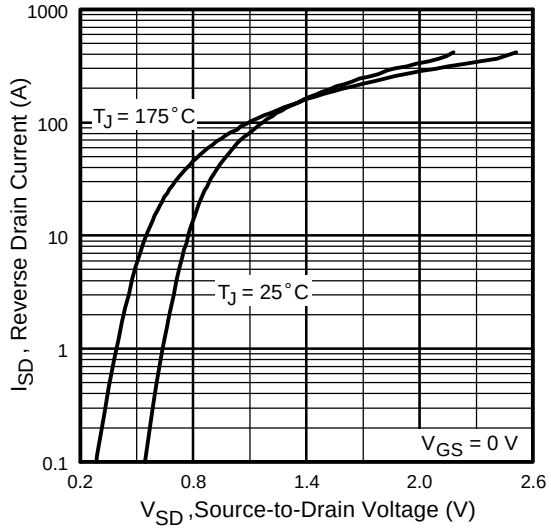


Fig 7. Typical Source-Drain Diode Forward Voltage

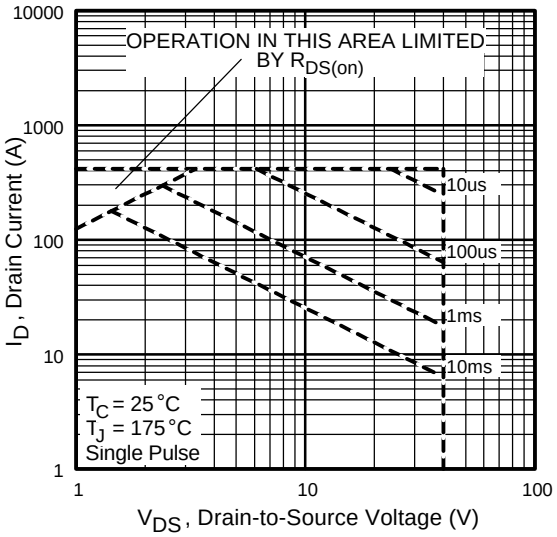


Fig 8. Maximum Safe Operating Area

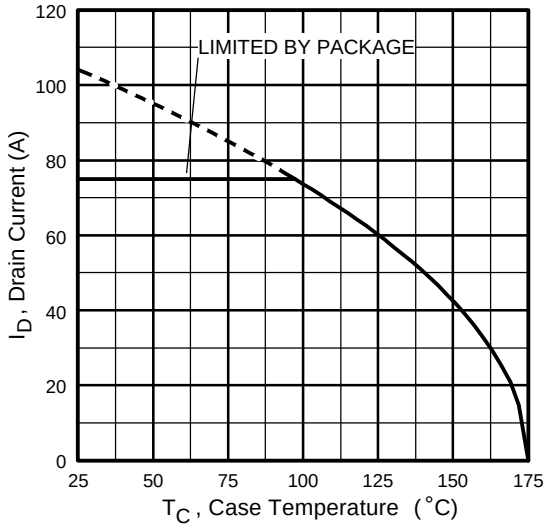


Fig 9. Maximum Drain Current Vs. Case Temperature

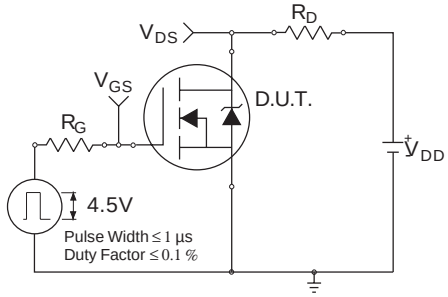


Fig 10a. Switching Time Test Circuit

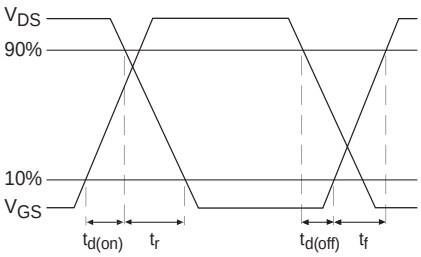


Fig 10b. Switching Time Waveforms

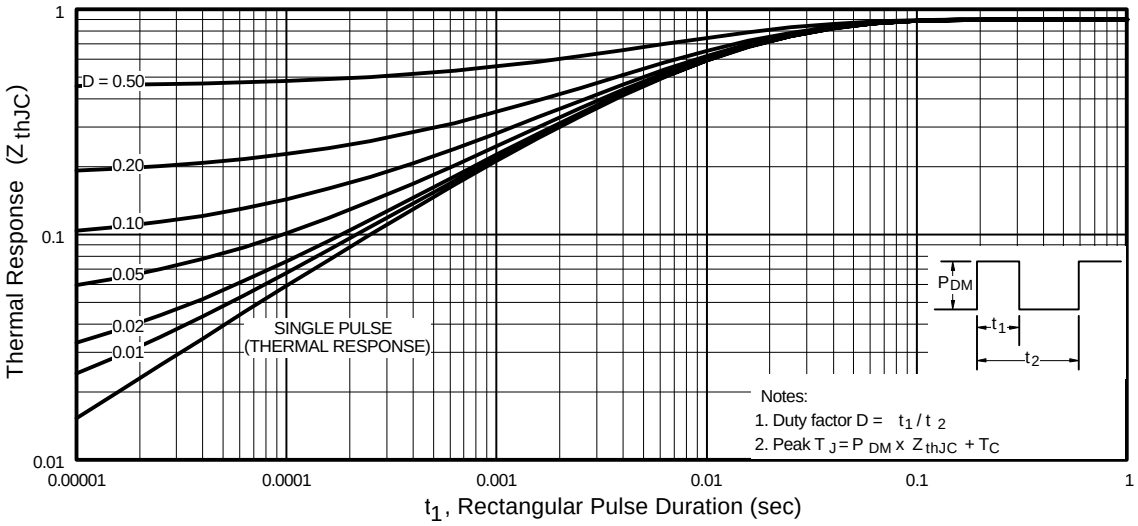


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

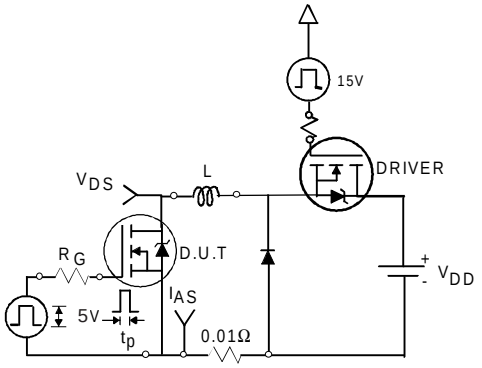


Fig 12a. Unclamped Inductive Test Circuit

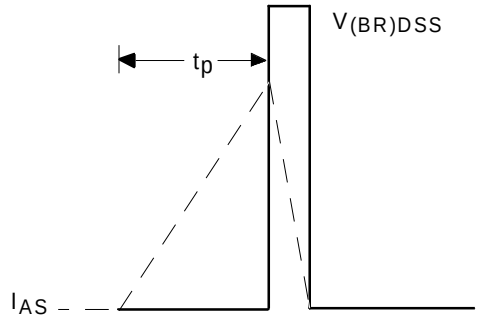


Fig 12b. Unclamped Inductive Waveforms

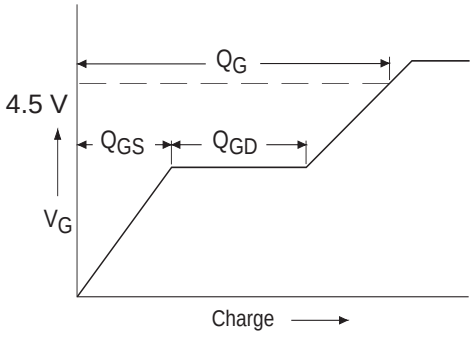


Fig 13a. Basic Gate Charge Waveform

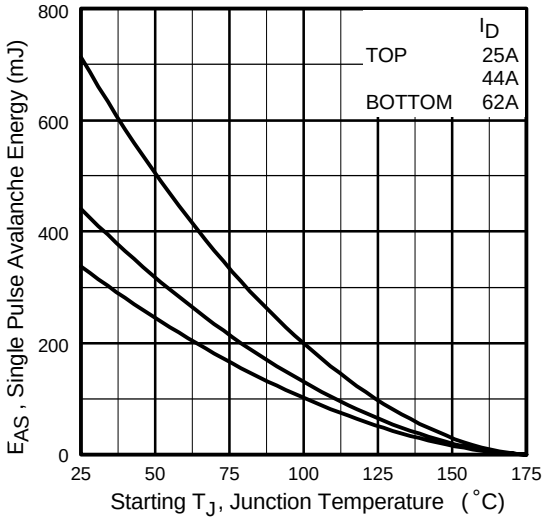


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

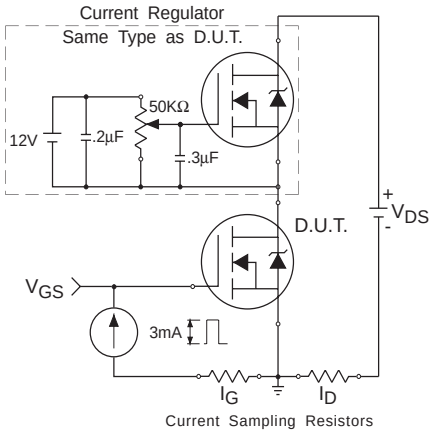
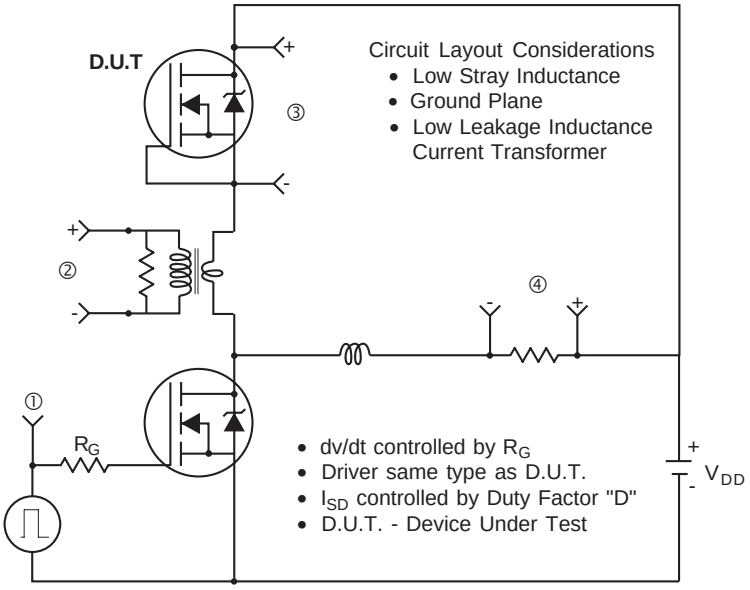
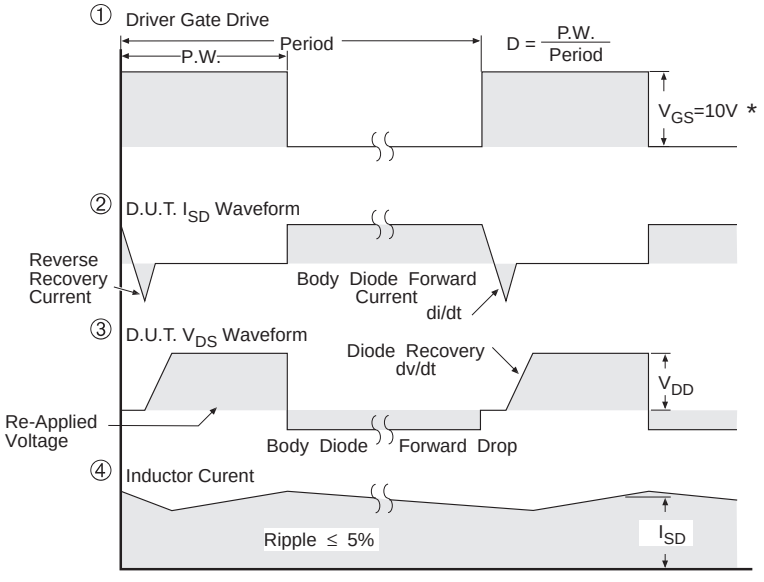


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

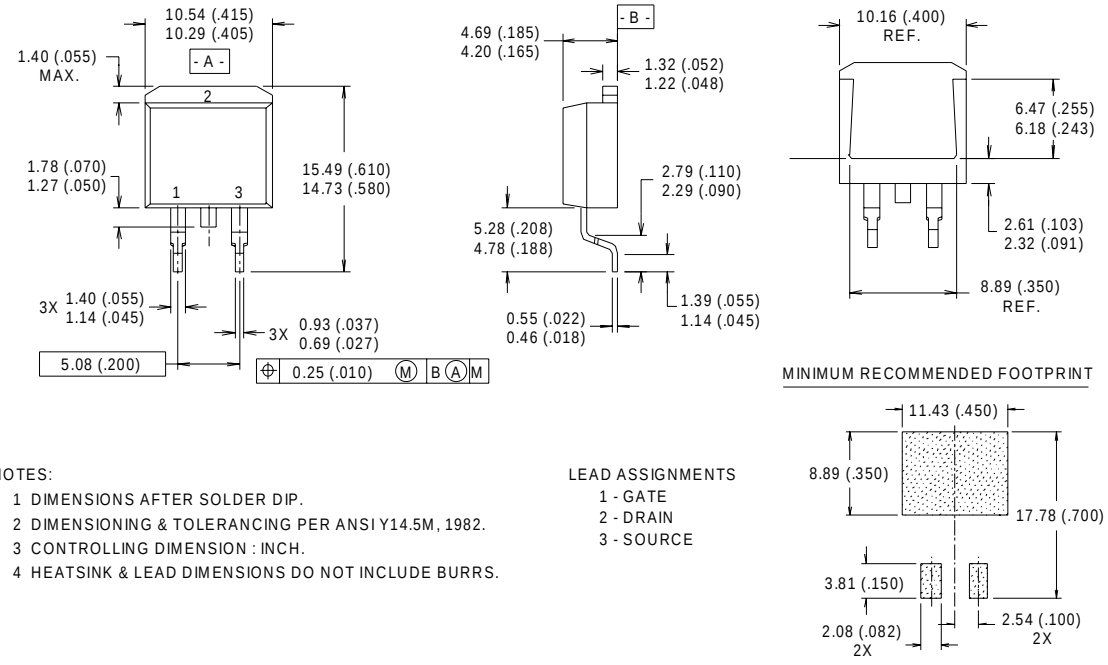




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

D²Pak Package Details



NOTES:

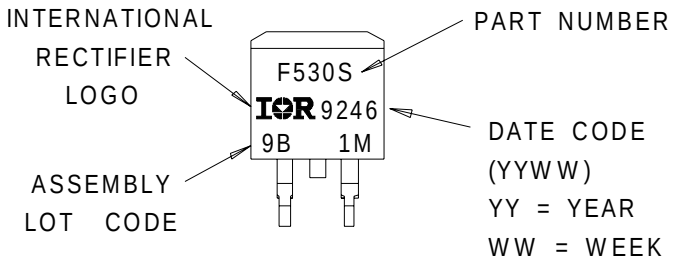
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

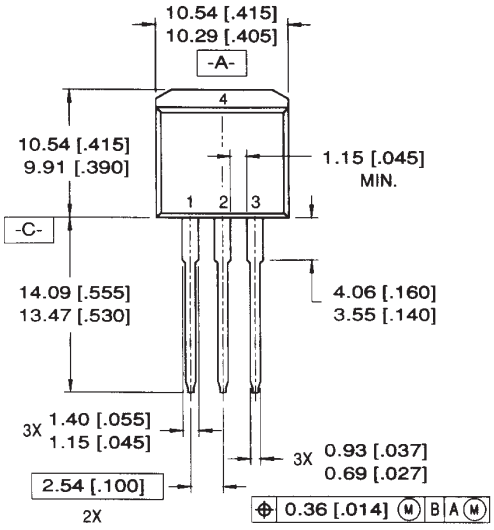
1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT

Part Marking

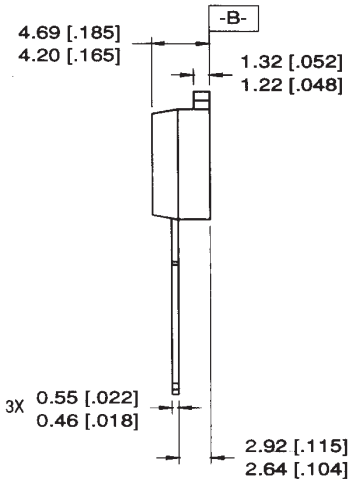


TO-262 Package Details



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

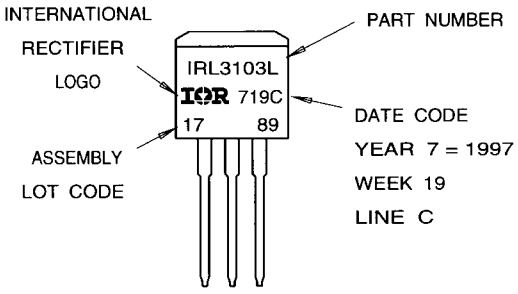


NOTES:

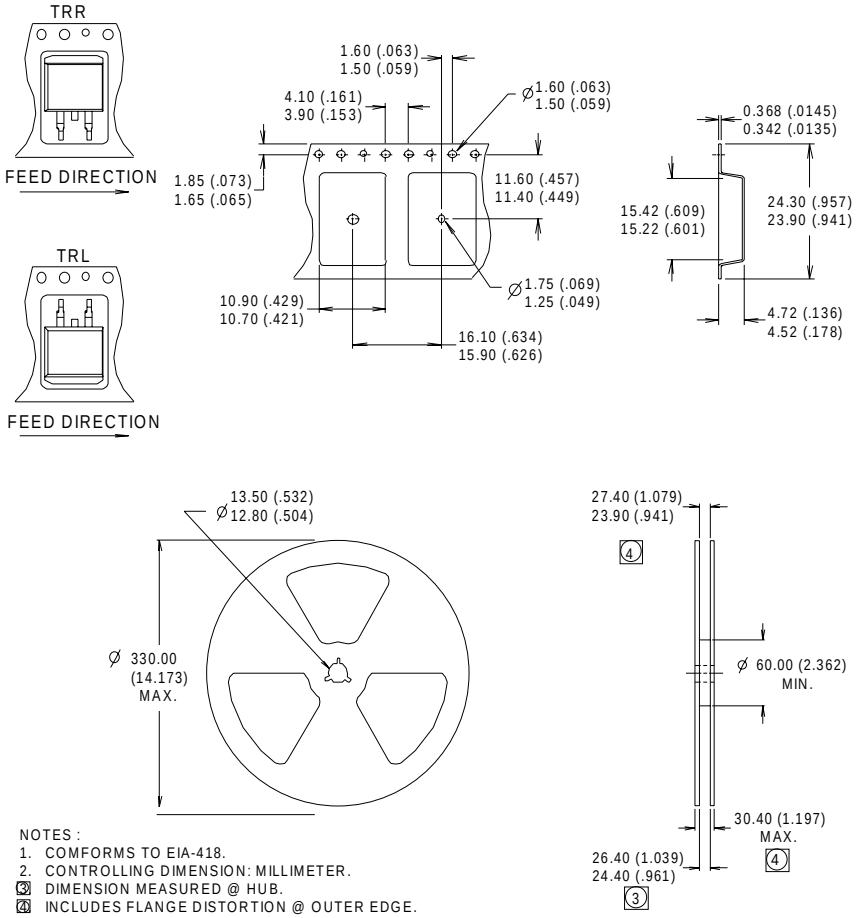
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape and Reel



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

International
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IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
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http://www.irf.com/ Data and specifications subject to change without notice. 10/98

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/