4096 WORD x 1 BIT STATIC RAM

N CHANNEL SILICON GATE DEPLETION LOAD

TMM315D
TMM315D-1

DESCRIPTION

TMM315D/TMM315D-1 are 4096 word x 1 bit read write memories operated with 5V single power supply. The memories are static in operation and require no clocks or refresh period. This device has two types in data access - address access and chip select access which are equal and very high speed. When $\overline{CS}$ goes high, this device is deselected and changes into the low power standby mode automatically, and keep its state during the period that $\overline{CS}$ is high. Accordingly, this device is suitable for use in larger memory system which the majority of devices are deselected, and is suitable for use in cache memory required very high speed. TMM315D/TMM315D-1 are directly TTL compatible and its output can drive the TTL up to 5. TMM315D/TMM315D-1 are fabricated with N-channel silicon gate depletion load type technology for stable and high performance. The chip is mounted in the standard 18 pin package of 0.3 inch width for low cost purpose.

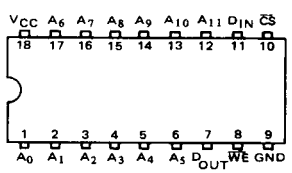
FEATURES

- Fully decoded 4096 word x 1 bit organization
- Static operation — No clocks
- 5V single power supply
- Easy memory expansion — $\overline{CS}$ input
- Standby feature — $\overline{CS} = V_{IH}$
- I/O separate
- Three state output
- Directly TTL compatible
- Current and Access time (Maximum value)

PARAMETER	TMM315D-1	TMM315D
Active Current (Max.)	180 mA	160 mA
Standby Current (Max.)	30 mA	20 mA
Address Access time	55 ns	70 ns
Chip select Access time	55 ns	70 ns

- Pin to pin compatible — i2147/i2147-3
- Inputs protected — All inputs have protection against static charge.

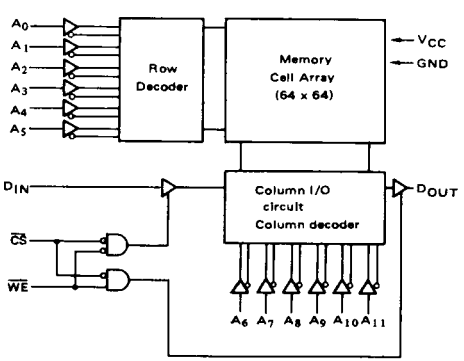
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_5$	Row Address inputs
$A_6 \sim A_{11}$	Column Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select input
$\overline{WE}$	Write enable input
V_{CC}/GND	Power supply

BLOCK DIAGRAM



OPERATION MODE

$\overline{CS}$	$\overline{WE}$	Output	Power	Mode
H	*	High-Impedance	Standby	Deselected
L	H	Data out	Active	Read
L	L	High-Impedance	Active	Write

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power supply voltage	−1.5 ~ 7.0	V
$V_{IN, OUT}$	Input and output voltage	−1.5 ~ 7.0	V
T_{opr}	Operating temperature	0 ~ 70	°C
T_{strg}	Storage temperature	−55 ~ 150	°C
T_{solder}	Soldering temperature · time	260 · 10	°C · sec
P_D	Power dissipation (Ta = 70°C)	1.0	W
I_{out}	DC output current	20	mA

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high voltage	—	2.0	–	6.0	V
V_{IL}	Input low voltage	—	−1.0	–	0.8	V
V_{CC}	Power supply voltage	—	4.5	5.0	5.5	V

DC CHARACTERISTICS

Ta = 0 ~ 70°C, V_{CC} = 5.0V± 10%,unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{OH}	Output high voltage	Isource = −4.0 mA		2.4	–	–	V
V_{OL}	Output low voltage	Isink = 8 mA		–	–	0.4	V
I_{OH}	Output high current	V_{OH} = 2.4V		−4.0	–	–	mA
I_{OL}	Output low current	V_{OL} = 0.4V		8.0	–	–	mA
I_{LI}	Input leakage current	V_{IN} = 0 ~ V_{CC}		–	±0.01	±10	μA
I_{LO}	Output leakage current	V_{OUT} = 0 ~ 4.5V $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}		–	±0.1	±50	μA
I_{CC}	Operating current	$\overline{CS}$ = V_{IL} output open	TMM315D	–	–	160	mA
			TMM315D-1	–	–	180	mA
I_{SB}	Standby current	$\overline{CS}$ = V_{IH} output open	TMM315D	–	–	20	mA
			TMM315D-1	–	–	30	mA
I_{SBP}	Peak power on current	$\overline{CS}$ = V_{IH} during power on	TMM315D	–	–	50	mA
			TMM315D-1	–	–	70	mA

* Typical values are at V_{CC} = 5.0V, Ta = 25°C.

A.C. CHARACTERISTICS

Ta = 0 ~ 70°C, V_{CC} = 5V± 10%,unless otherwise noted.

- **READ CYCLE**

SYMBOL	PARAMETER	TMM315D-1		TMM315D		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read cycle time	55	–	70	–	ns
t_{ACC}	Address access time	–	55	–	70	ns
t_{CO_1}	Chip select access time 1	–	55	–	70	ns
t_{CO_2}	Chip select access time 2	–	65	–	80	ns
t_{OH}	Output hold from address change	5	–	5	–	ns
t_{LZ}	Chip selection to output in low Z	10	–	10	–	ns
t_{HZ}	Chip deselection to output in high Z	0	40	0	40	ns
t_{PU}	Chip selection to power up time	0	–	0	–	ns
t_{PD}	Chip deselection to power down time	–	30	–	30	ns

- **WRITE CYCLE**

SYMBOL	PARAMETER	TMM315D-1		TMM315D		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write cycle time	55	–	70	–	ns
t_{CW}	Chip selection to end of write	45	–	55	–	ns
t_{AW}	Address valid to end of write	45	–	55	–	ns
t_{AS}	Address set up time	0	–	0	–	ns
t_{WP}	Write pulse width	35	–	40	–	ns
t_{WR}	Write recovery time	10	–	15	–	ns
t_{DS}	Data set up time	25	–	30	–	ns
t_{DH}	Data hold time	10	–	10	–	ns
t_{ODW}	Write enable to output in high Z	0	30	0	35	ns
t_{WO}	Output active from end of write	0	–	0	–	ns

- **AC TEST CONDITIONS**

Input pulse levels	0 ~ 3.5V
Input rise and fall times	10 ns
Input and output timing reference levels	1.5V
Output load	See Fig. 1

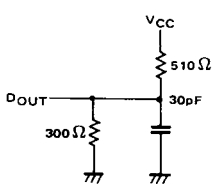


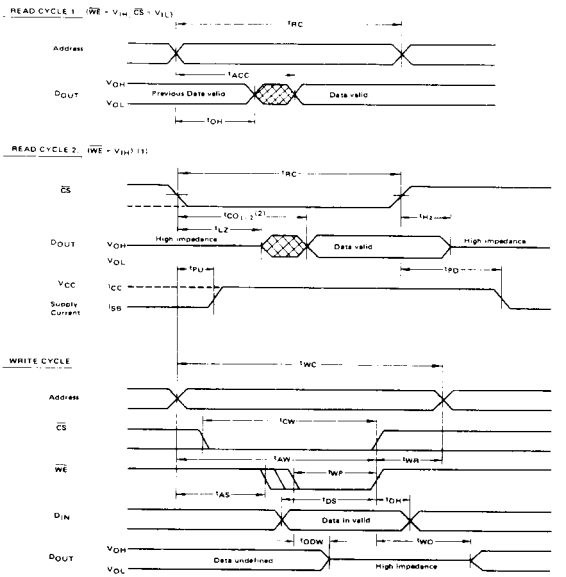
Fig. 1 Output load

[redacted]

SYMBOL	PARAMETER	MAX.	UNIT
C_{IN}	Input capacitance	5	pF
C_{OUT}	Output capacitance	7	pF

This parameter is periodically sampled and is not 100% tested.

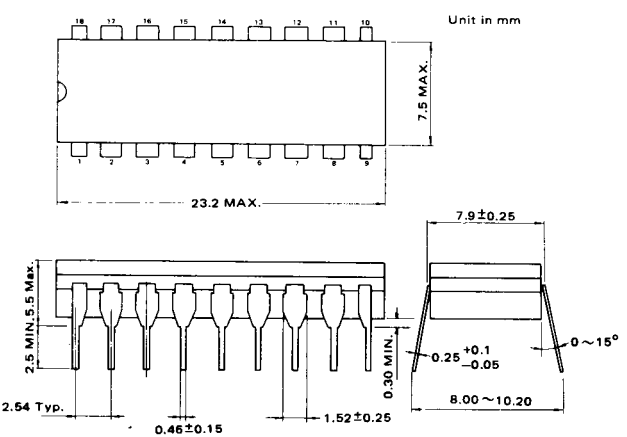
TIMING WAVEFORMS



Note: (1) Addresses are to valid prior to or coincident with $\overline{CS}$ transition low.
(2) t_{CO1}: Chip is deselected for a time that is greater than 55 ns prior to selection.
t_{CO2}: Chip is deselected for a time that is less than 55 ns prior to selection.

OUTLINE DRAWINGS

Unit in mm



Note. 1. Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 18 leads.
2. All dimensions are in millimeters.