



SPP3052

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP3052 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as DC/DC converter and Desktop computer power management.

The package is universally preferred for commercial industrial surface mount applications

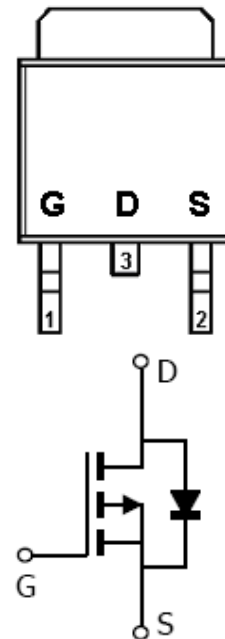
FEATURES

- ◆ -30V/- 25A, $R_{DS(ON)}=50m\Omega@V_{GS}=-10V$
- ◆ -30V/- 16A, $R_{DS(ON)}=85m\Omega@V_{GS}=-5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L package design

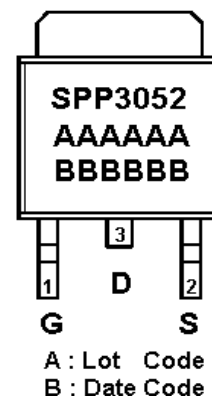
APPLICATIONS

- Power Management in Desktop Computer
- DC/DC Converter
- LCD Display inverter

PIN CONFIGURATION (TO-252-2L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3052T252RG	TO-252-2L	SPP3052
SPP3052T252RGB	TO-252-2L	SPP3052

- ※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)
- ※ SPP3052T252RG : Tape Reel ; Pb – Free
- ※ SPP3052T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-25
		TA=70°C	-18
Pulsed Drain Current	I _{DM}	-100	A
Continuous Source Current(Diode Conduction)	I _S	-15	A
Power Dissipation	P _D	TA=25°C	40
		TA=70°C	20
Avalanche Energy with Single Pulse (T _J =25°C , L = 0.14mH , I _{AS} = 43A , V _{DD} = 20V.)	E _{AS}	129	mJ
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	105	°C/W



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ELECTRICAL CHARACTERISTICS

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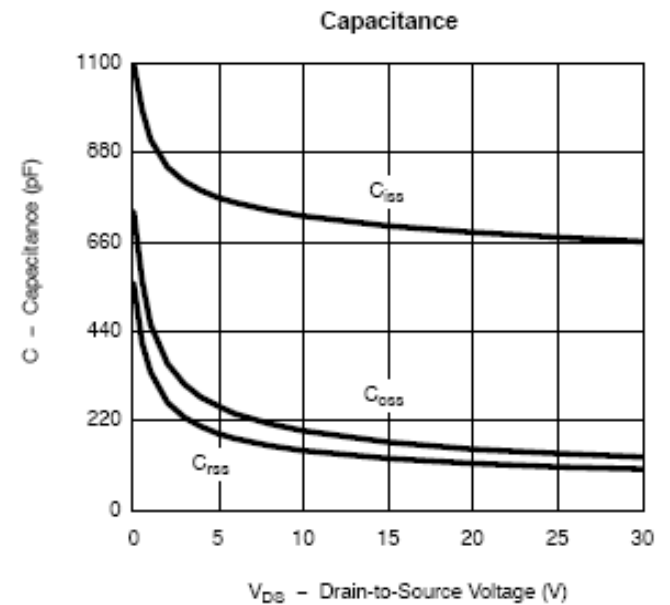
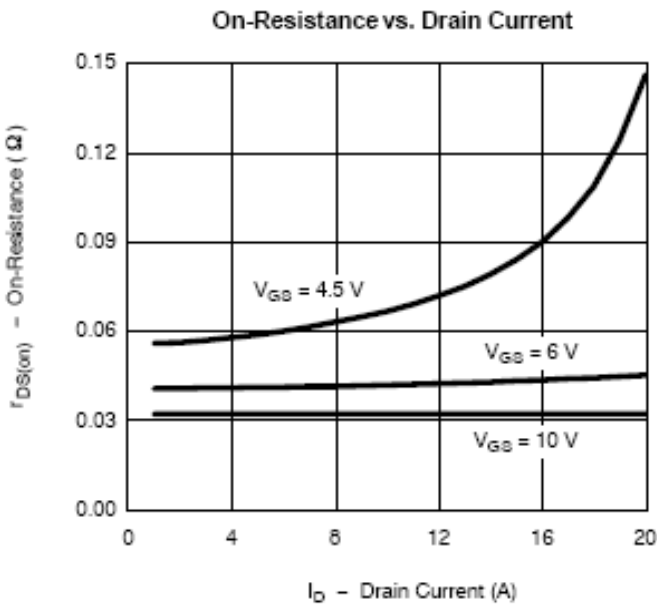
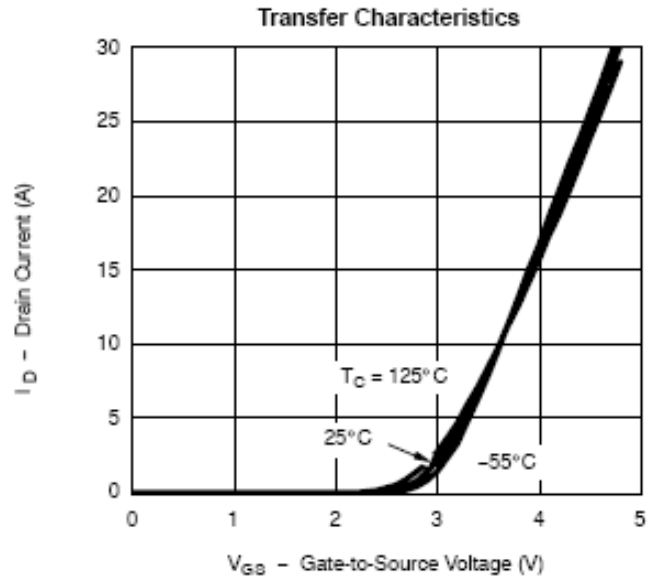
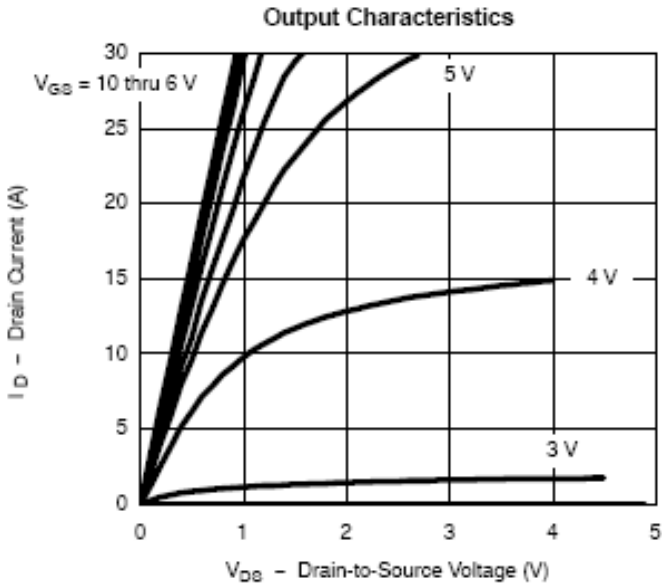
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-21V, V_{GS}=0V$			-2	uA
		$V_{DS}=-21V, V_{GS}=0V$ $T_J=55^\circ C$			-5	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-25A$		0.040	0.050	Ω
		$V_{GS}=-5V, I_D=-16A$		0.068	0.085	
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-8A$		8		S
Diode Forward Voltage	V_{SD}	$I_S=-16A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V, V_{GS}=-10V$ $I_D=-3.5A$		16	24	nC
Gate-Source Charge	Q_{gs}			2.3		
Gate-Drain Charge	Q_{gd}			4.5		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		680		pF
Output Capacitance	C_{oss}			120		
Reverse Transfer Capacitance	C_{rss}			75		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-10V$ $R_G=6\Omega$		14	25	ns
	t_r			15	26	
Turn-Off Time	$t_{d(off)}$			42	70	
	t_f			30	50	



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TYPICAL CHARACTERISTICS

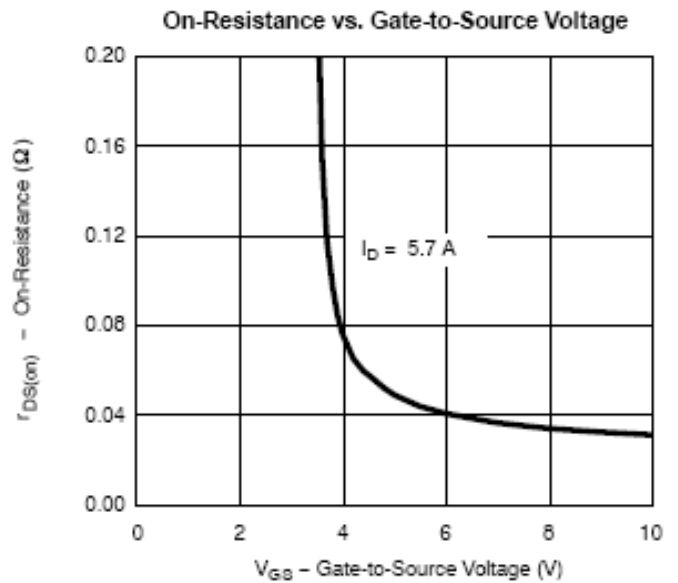
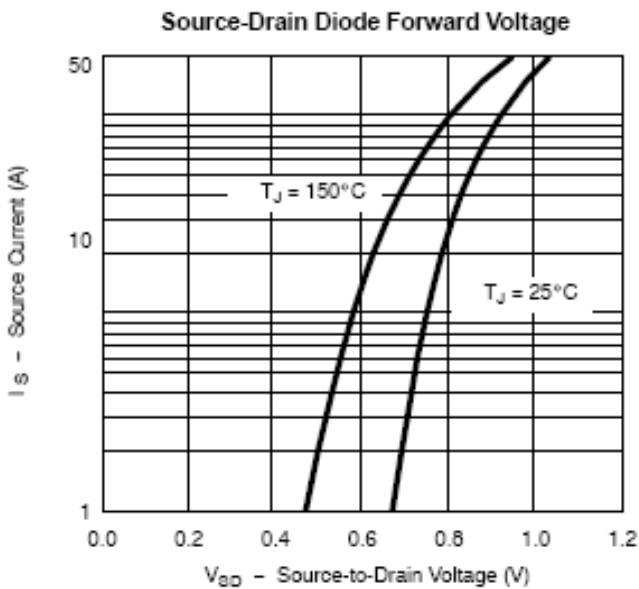
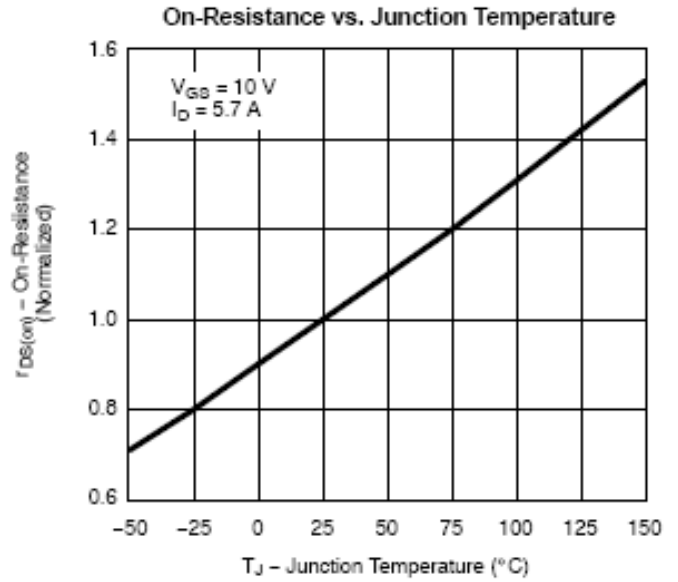
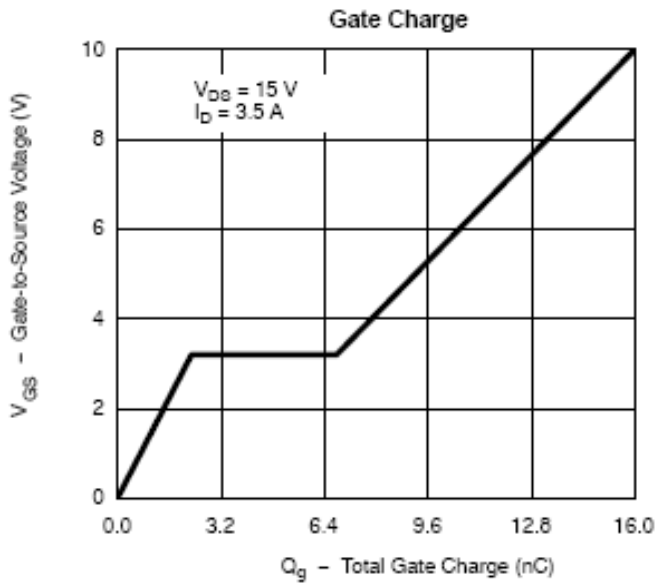




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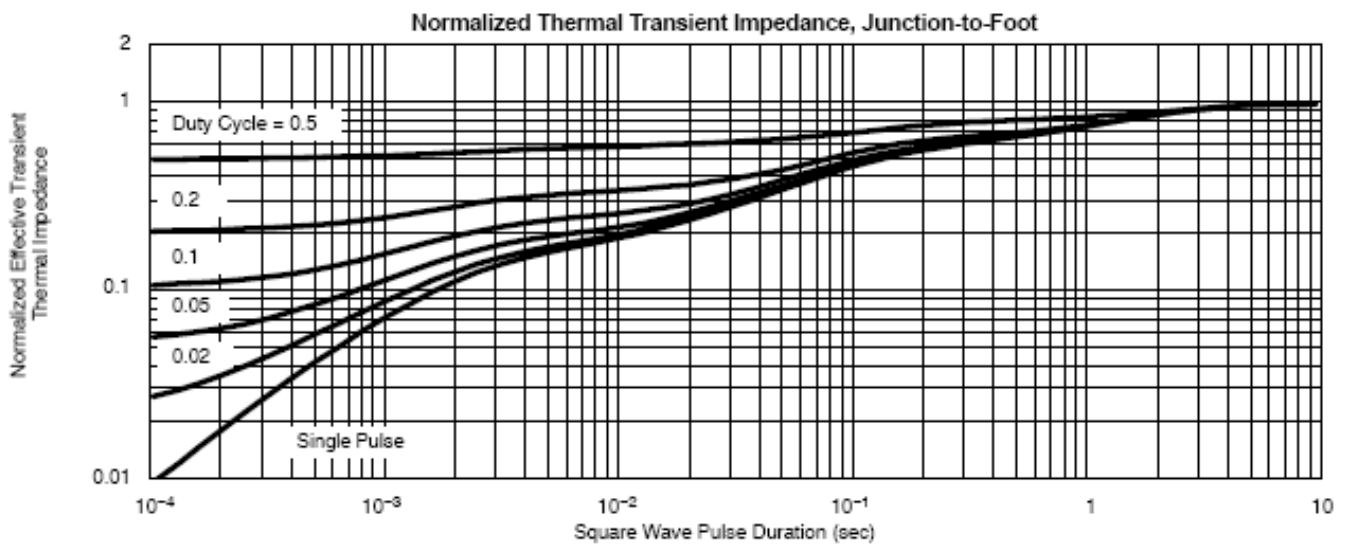
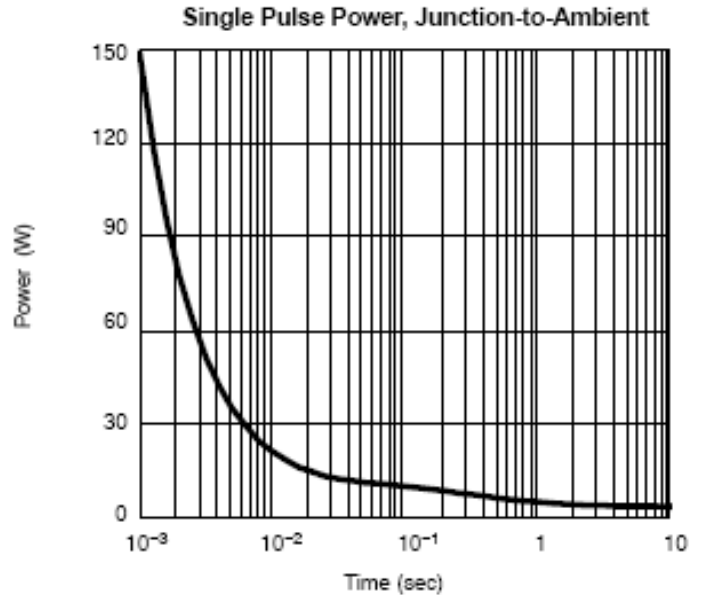
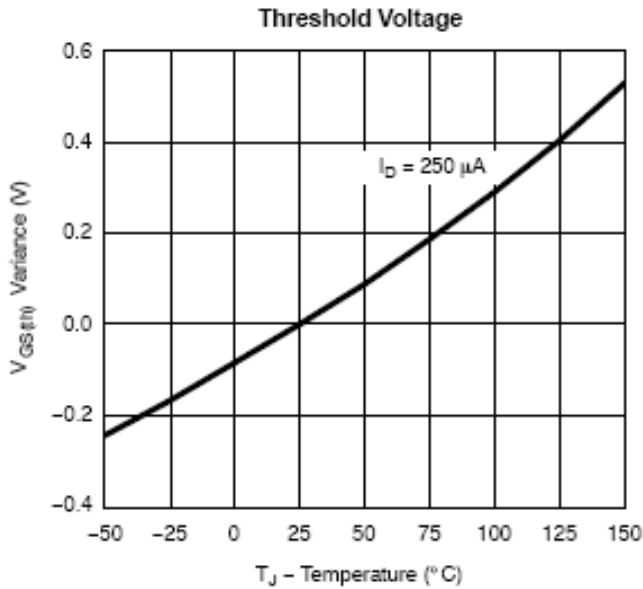




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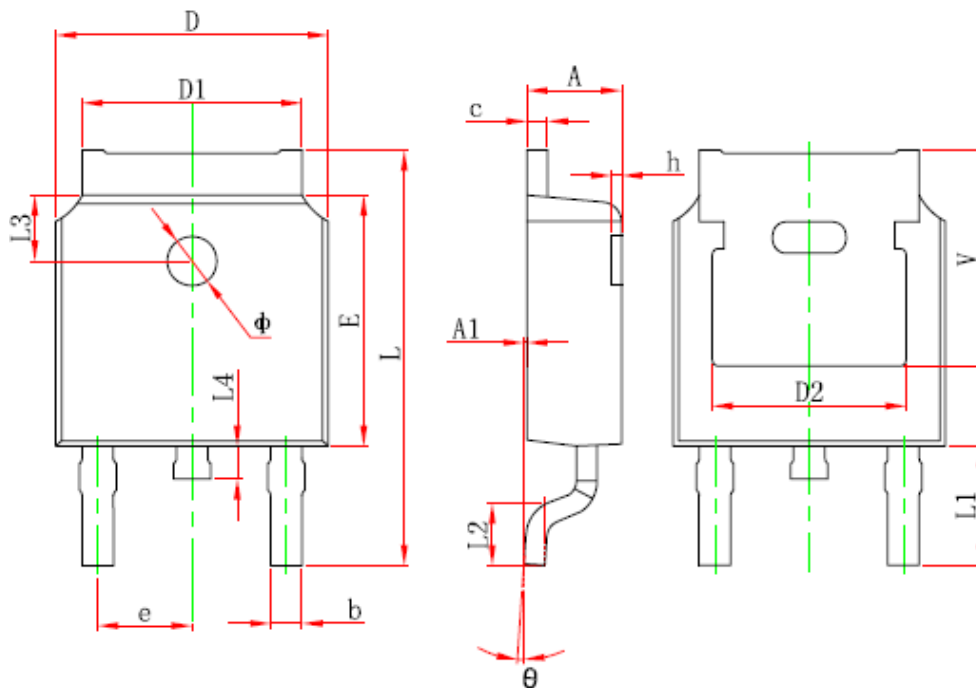




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TO-252-2L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	



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