

## FEATURES

- ❑ 4K x 4 Static RAM with Common I/O, Output Enable (L7C170 only)
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 8 ns maximum
- ❑ Low Power Operation  
Active: 190 mW typical at 35 ns  
Standby: 100 µW typical
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ Plug Compatible with IDT 6168 and Cypress CY7C168/170
- ❑ Package Styles Available:
  - 20/22-pin Plastic DIP
  - 20/22-pin Sidebrazed, Hermetic DIP
  - 20/22-pin CerDIP
  - 20-pin Plastic SOIC
  - 20/24-pin Plastic SOJ
  - 20-pin Ceramic LCC

## DESCRIPTION

The L7C168 and L7C170 are high-performance, low-power CMOS static RAMs. The storage cells are organized as 4096 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C170 version adds an active-low Output Enable control. These devices are available in seven speeds with maximum access times from 8 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 190 mW (typical) when being operated at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write

accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C168 and L7C170 consume only 15 µW (typical) at 3 V, allowing effective battery backup operation.

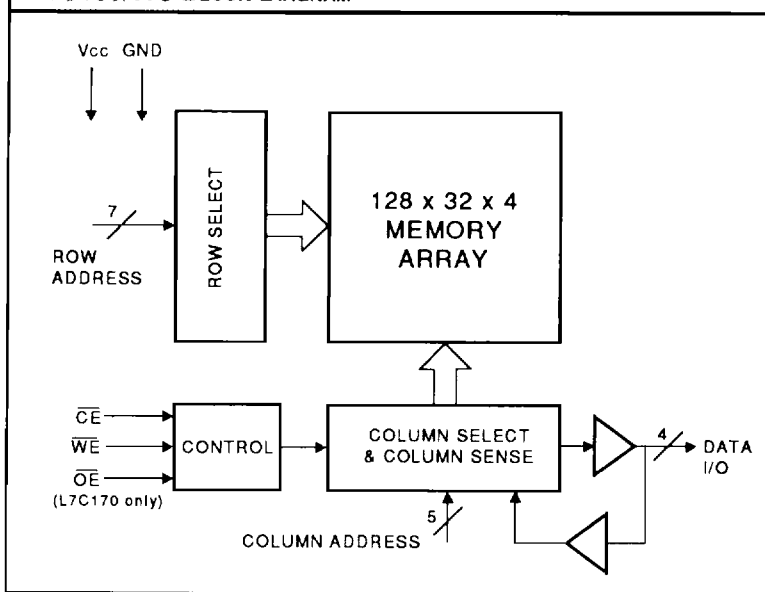
The L7C168 and L7C170 provide asynchronous (unlocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A0 through A11. Reading from a designated location is accomplished by presenting an address and driving CE low while WE remains high. The data in the addressed memory location will then appear on the Data I/O pins within one access time. The I/O pins stay in a high-impedance state when CE or OE is high or WE is low.

Writing to an addressed location is accomplished when the active-low CE and WE inputs are low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C168 and L7C170 can withstand an injection current of up to 200 mA on any pin without damage.

**L7C168/170 BLOCK DIAGRAM**

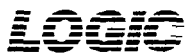


<b>MAXIMUM RATINGS</b> <i>Above which useful life may be impaired (Notes 1, 2)</i>	
Storage temperature .....	-65°C to +150°C
Operating ambient temperature .....	-55°C to +125°C
V <sub>CC</sub> supply voltage with respect to ground .....	-0.5 V to +7.0 V
Input signal with respect to ground .....	-3.0 V to +7.0 V
Signal applied to high impedance output .....	-3.0 V to +7.0 V
Output current into low outputs .....	25 mA
Latchup current .....	> 200 mA

<b>OPERATING CONDITIONS</b> <i>To meet specified electrical and switching characteristics</i>		
Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V
Active Operation, Military	-55°C to +125°C	4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V <sub>CC</sub> ≤ 5.5 V
Data Retention, Military	-55°C to +125°C	2.0 V ≤ V <sub>CC</sub> ≤ 5.5 V

<b>ELECTRICAL CHARACTERISTICS</b> <i>Over Operating Conditions (Note 5)</i>						
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4.0 mA, V <sub>CC</sub> = 4.5 V	2.4			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8.0 mA			0.4	V
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	(Note 3)	-3.0		0.8	V
I <sub>Ix</sub>	Input Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10		+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , C <sub>E</sub> = V <sub>CC</sub>	-10		+10	μA
I <sub>OS</sub>	Output Short Current	V <sub>OUT</sub> = GND, V <sub>CC</sub> = Max (Note 4)			-350	mA
I <sub>CC2</sub>	V <sub>CC</sub> Current, TTL Inactive	(Note 7)		15	30	mA
I <sub>CC3</sub>	V <sub>CC</sub> Current, CMOS Standby	(Note 8)		20	100	μA
I <sub>CC4</sub>	V <sub>CC</sub> Current, Data Retention	V <sub>CC</sub> = 3.0 V (Note 9)		5	50	μA
C <sub>IN</sub>	Input Capacitance	Ambient Temp = 25°C, V <sub>CC</sub> = 5.0 V			5	pF
C <sub>OUT</sub>	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

Symbol	Parameter	Test Condition	L7C168/170-							Unit
			35	25	20	15	12	10	8	
I <sub>CC1</sub>	V <sub>CC</sub> Current, Active	(Note 6)	50	65	85	110	135	150	165	mA



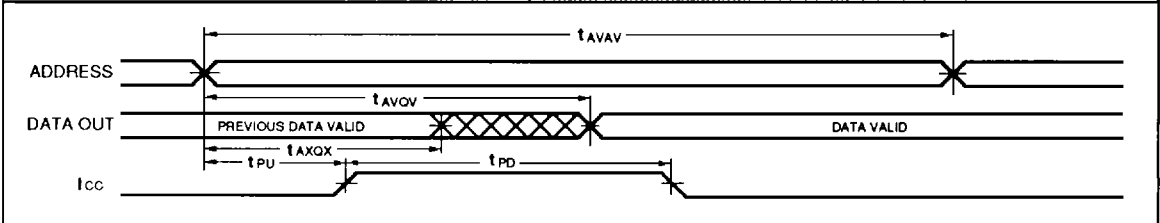
**SWITCHING CHARACTERISTICS** Over Operating Range (ns)

**READ CYCLE** (Notes 5, 11, 12, 22, 23, 24)

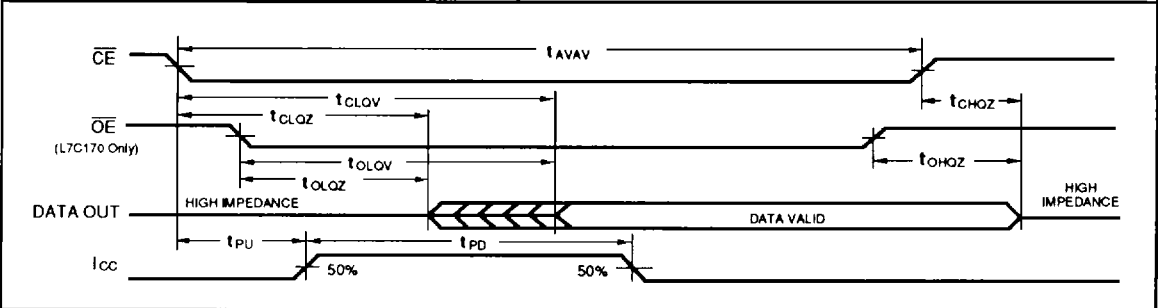
Symbol	Parameter	L7C168/170-													
		35		25		20		15		12		10		8	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	35		25		20		15		12		10		8	
tAVOV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
tAXOQ	Address Change to Output Change	3		3		3		3		3		3		3	
tCLOV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
tCLOZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
tCHOZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
tOLOV	Output Enable Low to Output Valid		15		12		10		8		6		4		4
tOLOZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0		0	
tOHOZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		4
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	

2

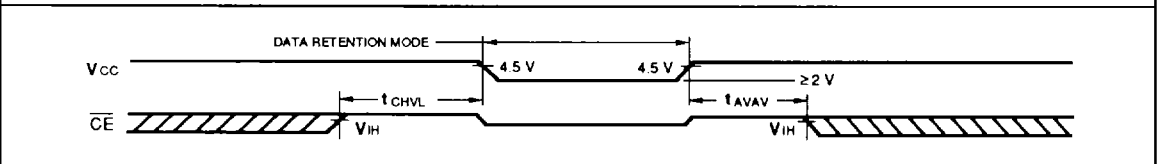
**READ CYCLE — ADDRESS CONTROLLED** (Notes 13, 14)



**READ CYCLE — CE/OE CONTROLLED** (Notes 13, 15)

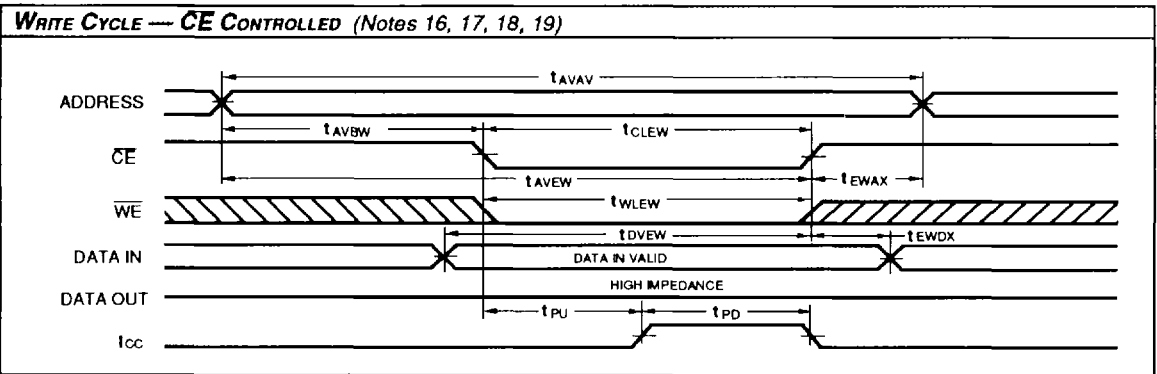
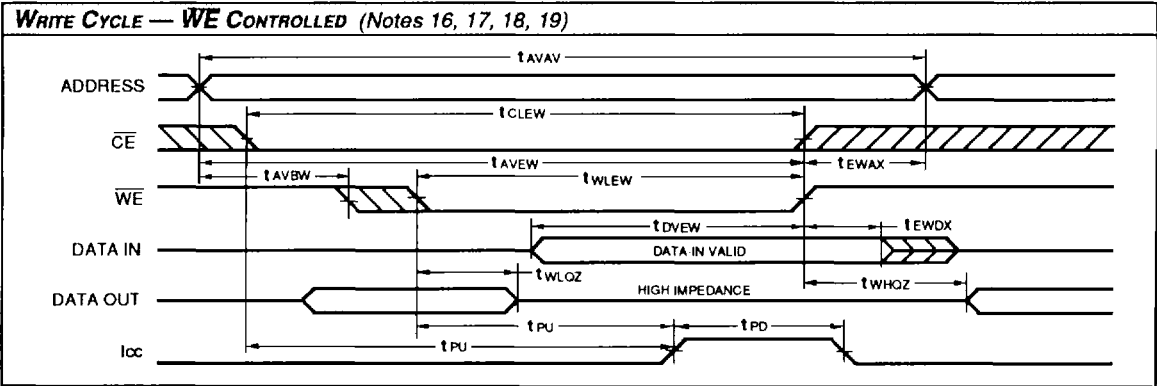


**DATA RETENTION**



**SWITCHING CHARACTERISTICS** *Over Operating Range (ns)*

Symbol		Parameter		L7C168/170-													
				35		25		20		15		12		10		8	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12		10		8			
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8			
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0			
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8		8			
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0		0			
twLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5			
tdVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5		4			
tEWDX	End of Write Cycle to Data Change	1		1		1		1		1		1		1			
tWHOZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0			
twLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3		



## NOTES

- Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.
- The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.
- This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at  $-0.6$  V. A current in excess of 100 mA is required to reach  $-2$  V. The device can withstand indefinite operation with inputs as low as  $-3$  V subject only to power dissipation and bond wire fusing constraints.
- Duration of the output short circuit should not exceed 30 seconds.
- A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.
- Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e.,  $CE \leq V_{II}$ ,  $WE \leq V_{II}$ . Input pulse levels are 0 to 3.0 V.
- Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e.,  $CE \geq V_{III}$ .
- Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e.,  $CE = V_{CC}$ . Input levels are within 0.2 V of VCC or ground.
- Data retention operation requires that VCC never drop below 2.0 V. CE must be  $\geq V_{CC} - 0.2$  V. For all other inputs  $V_{IN} \geq V_{CC} - 0.2$  V or  $V_{IN} \leq 0.2$  V is required to ensure full powerdown.
- These parameters are guaranteed but not 100% tested.
- Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOI, and

IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example,  $t_{AVW}$  is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. WE is high for the read cycle.

14. The chip is continuously selected (CE low).

15. All address lines are valid prior to or coincident with the CE transition to low.

16. The internal write cycle of the memory is defined by the overlap of CE low and WE low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If WE goes low before or concurrent with CE going low, the output remains in a high impedance state.

18. If CE goes high before or concurrent with WE going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

- Falling edge of CE.
- Falling edge of WE (CE active).
- Transition on any address line (CE active).
- Transition on any data line (CE and WE active).

The device automatically powers down from ICC2 to ICC1 after  $t_{PD}$  has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured  $\pm 200$  mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. CE or WE must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01  $\mu$ F high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

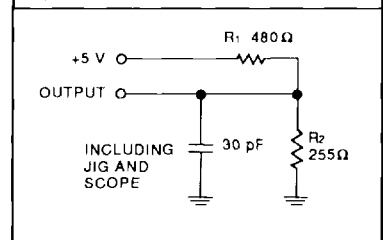


FIGURE 1b.

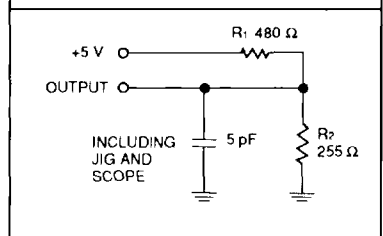
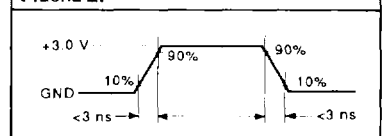
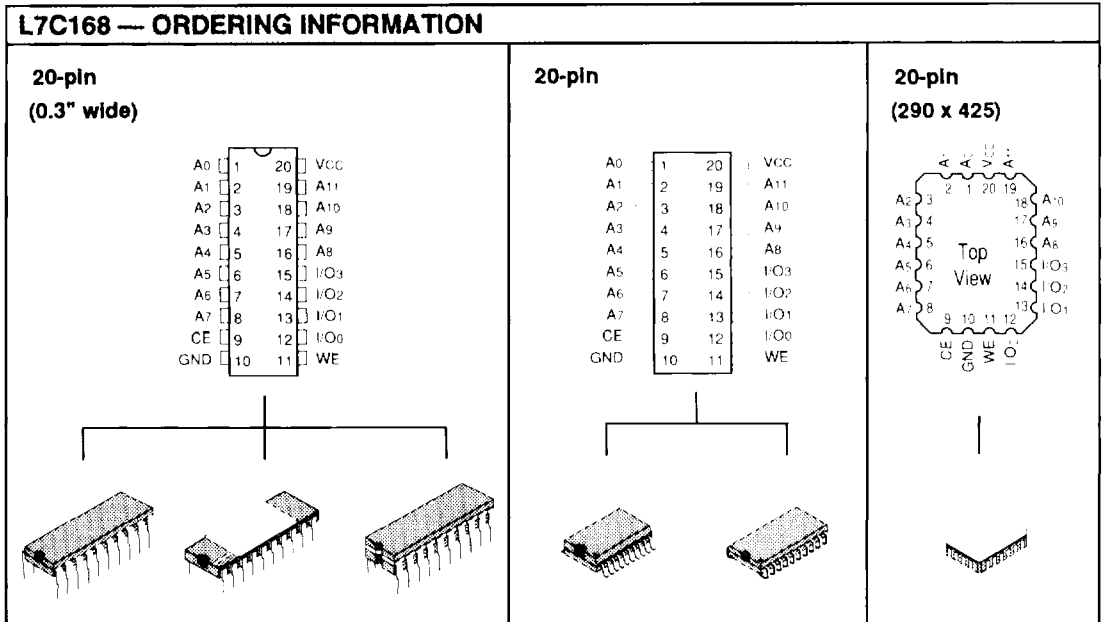


FIGURE 2.



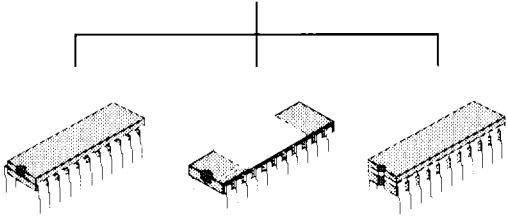


Speed	Plastic DIP (P6)	Sidebraze Hermetic DIP (D7)	CerDIP (C2)	Plastic SOIC (.300" — U3)	Plastic SOJ (.300" — W3)	Ceramic Leadless Chip Carrier (K6)
<b>0°C to +70°C — COMMERCIAL SCREENING</b>						
35 ns	L7C168PC35	L7C168DC35	L7C168CC35	L7C168UC35	L7C168WC35	L7C168KC35
25 ns	• • 25	• • 25	• • 25	• • 25	• • 25	• • 25
20 ns	• • 20	• • 20	• • 20	• • 20	• • 20	• • 20
15 ns	• • 15	• • 15	• • 15	• • 15	• • 15	• • 15
12 ns	• • 12	• • 12	• • 12	• • 12	• • 12	• • 12
10 ns	• • 10	• • 10	• • 10	• • 10	• • 10	• • 10
8 ns	• • 8	• • 8	• • 8	• • 8	• • 8	• • 8
<b>-55°C to +125°C — COMMERCIAL SCREENING</b>						
35 ns		L7C168DM35	L7C168CM35			L7C168KM35
25 ns		• • 25	• • 25			• • 25
20 ns		• • 20	• • 20			• • 20
15 ns		• • 15	• • 15			• • 15
12 ns		• • 12	• • 12			• • 12
10 ns		• • 10	• • 10			• • 10
8 ns						
<b>-55°C to +125°C — EXTENDED SCREENING</b>						
35 ns		L7C168DME35	L7C168CME35			L7C168KME35
25 ns		• • 25	• • 25			• • 25
20 ns		• • 20	• • 20			• • 20
15 ns		• • 15	• • 15			• • 15
12 ns		• • 12	• • 12			• • 12
10 ns		• • 10	• • 10			• • 10
8 ns						
<b>-55°C to +125°C — MIL-STD-883 COMPLIANT</b>						
35 ns		L7C168DMB35	L7C168CMB35			L7C168KMB35
25 ns		• • 25	• • 25			• • 25
20 ns		• • 20	• • 20			• • 20
15 ns		• • 15	• • 15			• • 15
12 ns		• • 12	• • 12			• • 12
10 ns		• • 10	• • 10			• • 10
8 ns						

### L7C170 — ORDERING INFORMATION

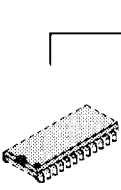
**22-pin  
(0.3" wide)**

A0	1	22	VCC
A1	2	21	A11
A2	3	20	A10
A3	4	19	A9
A4	5	18	A8
A5	6	17	NC
A6	7	16	I/O3
A7	8	15	I/O2
CE	9	14	I/O1
OE	10	13	I/O0
GND	11	12	WE



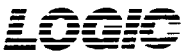
**24-pin**

A0	1	24	VCC
A1	2	23	A11
A2	3	22	A10
A3	4	21	A9
A4	5	20	A8
A5	6	19	NC
NC	7	18	NC
A6	8	17	I/O3
A7	9	16	I/O2
CE	10	15	I/O1
OE	11	14	I/O0
GND	12	13	WE



2

Speed	Plastic DIP (P8)	Sidebraze Hermetic DIP (D8)	CerDIP (C3)	Plastic SOJ (.300" — W1)		
<b>0°C to +70°C — COMMERCIAL SCREENING</b>						
35 ns	L7C170PC35	L7C170DC35	L7C170CC35	L7C170WC35		
25 ns	• • 25	• • 25	• • 25	• • 25		
20 ns	• • 20	• • 20	• • 20	• • 20		
15 ns	• • 15	• • 15	• • 15	• • 15		
12 ns	• • 12	• • 12	• • 12	• • 12		
10 ns	• • 10	• • 10	• • 10	• • 10		
8 ns	• • 8	• • 8	• • 8	• • 8		
<b>-55°C to +125°C — COMMERCIAL SCREENING</b>						
35 ns		L7C170DM35	L7C170CM35			
25 ns		• • 25	• • 25			
20 ns		• • 20	• • 20			
15 ns		• • 15	• • 15			
12 ns		• • 12	• • 12			
10 ns		• • 10	• • 10			
8 ns						
<b>-55°C to +125°C — EXTENDED SCREENING</b>						
35 ns		L7C170DME35	L7C170CME35			
25 ns		• • 25	• • 25			
20 ns		• • 20	• • 20			
15 ns		• • 15	• • 15			
12 ns		• • 12	• • 12			
10 ns		• • 10	• • 10			
8 ns						
<b>-55°C to +125°C — MIL-STD-883 COMPLIANT</b>						
35 ns		L7C170DMB35	L7C170CMB35			
25 ns		• • 25	• • 25			
20 ns		• • 20	• • 20			
15 ns		• • 15	• • 15			
12 ns		• • 12	• • 12			
10 ns		• • 10	• • 10			
8 ns						



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