AKD4712-A

AK4712 Evaluation Board Rev.0

GENERAL DESCRIPTION

AKD4712 is an evaluation board for quickly evaluating the AK4712, a High Definition A/V cap-less line driver.
Evaluation requires audio/video analog analyzer/generator and a power supply.

■ **Ordering guide**

AKD4712-A --- AK4712 Evaluation Board
(Control software and USB cable are included in this package.)

FUNCTION

- **RCA connectors for analog audio output**
- **XLR connectors for analog audio input**
- **RCA connectors for SD/HD video input/output**
- **USB connector for serial control interface**

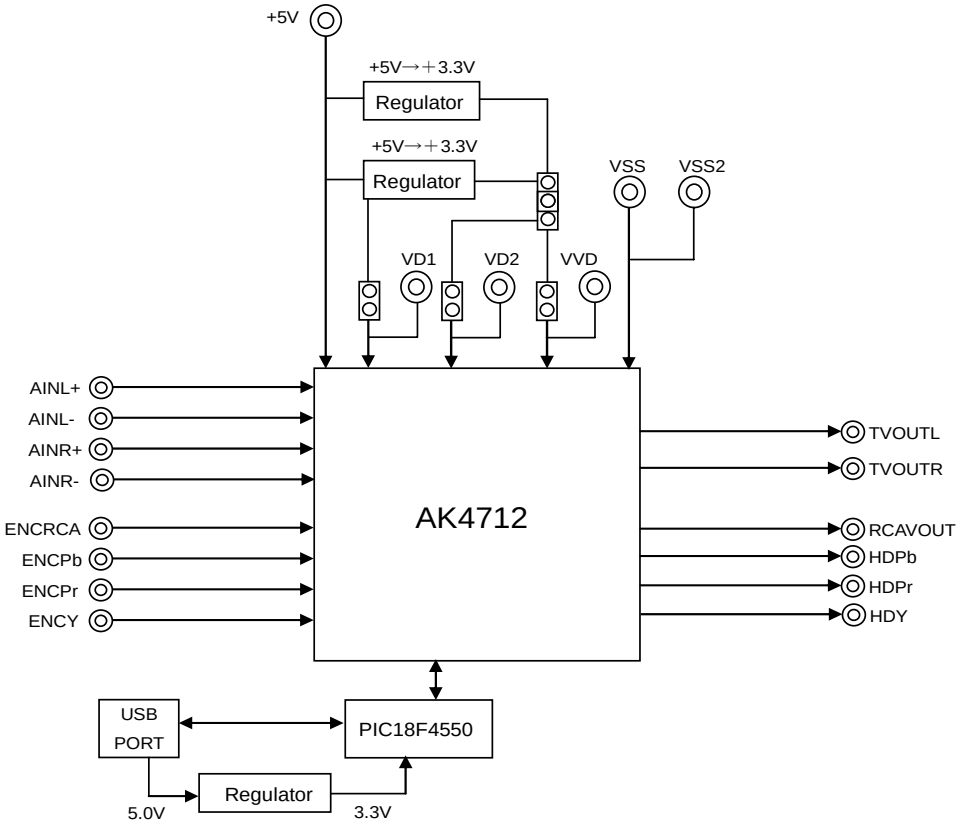


Figure 1. AKD4712 Block Diagram

※Circuit diagram and PCB layout are attached at the end of this manual.

EVALUATION BOARD MANUAL

■ Operation sequence

1) Set up the power supply lines.

Name of Jack	Color of Jack	Voltage	Used for	Comments	Default of Jack
+5V	Yellow	+5V	Power supply of AK4712	Should always be connected	+5V
VD1	Red	+3.13~+3.47	VD1 of AK4712	Should be connected when JP9 (VD1) is OPEN. Should be open when JP9 (VD1) is SHORT.	SHORT
VD2	Red	+3.13~+3.47V	VD2 of AK4712	Should be connected when JP11 (VD2) is OPEN. Should be open when R51 (VD2) is SHORT.	SHORT
VVD	Red	+3.13~+3.47V	VVD of AK4712 HDVVD of AK4712	Should be connected when JP12 (VVD) is OPEN. Should be open when JP12(VVD) is SHORT.	SHORT
D3.3V	Red	+3.13 ~ 3.47V	Logic Power supply	Should be connected when JP10 (D3.3V) is OPEN. Should be open when JP10 (D3.3V) is SHORT.	SHORT
VSS	Black	0V	Analog Ground	Should always be connected	0V
VSS2	Black	0V	Analog Ground	Should always be connected when VD2 is connected.	open
DGND	Black	0V	Digital Ground	Should be connected when JP8 (GND) is OPEN. Should be open when JP8(GND) is SHORT.	open

Table 1.Power supply lines

Each supply line should be distributed from the power supply unit.

2) Set-up jumper pins. (See the following.)

3) Power on.
AK4712 should be reset once by bringing SW1 “L” upon power-up.

■ Jumper pin settings

[JP1] (AINL+_SEL): AINL+ pin input select
INPUT1: R=20kΩ <Default>
INPUT2: R=0Ω

[JP2] (AINR+_SEL): AINR+ pin input select
INPUT1: R=20kΩ <Default>
INPUT2: R=0Ω

[JP3] (MUTEN/SCL_SEL): SDA/MUTEN pin input select
SDA: SDA
MUTEN: MUTEN <Default>

*When I2CSEL=”L”(Hard Wired), SDA/MUTEN pin is used for audio mute.

[JP4] (UVP/SCL_SEL): SCL/UVP (Under Voltage Protection)
SCL: SCL <Default>
UVP: UVP

*When I2CSEL=”L”, UVP pin can be used for Under Voltage Protection.

[JP5] (GND): AINL- pin input select
OPEN: J5 (AINL): 3pin <Default>
SHORT: GND (Not to use)

[JP6] (GND): AINR- pin input select
OPEN: J13 (AINR): 3pin <Default>
SHORT: GND (Not to use)

[JP7] Not for use

[JP8] (GND): Analog ground and Digital ground
OPEN: Separated
SHORT: Common. (The connector "DGND" can be open.) <Default>

[JP9] (VD1): Regulator (+3.3V) or VD1 connector
OPEN: VD1 pin is supplied from VD1 connector.
SHORT: VD1 pin is supplied from regulator (+3.3V). (The connector "VD1" can be open.) <Default>

[JP10] (D3.3V): Regulator (+3.3V) or D3.3V connector
OPEN: Logic voltage is supplied from D3.3V connector.
SHORT: Logic voltage is supplied form regulator (+3.3V). (The connector "VCC" can be open.) <Default>

[JP11] (VD2): Regulator (+3.3V) or VD2 connector
OPEN: VD2 pin is supplied from VD2 connector.
SHORT: VD2 pin is supplied from regulator (+3.3V). (The connector "VD1" can be open.) <Default>

[JP12] (VVD): Regulator (+3.3V) or VVD connector
OPEN: VVD and HVVD pins are supplied from VVD connector.
SHORT: VVD and HVVD pins are supplied from regulator (+3.3V)
(The connector "VVD" can be open.) <Default>

[JP13] (REG-SEL): Regulator (+3.3V) from T2 or T3
T2: Regulator supplied from T2. <Default>
T3: Regulator supplied from T3.

The T2 regulator can supply 3.3V to all circuits by shorting JP9, JP10, JP11 and JP12 and supplying 5V to +5V connector.

■ DIP SW Function

No.	Pin	OFF	ON	Default
1	MUTEN	Audio mute MUTEN bit L: Mute H: Unmute (default)		ON
2	I2CSEL	I2C Control Enable pin L: Disable (Hard Wired) (default) H: Enable (I2C)		OFF

When the I2CSEL pin = "L" (Hard Wired), the SDA/MUTEN pin is used for audio mute. MUTEN bit is ignored.

MUTEN pin	Audio Output Status
L	Mute
H	Unmute

(1) Hard Wired Mode

When the I2CSEL pin= "H" (I2C), MUTEN bit is used for audio mute. The SDA/MUTEN pin is used for Control Data Input.

MUTEN bit	Audio Output Status	
0	Mute	
1	Unmute	(default)

(2) I2C Mode

■ Toggle SW Function

[SW2] (PDN): Resets AK4712. Keep "H" during normal operation.

■ Board Control

The AK4712 can be controlled via USB PORT with a PC. Connect PORT1 with PC by USB cable included in AKD4712-A package. The control software is also included.

■ Analog Input/Output List

		Signal Name	Note
Audio	Input	J5(AINL+, AINL-), J12(AINR+, AINR-)	Typ. 2Vrms
	Output	J4 (TVOUTL), J8 (TVOUTR)	Typ. 2Vrms
Video	Input	J2 (ENCY), J9 (ENCPr), J6 (ENCPb), J13 (ENCRCA)	Max. 1.25Vpp
	Output	J3 (HDY), J7 (HDPb), J11(HDPr), J14(RCAVOUT)	Max. 2.5Vpp

Table 2. Analog Input/Output List

Control Software Manual

■ Evaluation Board and Control Software Settings

1. Set up the evaluation board as needed, according to the previous terms.

2. Connect the evaluation board to a PC with USB cable.
   USB control is recognized as HID (Human Interface Device) on PC.
   When it is not recognized properly, please reconnect the evaluation board to PC.

3. Insert the CD-ROM labeled “AKD4712-A Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon “akd4712-A.exe” to open the control program.

5. Begin evaluation by following the procedure below.

[Supported OS]
Windows 2000 / XP
64bit OS is not supported.
Windows 95 / 98 / Me / NT are not supported.

■ Operation Screen

1. Start up the control program following the above procedure.
2. After power is supplied to the evaluation board, AK4712 must be reset once by bringing SW2 (AK4712-PDN) from "L" to "H".
3. The control program operation screen is shown below

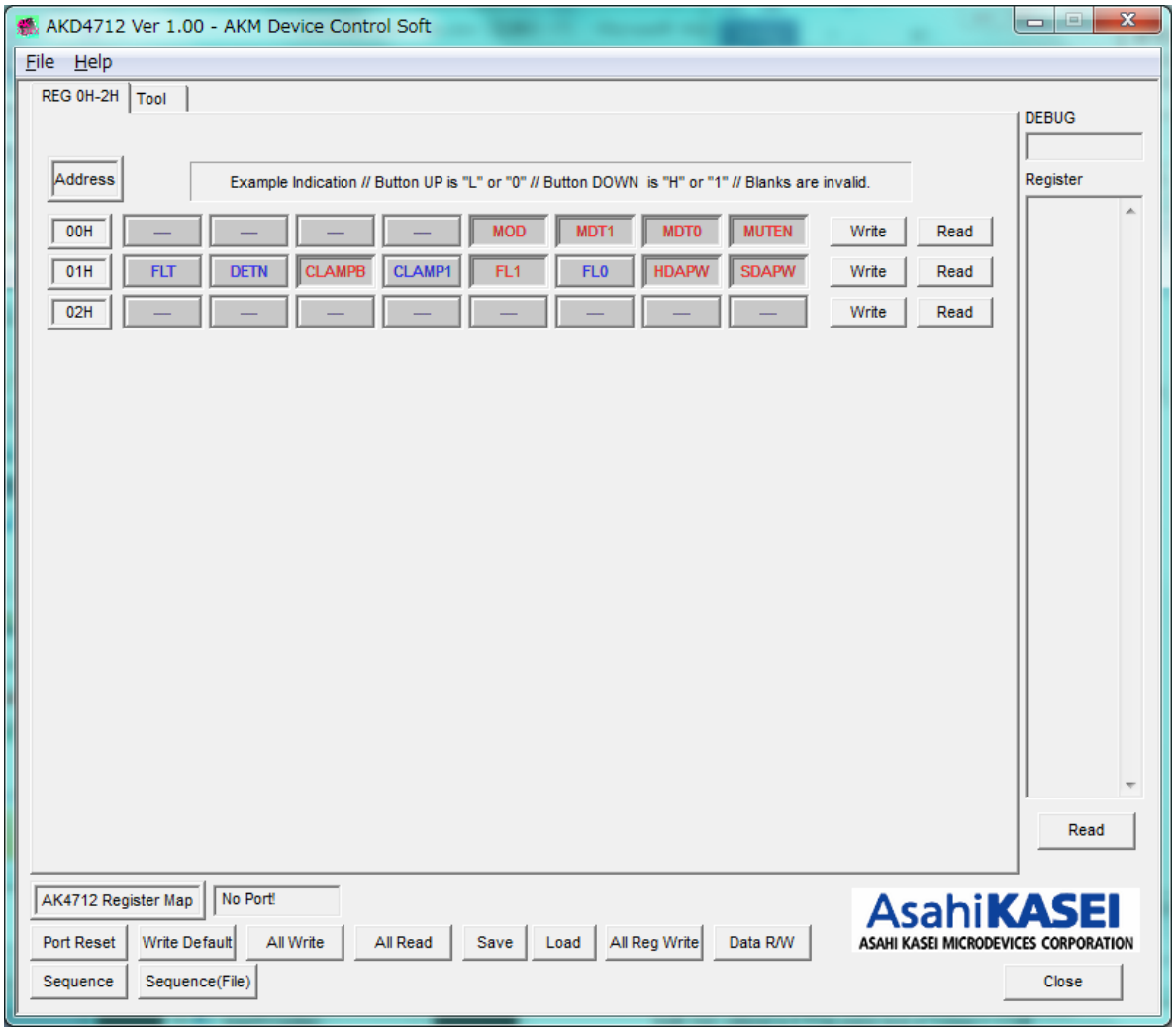


Figure 2. Control program window

■ Operation Overview

Register map and testing are controlled by this control software. These controls may be selected by the upper tabs.

Frequently used buttons, such as the register initializing button "Write Default", are located outside of the switching tab window. Refer to the "■ Dialog Box" section for details of each dialog box setting.

■ Button Functions

1. [Port Reset]: Reset connection to PC
   Click this button after the control software starts up and the evaluation board is connected to the PC via USB cable.

2. [Write Default]: Register Initialization

Use this button to initialize the registers when the device is reset by a hardware reset.

3. [All Write]: Execute write command for all registers displayed.

4. [All Read]: Execute read command for all registers displayed.

5. [Save]: Save current register settings to a file.

6. [Load]: Execute data write from a saved file.

7. [All Reg Write]: [All Reg Write] dialog box pops up.

8. [Data R/W]: [Data R/W] dialog box pops up.

9. [Read]: Read current register settings and display to the Register area (on the right of the main window).
This is different from [All Read] button as it does not reflect to the register map. It only displays the current register values in hexadecimal numbers.

■ Tab Functions

1. [REG]: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is shown in red (when read-only the name is shown in dark red).
Button Up indicates “L” or “0” and the bit name is shown in blue (when read-only the name is shown in gray)

Grayed out registers are Read-Only registers. They can not be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

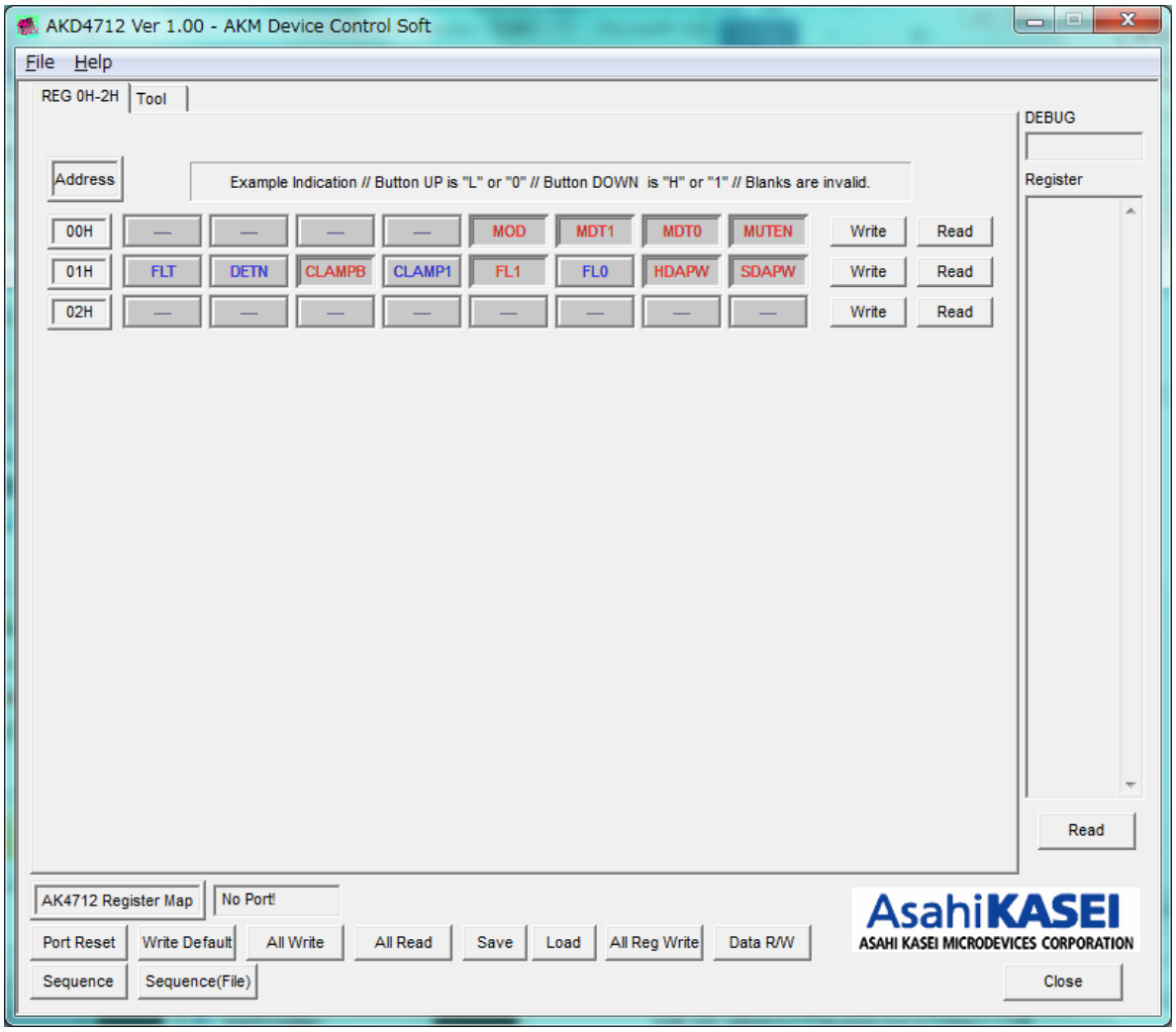


Figure 3. [REG] window

1-1. [Write]: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown below.

When the checkbox next to the register is checked, the data will become “H” or “1”. When the checkbox is not checked, the data will become “L” or “0”. Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

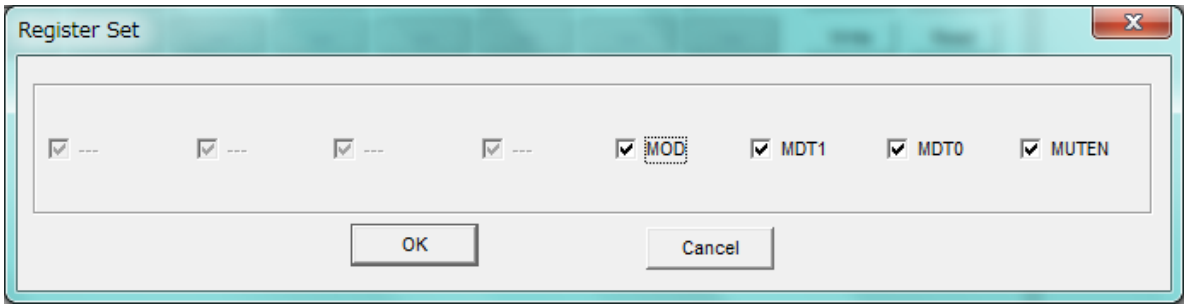


Figure 4. [Register Set] window

1-2. [Read]: Data Read

Click the [Read] button located on the right of the each corresponding address to execute a register read.

The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.

Button Down indicates “H” or “1” and the bit name is shown in red (when read only the bit name is shown in dark red).
Button Up indicates “L” or “0” and the bit name is shown in blue (when read only the bit name is shown in gray)

Please be aware that button statuses will be changed by a Read command.

2. [Tool]: Testing Tools

Evaluation testing tools are available in this tab.
Click the corresponding button for each testing tool.

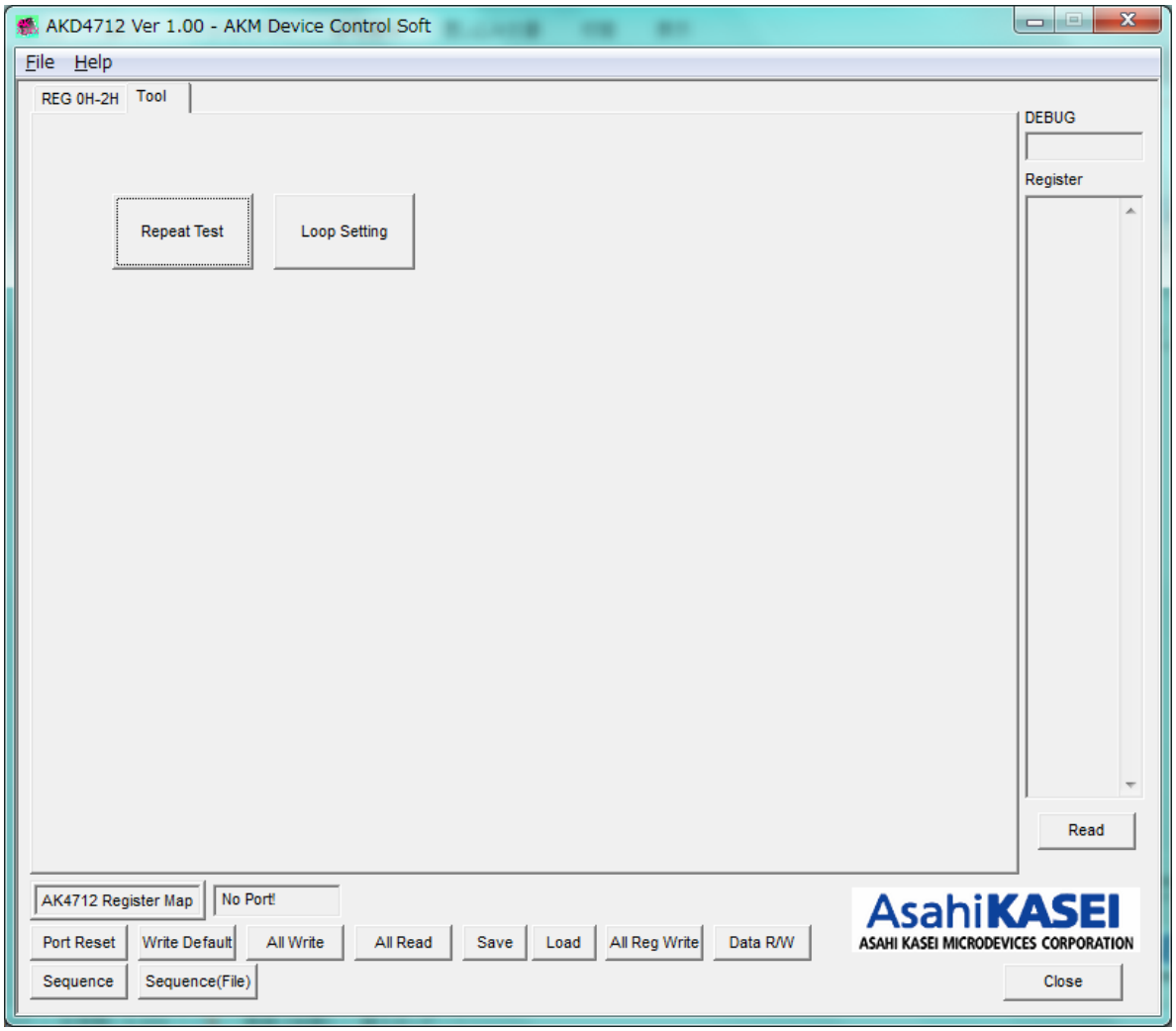


Figure 5. [Tool] window

2-1. [Repeat Test]: Repeat Test Dialog

Click the [Repeat Test] button in the Tool tab to open the repeat test dialog shown below.
A write repeat test can be executed by this dialog.

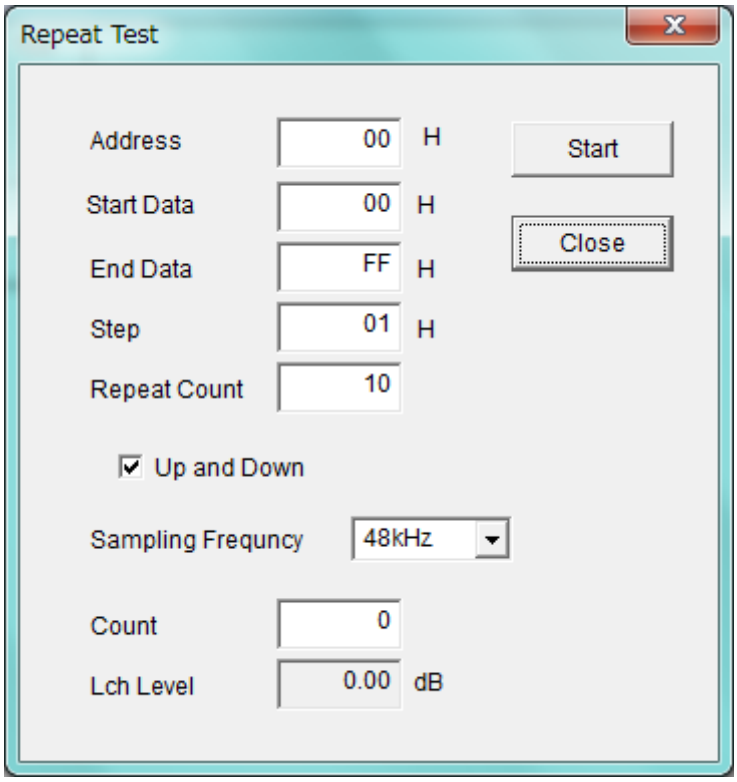


Figure 6. [Repeat Test] window

[Start] Button : Start repeat test.
A dialog for saving a file of the test result will open when this button is clicked.
Name the file.
Test will start after inserting a filename.
[Close] Button : Close dialog and finish process.
[Address] Box : Input write data address in hexadecimal numbers.
[Start Data] Box : Input start data in hexadecimal numbers.
[End Data] Box : Input end data in hexadecimal numbers.
[Step] Box : Input data write step interval.
[Repeat Count] Box : Input number of repeat cycles for the test writing.
[Up and Down] Box : Data write flow is changed as below.

- Checked: Writes in step interval from the start data to the end data and turns back at the end data to the start data.
  [Example] Start Data = 00, End Data = 05, Step = 1, [ ]…for 1 count.
  Data flow: [00→01→02→03→04→05→05→04→03→02→01→00] x Repeat Count Number

- Not checked: Writes in step interval from the start data to the end data and finishes writing.
  [Example] Start Data = 00, End Data = 05, Step = 1, [ ]…for 1 count.
  Data flow: [00→01→02→03→04→05] x Repeat Count Number

[Sampling Frequency] Box: Select sampling frequency from 44.1kHz/48kHz
[Count] Box : Indicates the count number during a repeat test.
[Lch Level] Box : Indicates the Lch Level during a repeat test.

2-2. [Loop Setting]: Loop Dialog

Click the [Loop Setting] button in the Tool tab to open the loop setting dialog shown below.
A write test can be executed.

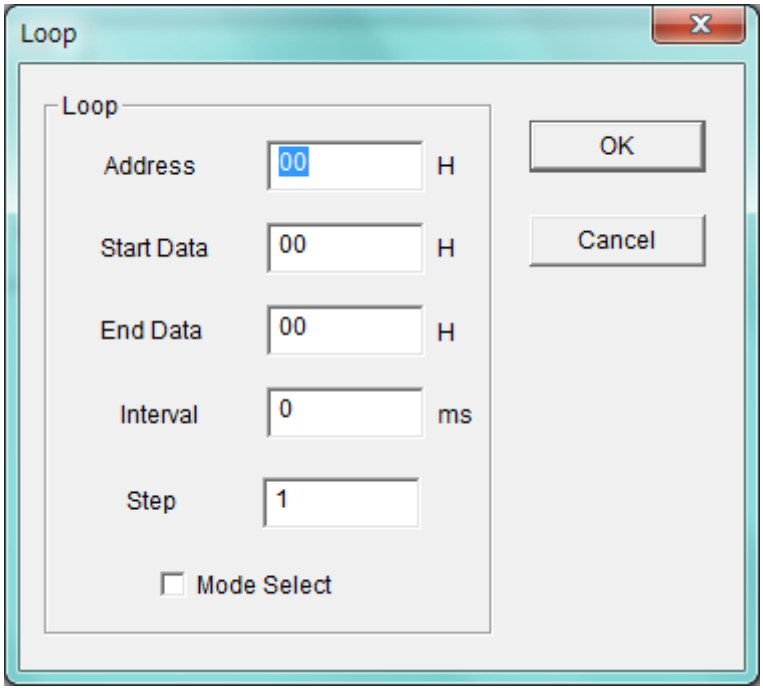


Figure 7. [Loop] window

[OK] Button : Start loop test.
[Cancel] Button : Close dialog and finish process.
[Address] Box : Input data write address in hexadecimal numbers.
[Start Data] Box : Input start data in hexadecimal numbers.
[End Data] Box : Input end data in hexadecimal numbers.
[Interval] Box : Input data write interval time.
[Step] Box : Input data write step interval.
[Mode Select] Box : Mode select check box.

- Checked: Write in step interval from the start data to the end data and turn back at the end data to start data.
  [Example] Start Data = 00, End Data = 05, Step = 1
  Data flow: 00→01→02→03→04→05→05→04→03→02→01→00

- Not Checked: Write in step interval from the start data to the end data and finish write.
  [Example] Start Data = 00, End Data = 05, Step = 1
  Data flow: 00→01→02→03→04→05

■ Dialog Box

1. [All Req Write]: All Reg Write dialog box

Click [All Reg Write] button in the main window to open register setting file window shown below.
Register setting files saved by [SAVE] button may be applied.

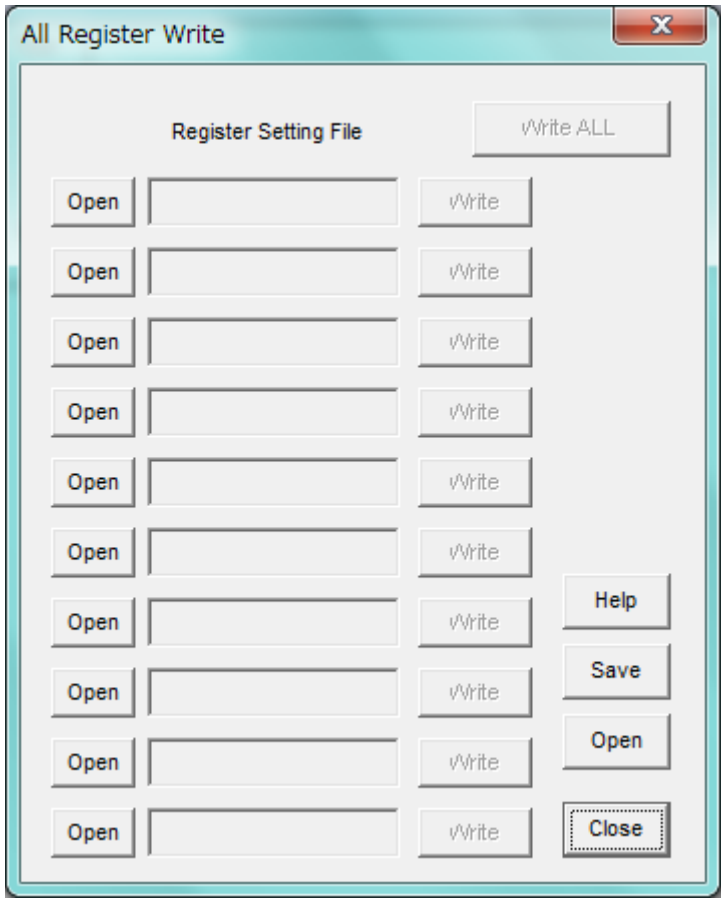


Figure 8. [All Reg Write] window

[Open (left)]: Select a register setting file (*.akr).
[Write]: Execute register write with selected setting file.
[Write All]: Execute register write with all selected setting files.
Selected files are executed in descending order.

[Help]: Open help window.
[Save]: Save register setting file assignment. File name is "*.mar".
[Open (right)]: Open saved register setting file assignment "*. mar".
[Close]: Close dialog box and finish process.

~ Operating Suggestions ~

1. Files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.
2. When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data is written to the specified address.

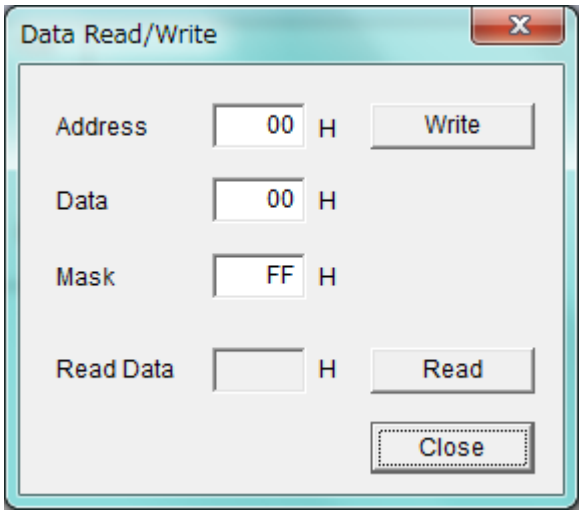


Figure 9. [Data R/W] window

[Address] Box: Input data write address in hexadecimal numbers.
[Data] Box : Input write data in hexadecimal numbers.
[Mask] Box : Input mask data in hexadecimal numbers.
This value "ANDed" with the write data becomes the input data.

[Write]: Write data generated from Data and Mask value is written to the address specified in "Address" box.

[Read]: Read data from the address specified in "Address" box.
The result will be shown in the Read Data Box in hexadecimal numbers.

[Close]: Close dialog box and finish process.
Data write will not be executed unless [Write] is clicked.

*The register map will be updated after executing the [Write] or [Read] command.

MEASUREMENT RESULTS

■ Audio

[Measurement condition]
- Measurement unit : Audio Precision SYS-2722
- BW : 20Hz~20kHz
- Power Supply : +5V=5V, VD1=3.3V, VD2=3.3V, VVD=3.3V
- Interface : Input: Cannon, Output: BNC
- Temperature : Room
- Volume Gain : 0dB
- Measurement signal line path: AINL/AINR → TVOUTL/TVOUTR

Parameter	Input signal	Measurement filter	Results Lch [dB]	Results Rch [dB]
S/(N+D) (At 2Vrms Output)	1kHz, 0dBFS	20kLPF	104.2	104.6
DR	1kHz, -60dBFS	22kLPF, A-weighted	109.2	109.1
S/N	No input	22kLPF, A-weighted	109.2	109.1

Plots

Figure 1-1. FFT (1kHz, 0dBFS input) at 2Vrms output
Figure 1-2. FFT (1kHz, -60dBFS input)
Figure 1-3. FFT (Noise floor)
Figure 1-4. THD+N vs. Input Level (fin=1kHz)
Figure 1-5. THD+N vs. fin (Input Level=0dBFS)
Figure 1-6. Linearity (fin=1kHz)
Figure 1-7. Frequency Response (Input Level=0dBFS)
Figure 1-8. Crosstalk (Input Level=0dBFS)

■ Video

[Measurement condition]
- Signal Generator : Sony Tectronix TG2000
- Measurement unit : Sony Tectronix VM700T
- Power Supply : +5V=5V, VD1=3.3V, VD2=3.3V, VVD=3.3V
- Interface : Input: BNC, Output: BNC
- Temperature : Room
- Measurement signal line path: S/N: ENCRCA → RCAVOUT
  DG, DP: ENCRCA → RCAVOUT

Parameter	Input Signal	Measurement Filter	Results	Unit
S/N	0% Flat Field	BW=15kHz to 5MHz Filter=Uni-Weighted	75.2	dB
DG	Modulated 5 step		Min: 0.00 Max: 1.34	%
DP	Modulated 5 step		Min: -0.04 Max: 0.16	deg.

Plots

Figure 2-1. Noise spectrum SD/HD (Input=0% Flat Field, BW=15kHz to 5MHz, Filter=Uni-Weighted)
Figure 2-2. DG, DP (Input= Modulated 5 step)

Plots (Audio)

AK4712 AINL/AINR → TVOUTL/TVOUTR: FFT: fin=1KHz, Input Level=0dB

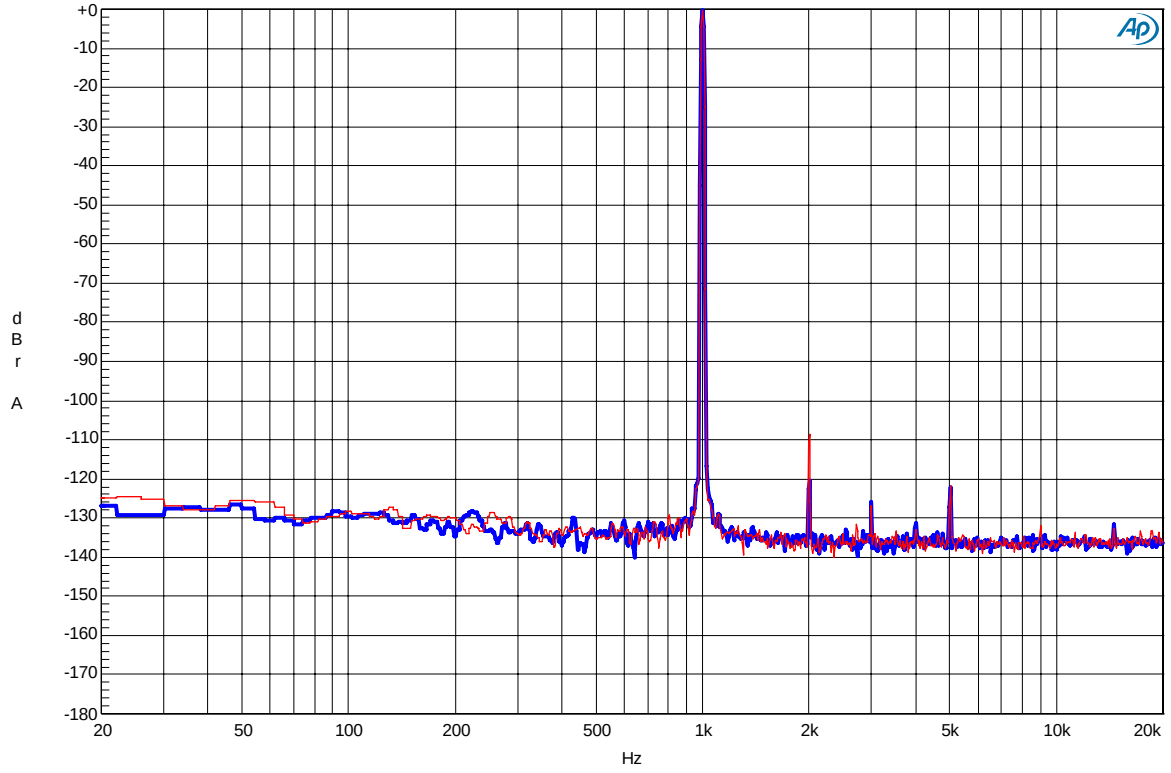


Figure 1 - 1. FFT (fin=1kHz, Input Level=0dB)

AK4712 AINL/AINR → TVOUTL/TVOUTR: FFT: fin=1KHz, Input Level=-60dB

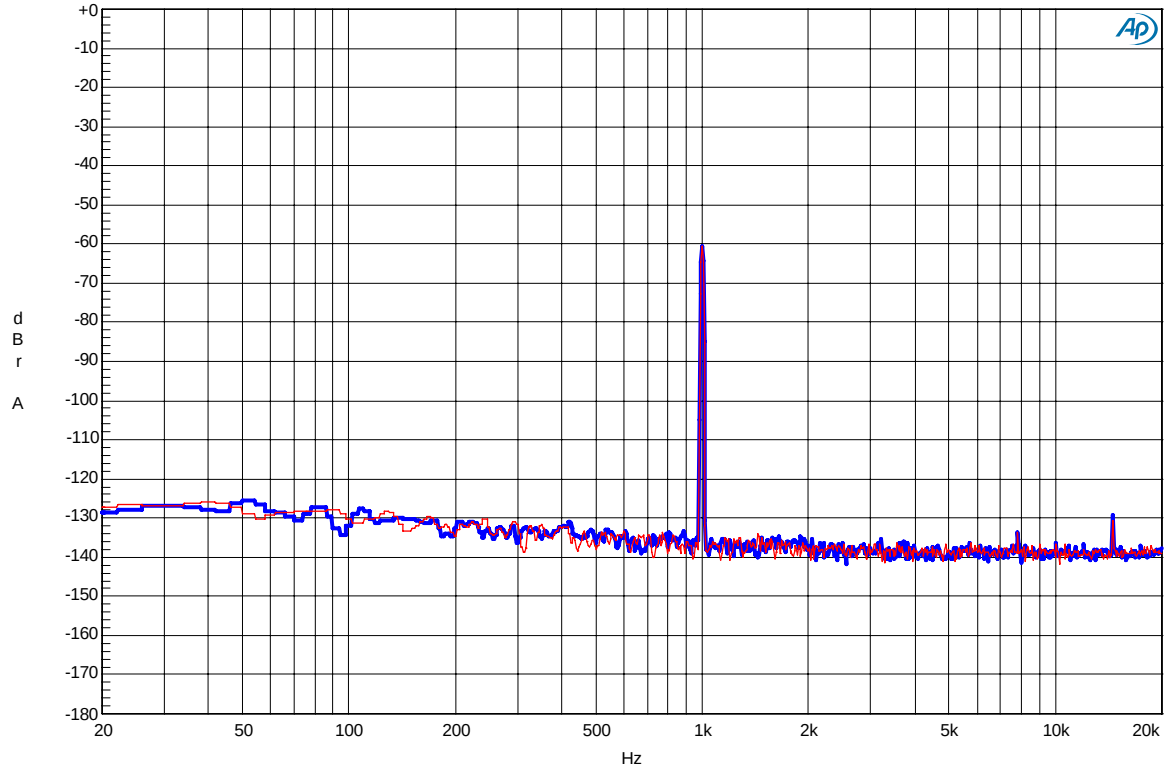


Figure 1 - 2. FFT (fin=1kHz Input Level=-60dB)

AK4712 AINL/AINR → TVOUTL/TVOUTR: FFT: No-input

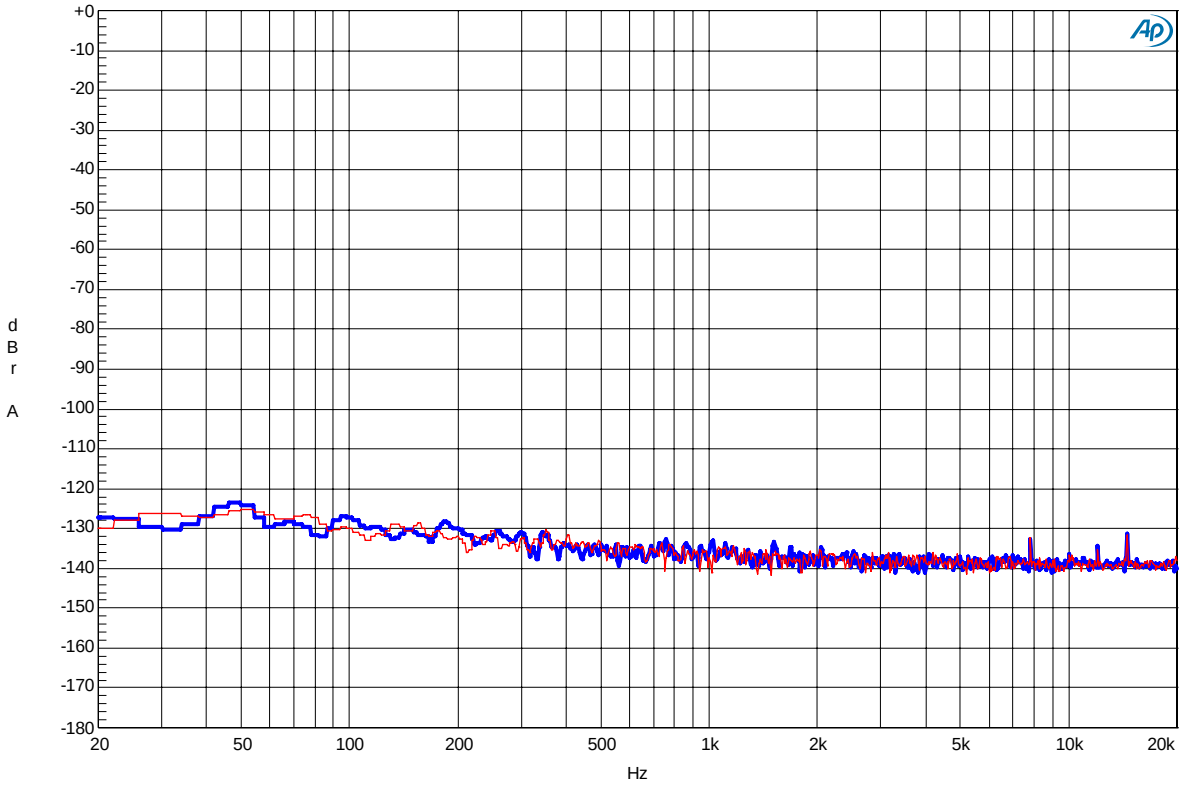


Figure 1 - 3. FFT (Noise Floor)

AK4712 AINL/AINR → TVOUTL/TVOUTR: THD+N Amplitude vs Input Amplitude: fin=1KHz

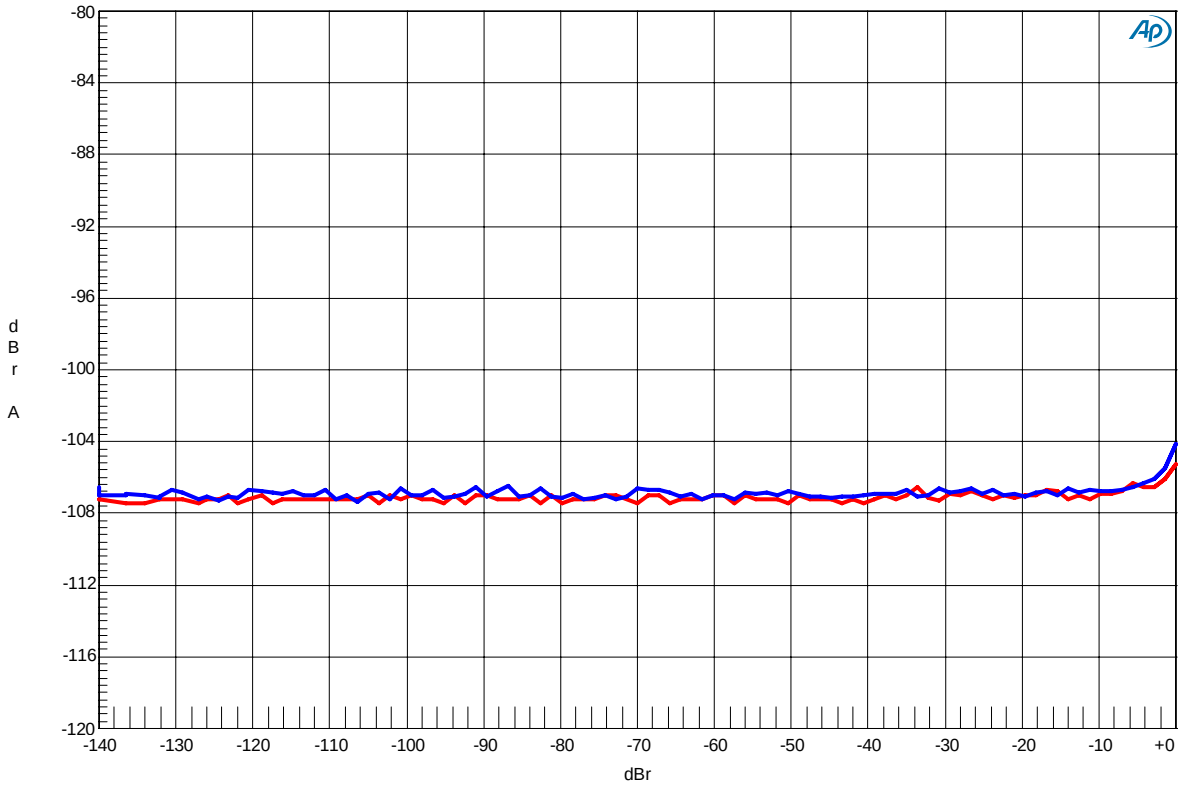


Figure 1 - 4. THD+N vs. Input level (fin=1kHz)

AK4712 AINL/AINR → TVOUTL/TVOUTR: THD+N Amplitude vs Input Frequency: Input Level=0dB

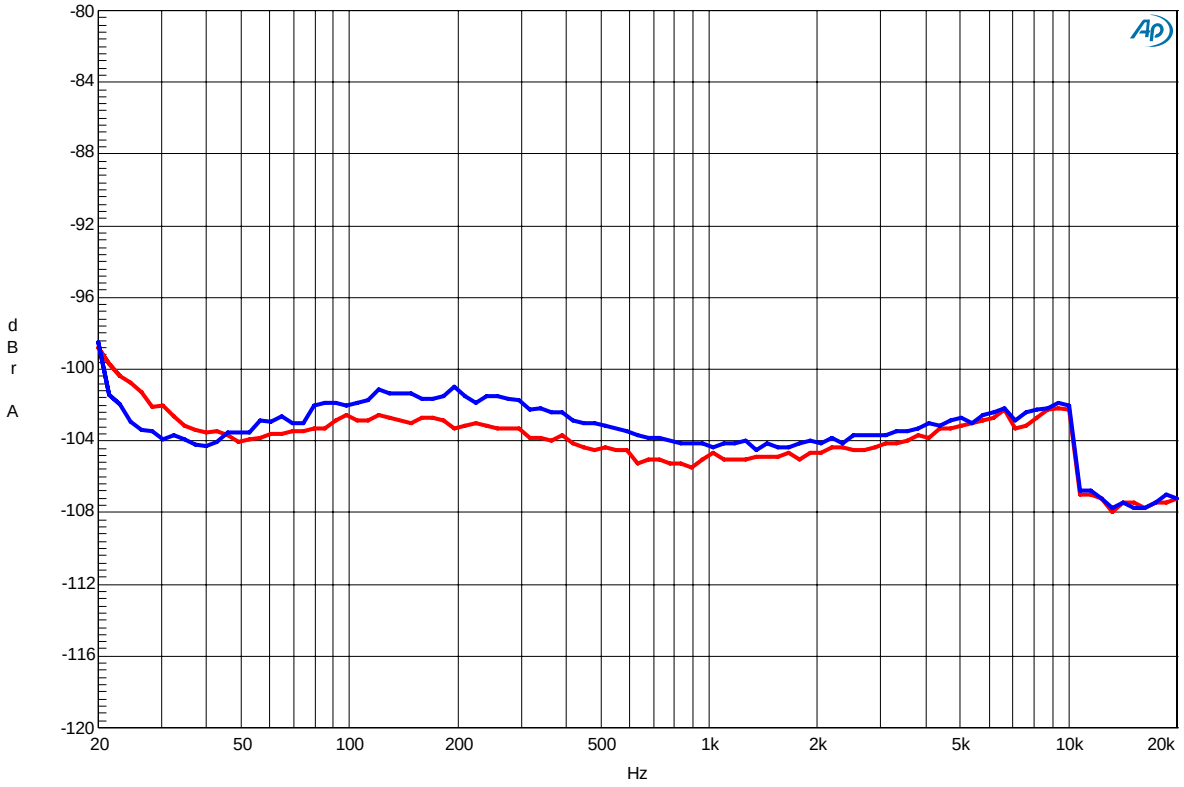


Figure 1 - 5. THD+N vs. Input Frequency (Input level=0dB)

AK4712 AINL/AINR → TVOUTL/TVOUTR: Linearity: fin=1KHz

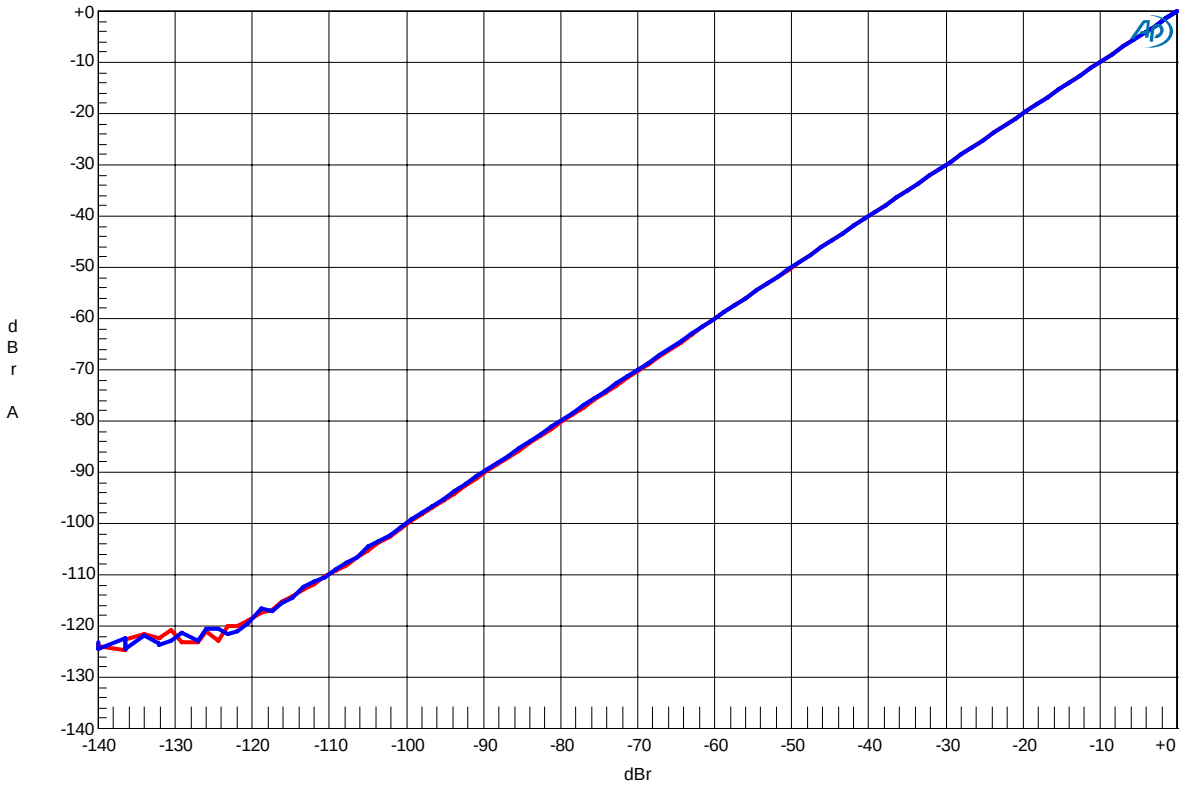


Figure 1 - 6. Linearity (fin=1kHz)

AK4712 AINL/AINR → TVOUTL/TVOUTR: Frequency Response: Input Level=0dBr

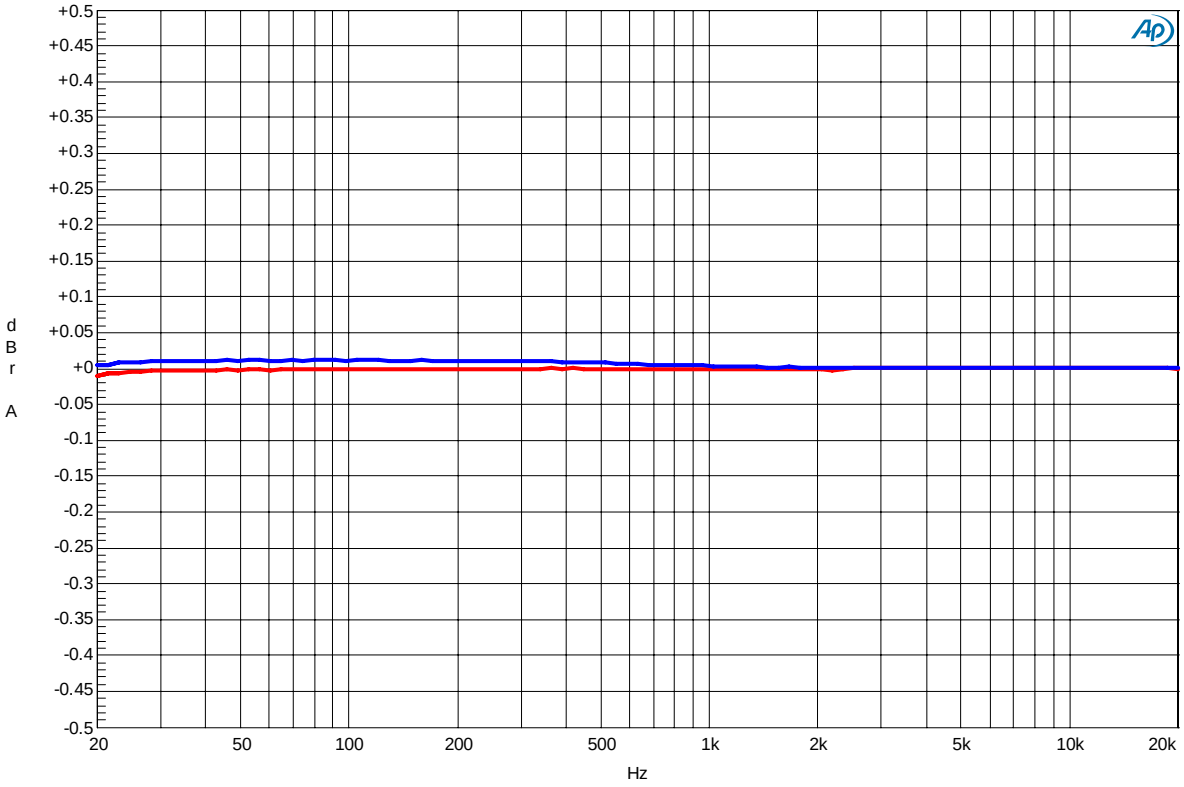


Figure 1 - 7. Frequency Response (Input level=0dB)

AK4712 AINL/AINR → TVOUTL/TVOUTR: Crosstalk: fin=1KHz, Input Level=0dBr / No-input

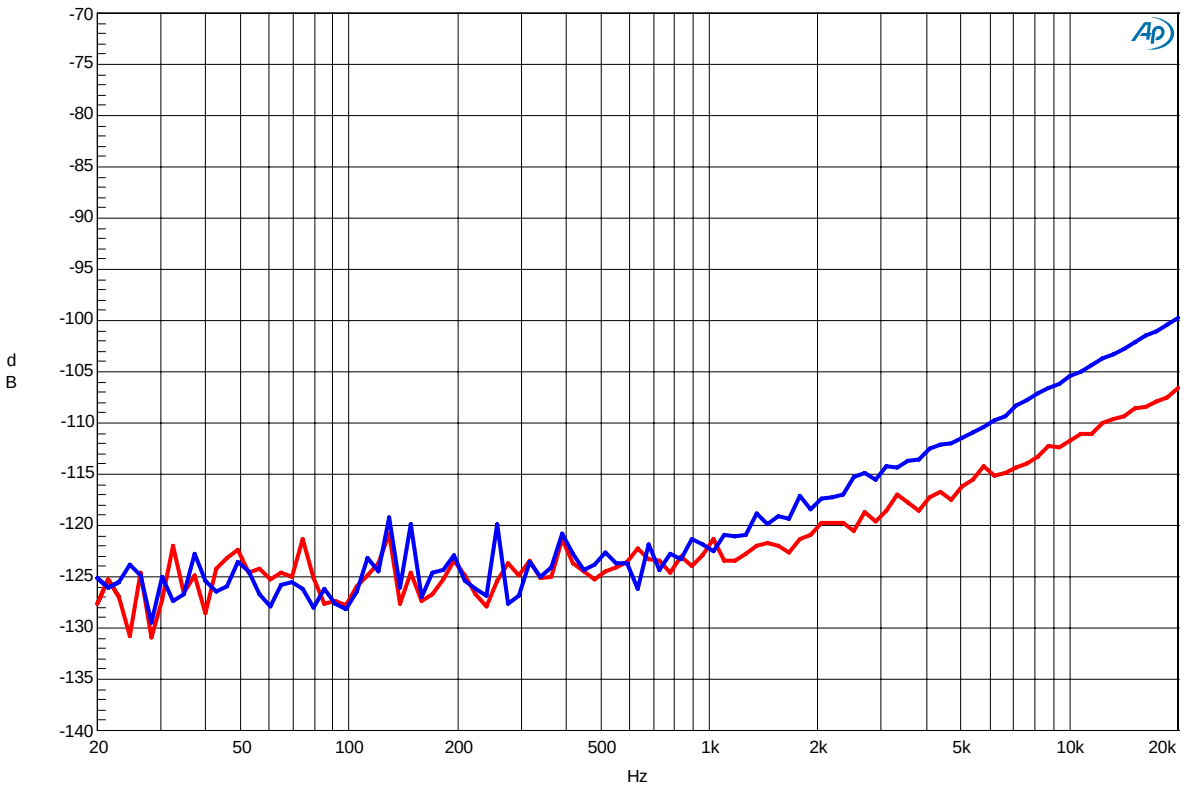


Figure 1 - 8. Crosstalk (Input level=0dB)

Plots(Video)

AK4712 ENCV → TVOUT: S/N: Input Signal=0% Flat Field, BW=15kHz to 5MHz, Filter=Uni-Weighted

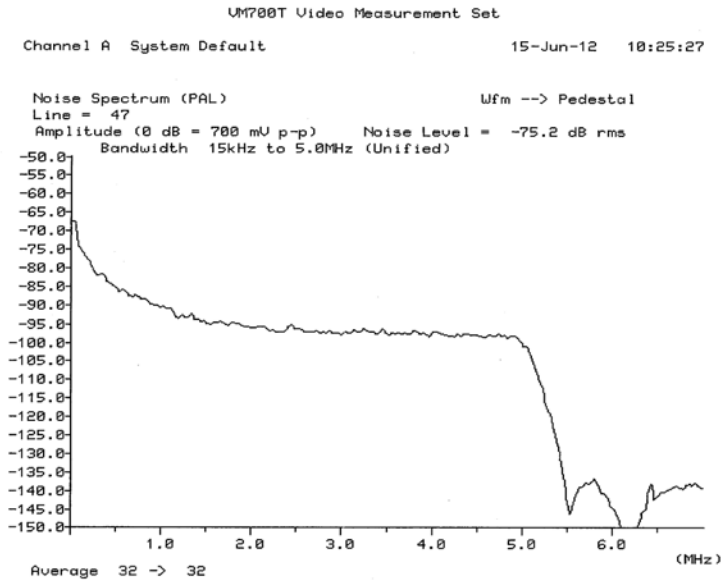


Figure 2 - 1a. RCAVOUT Noise spectrum (Input=0% Flat Field, BW=15kHz to 5MHz, Filter=Uni-Weighted)

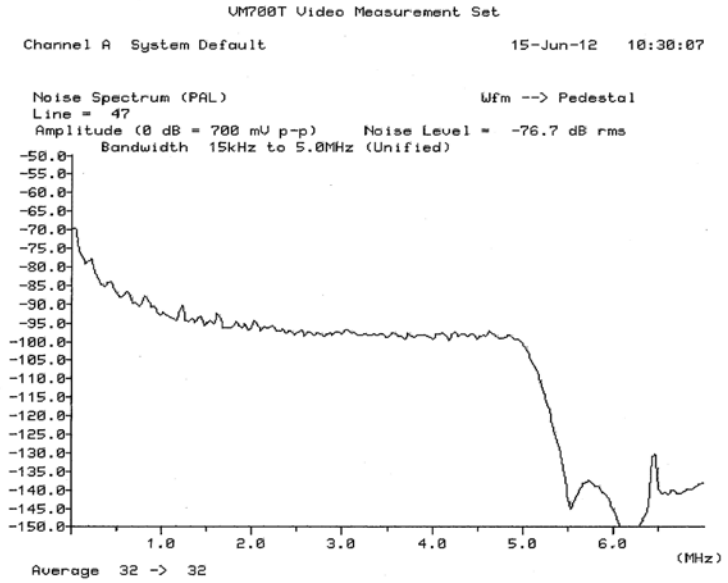


Figure 2 - 1b. HDY Noise spectrum (Input=0% Flat Field, BW=15kHz to 5MHz, Filter=Uni-Weighted)

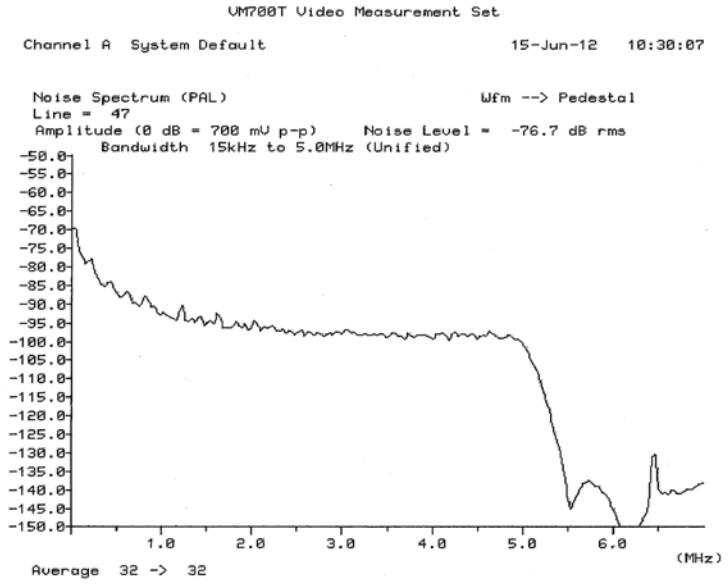


Figure 2 - 1c. HDPr Noise spectrum (Input=0% Flat Field, BW=15kHz to 5MHz, Filter=Uni-Weighted)

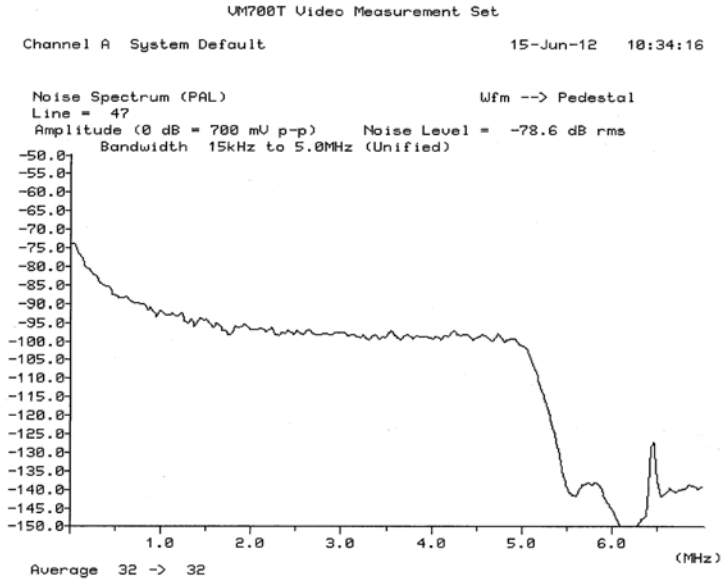


Figure 2 - 1d. HDPb Noise spectrum (Input=0% Flat Field, BW=15kHz to 5MHz, Filter=Uni-Weighted)

AK4712 ENCRCA → RCAVOUT: DG, DP: Input Signal=Modulated 5 step

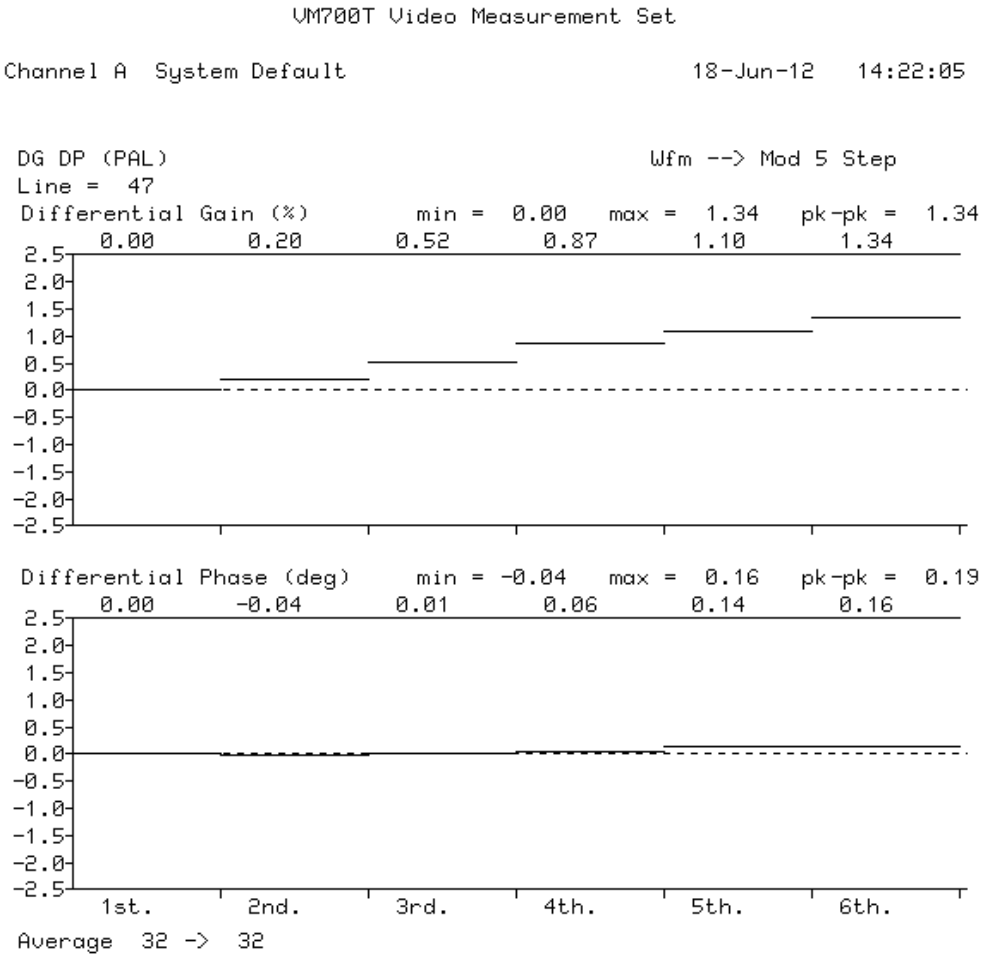


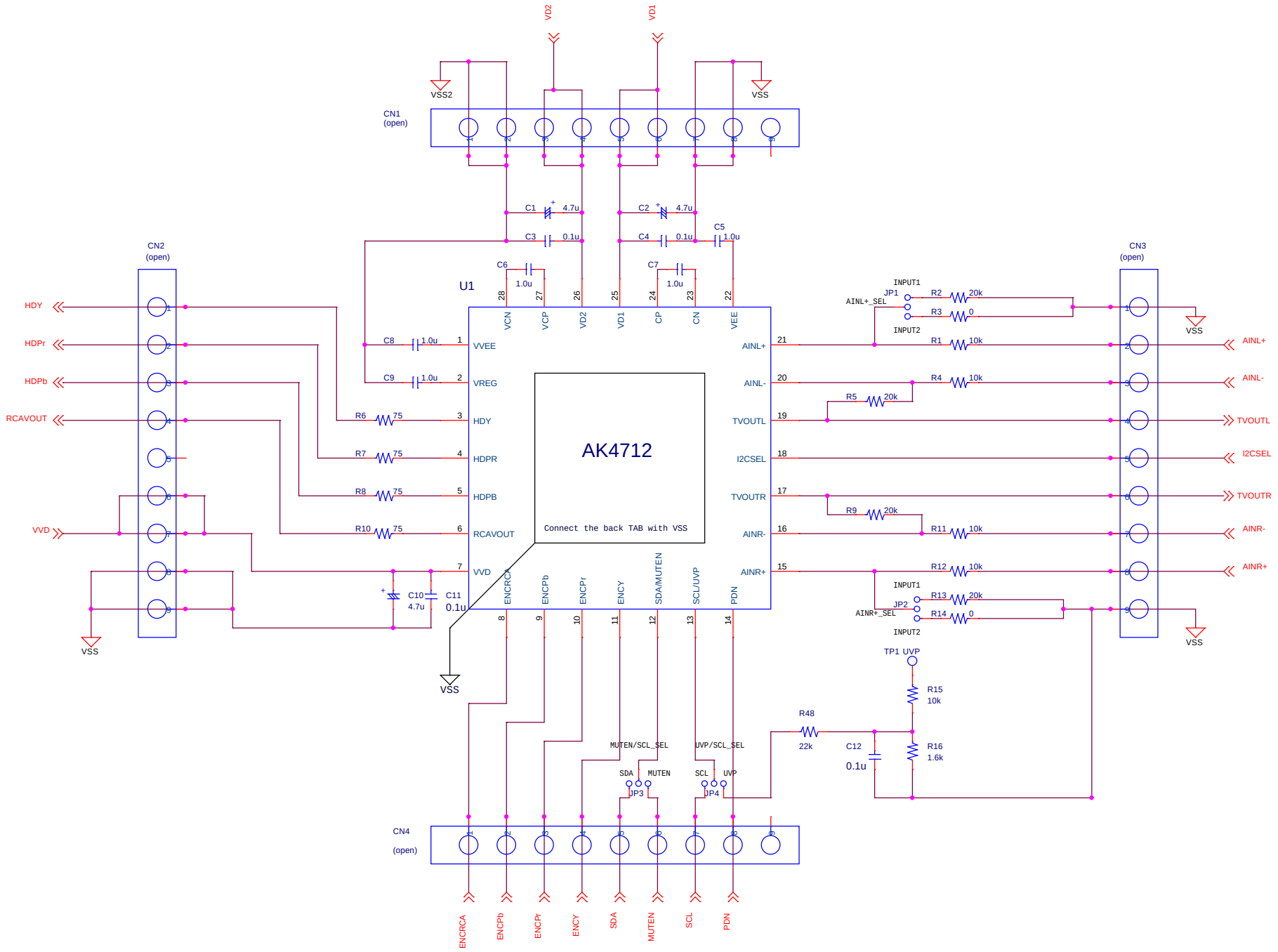
Figure 2 - 2. DG, DP (Input Signal= Modulated 5 step)

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
12/06/19	KM111300	0	First Edition	

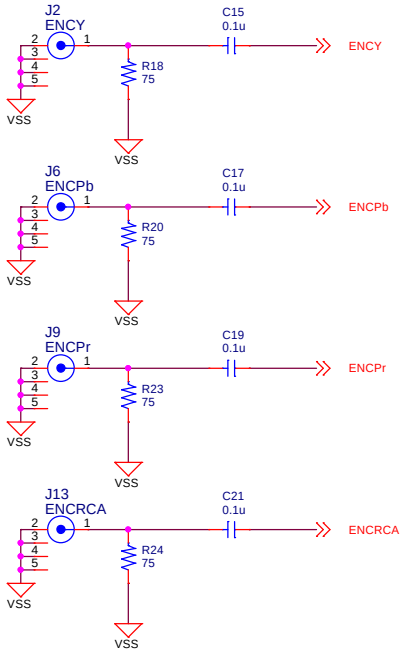
IMPORTANT NOTICE

- These products and their specifications are subject to change without notice.
  When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei Microdevices Corporation (AKM) or authorized distributors as to current status of the products.
- Descriptions of external circuits, application circuits, software and other related information contained in this document are provided only to illustrate the operation and application examples of the semiconductor products. You are fully responsible for the incorporation of these external circuits, application circuits, software and other related information in the design of your equipments. AKM assumes no responsibility for any losses incurred by you or third parties arising from the use of these information herein. AKM assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of such information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components$_{Note1)}$ in any safety, life support, or other hazard related device or system$_{Note2)}$, and AKM assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKM. As used here:
  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKM products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.

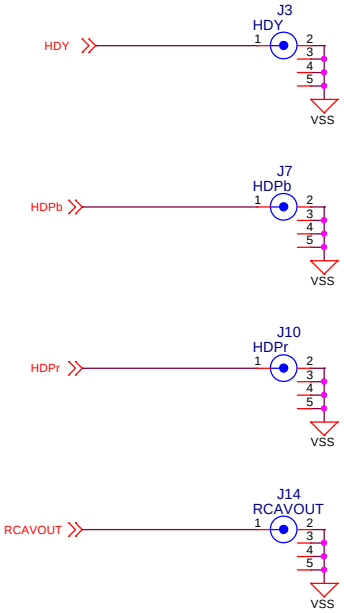


Title	AKD4712-A	
Size A3	Document Number AK4712	Rev 0
Date: Thursday, June 14, 2012	Sheet 1 of 4	

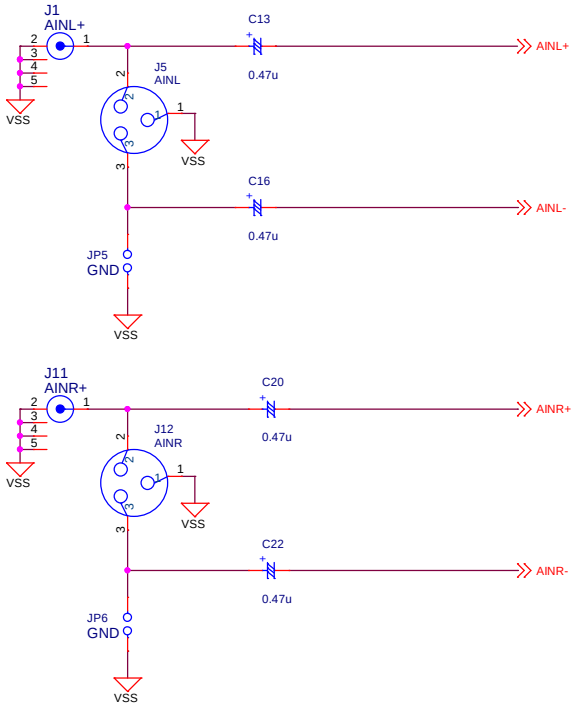
Video Intput



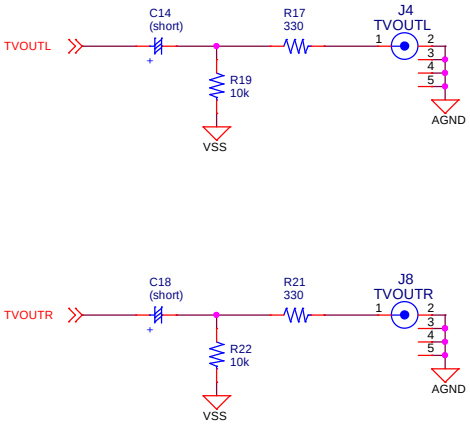
Video Output



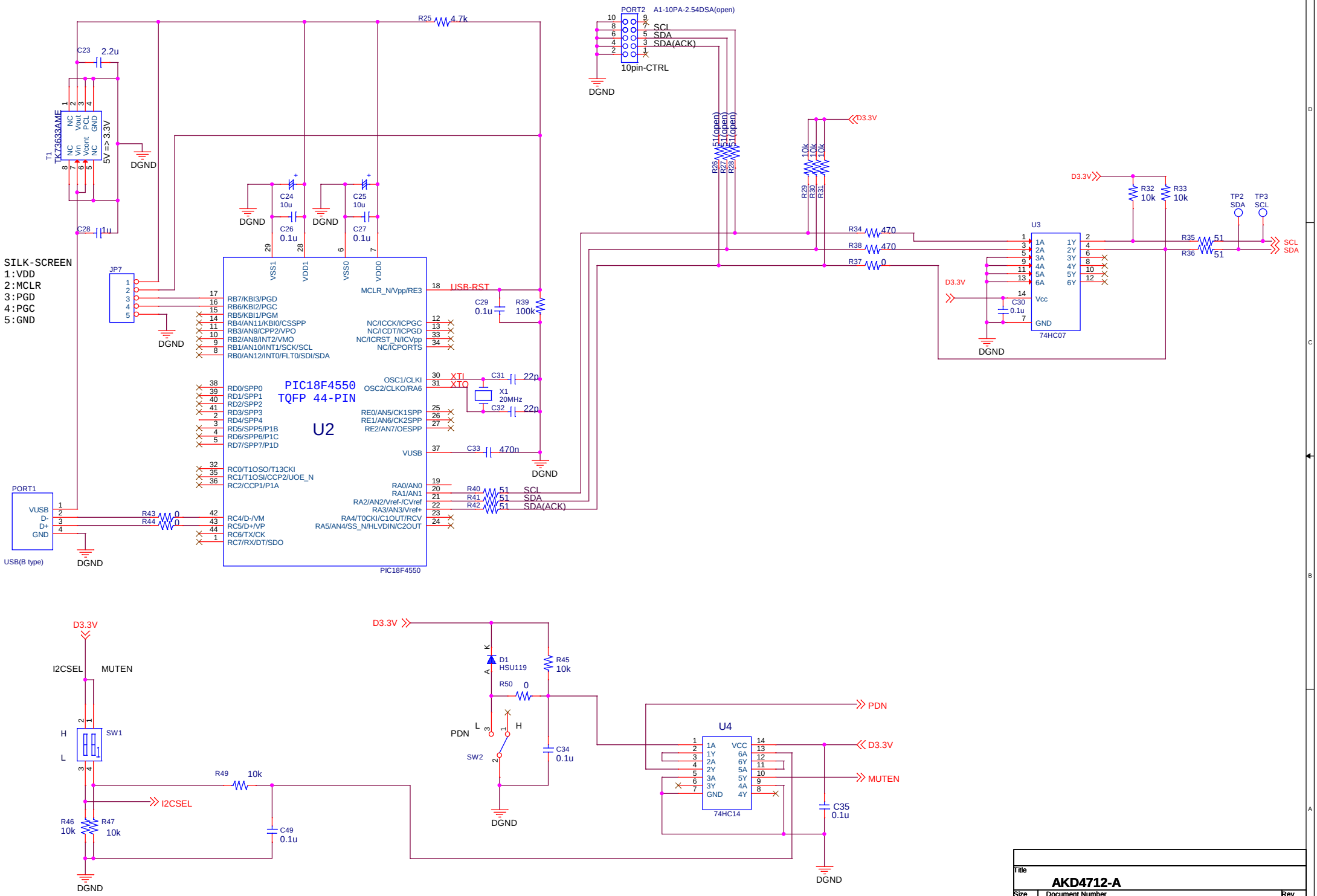
Audio Intput

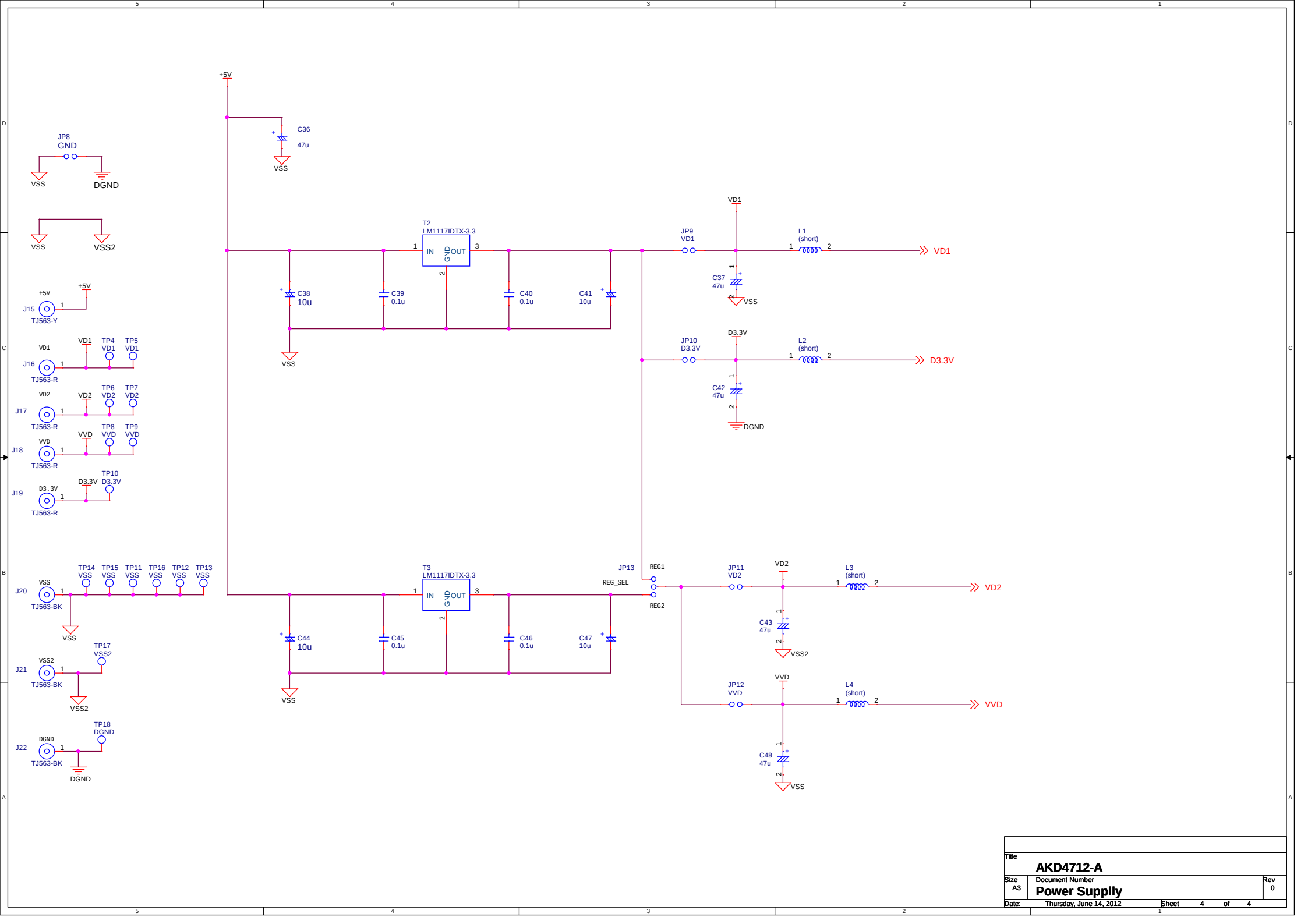


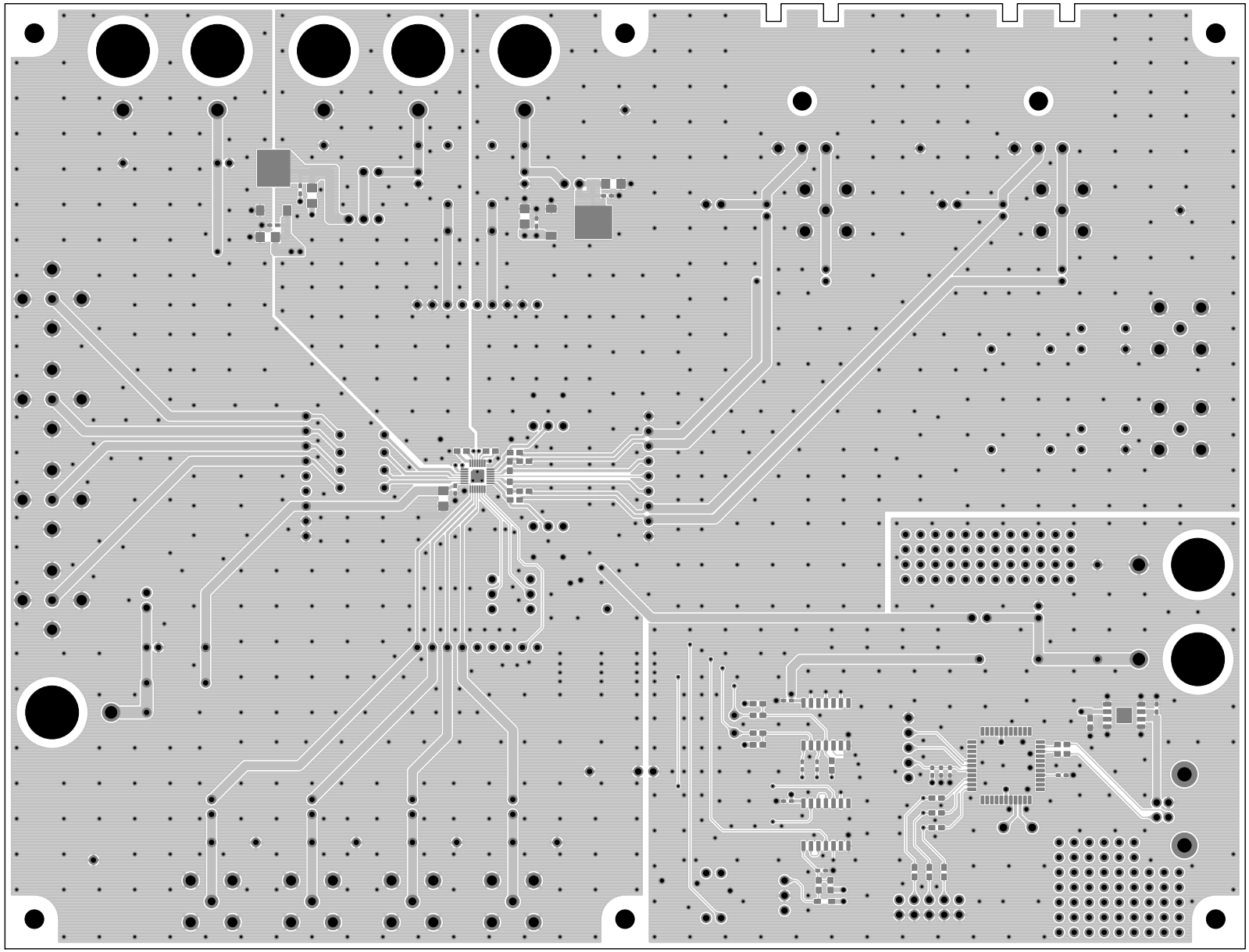
Audio Output



Title	AKD4712-A	
Size: A3	Document Number: Audio Video Input / Output	Rev: 0
Date: Thursday, June 14, 2012	Sheet 2 of 4	

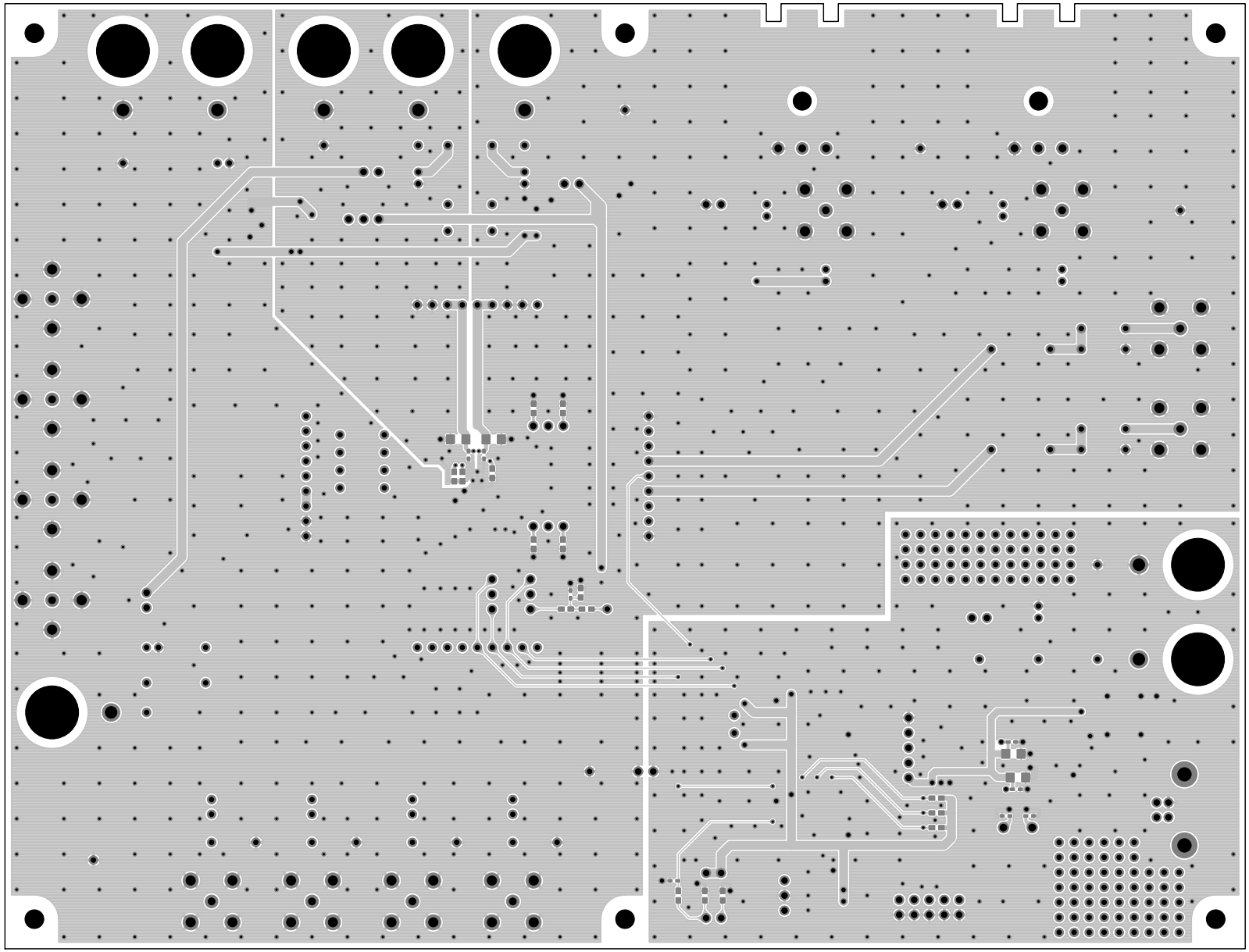

R25 4.7k
C23 2.2u
T1 TK73633AME
5V => 3.3V
C28 1u
DGND
C24 10u
C26 0.1u
C25 10u
C27 0.1u
SILK-SCREEN
1:VDD
2:MCLR
3:PGD
4:PGC
5:GND
JP7
PIC18F4550
TQFP 44-PIN
U2
VSS1
VDD1
VSS0
VDD0
MCLR_N/Vpp/RE3
USB-RST
C29 0.1u
R39 100k
RB7/KBI3/PGD
RB6/KBI2/PGC
RB5/KBI1/PGM
RB4/AN11/KBI0/CSSPP
RB3/AN9/CPP2/VPO
RB2/AN8/INT2/VMO
RB1/AN10/INT1/SCK/SCL
RB0/AN12/INT0/FLT0/SDI/SDA
NC/ICCK/ICPGC
NC/ICDT/ICPGD
NC/ICRST_N/ICVpp
NC/ICPORTS
OSC1/CLKI
OSC2/CLKO/RA6
XTI
XTO
X1 20MHz
C31 22p
C32 22p
RE0/AN5/CK1SPP
RE1/AN6/CK2SPP
RE2/AN7/OESPP
VUSB
C33 470n
RD0/SPP0
RD1/SPP1
RD2/SPP2
RD3/SPP3
RD4/SPP4
RD5/SPP5/P1B
RD6/SPP6/P1C
RD7/SPP7/P1D
RC0/T1OSO/T13CKI
RC1/T1OSI/CCP2/UOE_N
RC2/CCP1/P1A
RA0/AN0
RA1/AN1
RA2/AN2/Vref-/CVref
RA3/AN3/Vref+
RA4/T0CKI/C1OUT/RCV
RA5/AN4/SS_N/HLVDIN/C2OUT
RC4/D-/VM
RC5/D+/VP
RC6/TX/CK
RC7/RX/DT/SDO
PIC18F4550
PORT1
USB(B type)
R43 0
R44 0
R40 51 SCL
R41 51 SDA
R42 51 SDA(ACK)
PORT2 A1-10PA-2.54DSA(open)
SCL
SDA
SDA(ACK)
10pin-CTRL
R26 51(open)
R27 51(open)
R28 51(open)
R29 10k
R30 10k
R31 10k
D3.3V
R34 470
R38 470
R37 0
U3
74HC07
C30 0.1u
R32 10k
R33 10k
R35 51
R36 51
TP2 SDA
TP3 SCL
SCL
SDA
I2CSEL
MUTEN
SW1
R49 10k
R46 10k
R47 10k
C49 0.1u
D1 HSU119
R45 10k
R50 0
PDN
SW2
C34 0.1u
U4
74HC14
C35 0.1u
Title
AKD4712-A
Size A3
Document Number uP-I/F
Rev 0
Date: Thursday, June 14, 2012
Sheet 3 of 4


+5V
C36
47u
VSS
JP8
GND
VSS
DGND
VSS
VSS2
T2
LM1117IDTX-3.3
IN
GND
OUT
C38
10u
C39
0.1u
C40
0.1u
C41
10u
VD1
JP9
VD1
L1
(short)
VD1
C37
47u
VSS
D3.3V
JP10
D3.3V
L2
(short)
D3.3V
C42
47u
DGND
+5V
J15
TJ563-Y
VD1
TP4
VD1
TP5
VD1
J16
TJ563-R
VD2
TP6
VD2
TP7
VD2
J17
TJ563-R
VVD
TP8
VVD
TP9
VVD
J18
TJ563-R
TP10
D3.3V
D3.3V
J19
TJ563-R
TP14
VSS
TP15
VSS
TP11
VSS
TP16
VSS
TP12
VSS
TP13
VSS
J20
TJ563-BK
VSS
TP17
VSS2
J21
TJ563-BK
VSS2
TP18
DGND
J22
TJ563-BK
DGND
T3
LM1117IDTX-3.3
C44
10u
C45
0.1u
C46
0.1u
C47
10u
JP13
REG_SEL
REG1
REG2
JP11
VD2
VD2
L3
(short)
VD2
C43
47u
VSS2
JP12
VVD
VVD
L4
(short)
VVD
C48
47u
VSS
Title
AKD4712-A
Size
A3
Document Number
Power Supplly
Rev
0
Date:
Thursday, June 14, 2012
Sheet
4
of
4



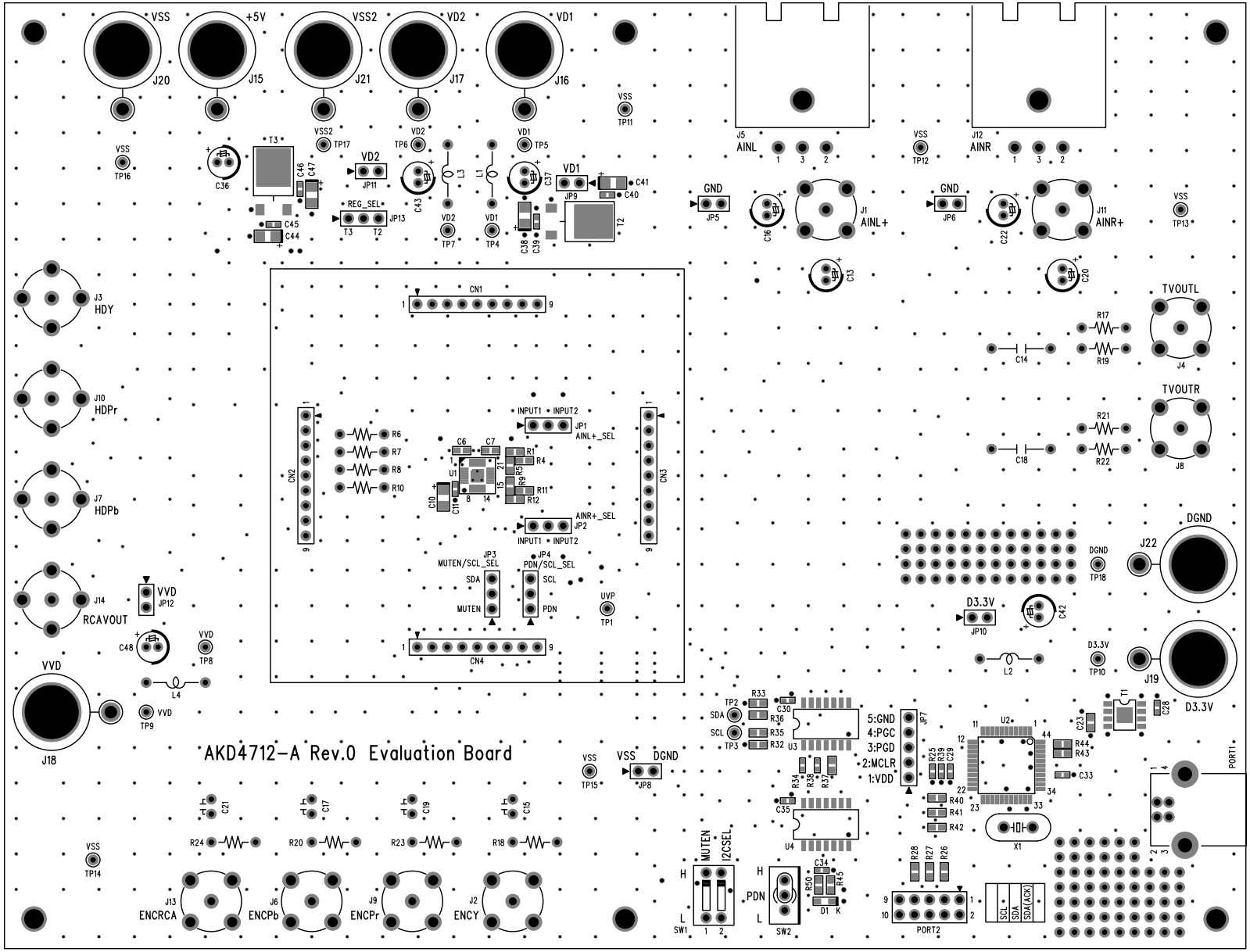
AKD4712-A-MAIN
2012.4.24

Lay1



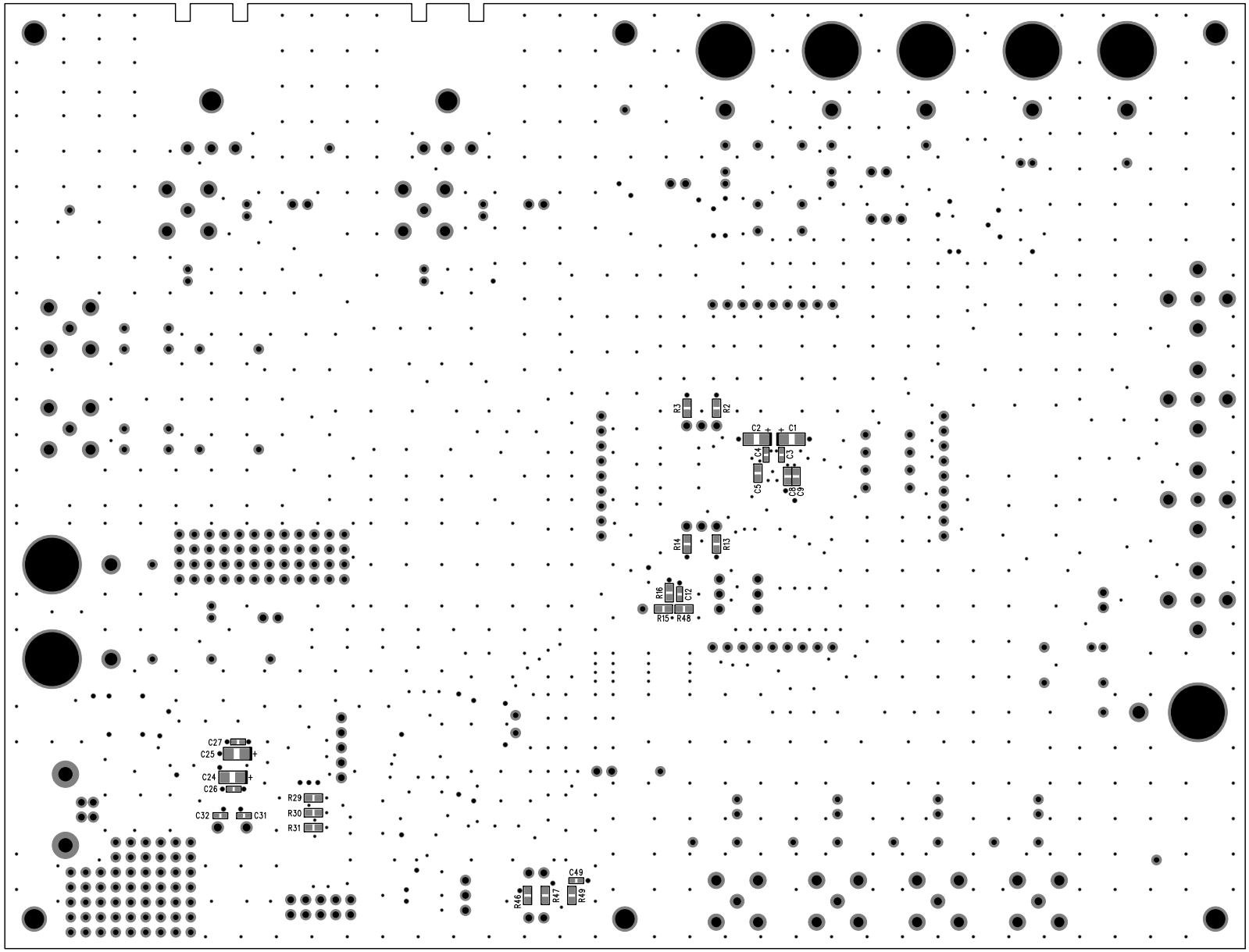
AKD4712-A-MAIN
2012.4.24

Layer2



AKD4712-A-MAIN
2012.4.24

Silk1 Resist1



Silk2 Resist2

AKD4712-A-MAIN
2012.4.24