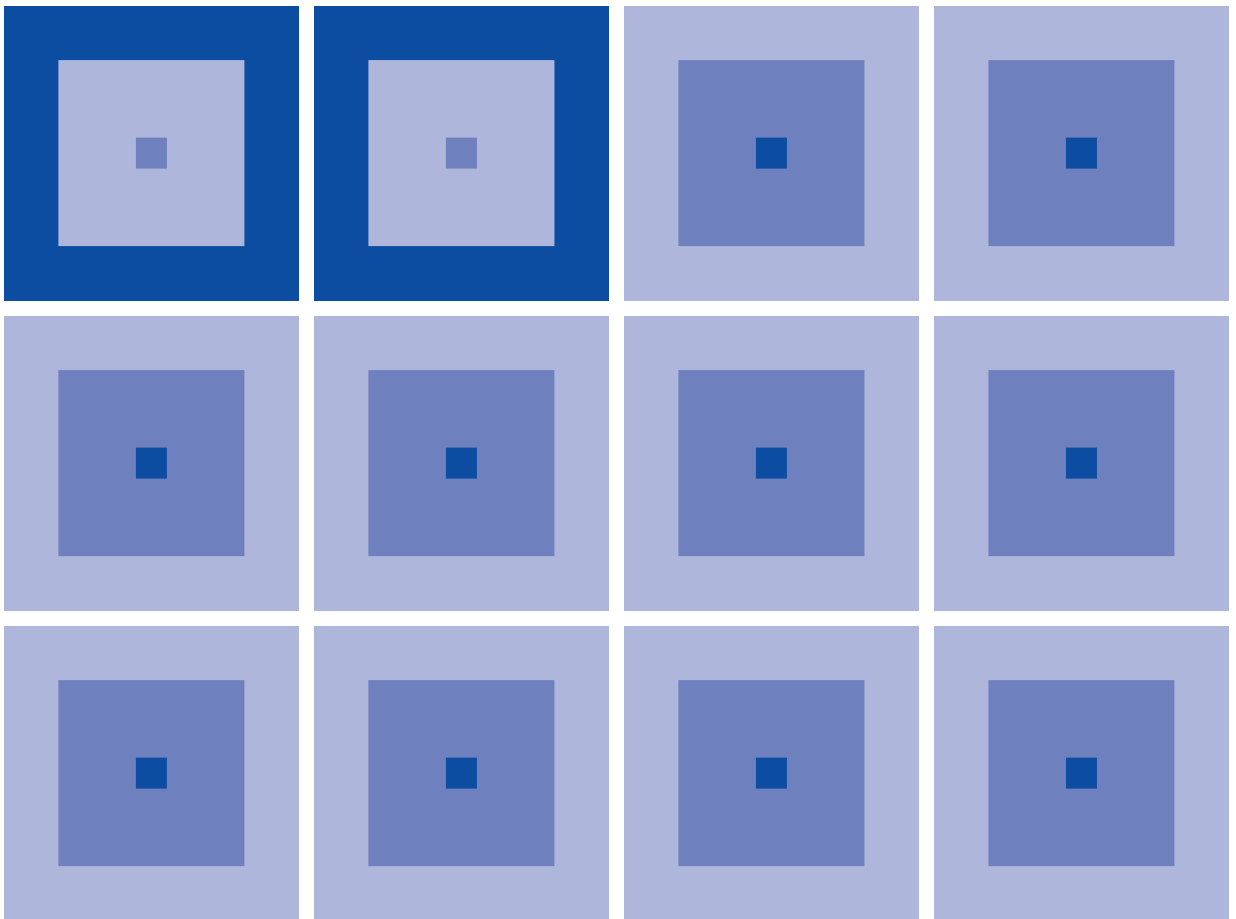


CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C60N02

Technical Manual

S1C60N02 Technical Hardware



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Revisions and Additions for this manual

| Chapter | Section | Page | Item | Contents |
|------------|------------|------|-----------------------------|--|
| Appendices | Appendix B | 88 | A/D converter error factors | Figure B.4 and the explanation were added. |
| | Appendix C | 91 | Ratings | The table was revised. |
| | | | External dimension | The figure was revised. |

Configuration of product number

Devices

S1 C 60N01 F 0A01 00

Packing specifications

[00 : Besides tape & reel
 0A : TCP BL 2 directions
 0B : Tape & reel BACK
 0C : TCP BR 2 directions
 0D : TCP BT 2 directions
 0E : TCP BD 2 directions
 0F : Tape & reel FRONT
 0G : TCP BT 4 directions
 0H : TCP BD 4 directions
 0J : TCP SL 2 directions
 0K : TCP SR 2 directions
 0L : Tape & reel LEFT
 0M : TCP ST 2 directions
 0N : TCP SD 2 directions
 0P : TCP ST 4 directions
 0Q : TCP SD 4 directions
 0R : Tape & reel RIGHT
 99 : Specs not fixed

Specification

Package

[D: die form; F: QFP]

Model number

Model name

[C: microcomputer, digital products]

Product classification

[S1: semiconductor]

Development tools

S5U1 C 60R08 D1 1 00

Packing specifications

[00: standard packing]

Version

[1: Version 1]

Tool type

[Hx : ICE
 Ex : EVA board
 Px : Peripheral board
 Wx : Flash ROM writer for the microcomputer
 Xx : ROM writer peripheral board
 Cx : C compiler package
 Ax : Assembler package
 Dx : Utility tool by the model
 Qx : Soft simulator

Corresponding model number

[60R08: for S1C60R08]

Tool classification

[C: microcomputer use]

Product classification

[S5U1: development tool for semiconductor products]

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CHAPTER 1 INTRODUCTION

Each member of the S1C60N02 Series of single chip micro-computers feature a 4-bit S1C6200B core CPU, 1,024 words of ROM (12 bits per word), 80 words of RAM (4 bits per word), an LCD driver, 4 bits for input ports (K00–K03), 4 bits for output ports (R00–R03), one 4-bit I/O port (P00–P03), clock timer and A/D converter.

Because of their low voltage operation and low power consumption, the S1C60N02 Series are ideal for a wide range of applications.

1.1 Configuration

The S1C60N02 Series are configured as follows, depending on the supply voltage.

Table 1.1.1
Configuration of the
S1C60N02 Series

| Model | Supply voltage | Oscillation circuits |
|----------|----------------|----------------------|
| S1C60N02 | 1.8–3.5 V | Crystal or CR |
| S1C60L02 | 1.2–2.0 V | Crystal or CR |

1.2 Features

| | | |
|------------------------------|---|----------|
| Built-in oscillation circuit | Crystal or CR oscillation circuit, 32,768 Hz (typ.) | |
| Instruction set | 100 instructions | |
| ROM capacity | 1,024 words × 12 bits | |
| RAM capacity (data RAM) | 80 words × 4 bits | |
| Input port | 4 bits (Supplementary pull-down resistors may be used) | |
| Output port | 4 bits (Piezo buzzer and programmable frequency output can be driven directly by mask option) | |
| Input/output port | 4 bits | |
| LCD driver | 20 segments × 4 common duty (or 3 and 2 common duty) | |
| Timer | Clock timer | |
| A/D converter | CR oscillation type A/D converter built-in | |
| Interrupts: | | |
| External interrupt | Input port interrupt | 1 system |
| Internal interrupt | Timer interrupt | 1 system |
| | A/D converter interrupt | 1 system |
| Supply voltage | 1.5 V (1.2–2.0 V) S1C60L02 (During A/D conversion) 3.0 V (1.8–3.5 V) S1C60N02 | |
| Current consumption (typ.) | 1.0 μA (Crystal oscillation CLK = 32,768 Hz, when halted) 2.5 μA (Crystal oscillation CLK = 32,768 Hz, when executing) | |
| Supply form | QFP6-60pin (plastic) or chip | |

1.3 Block Diagram

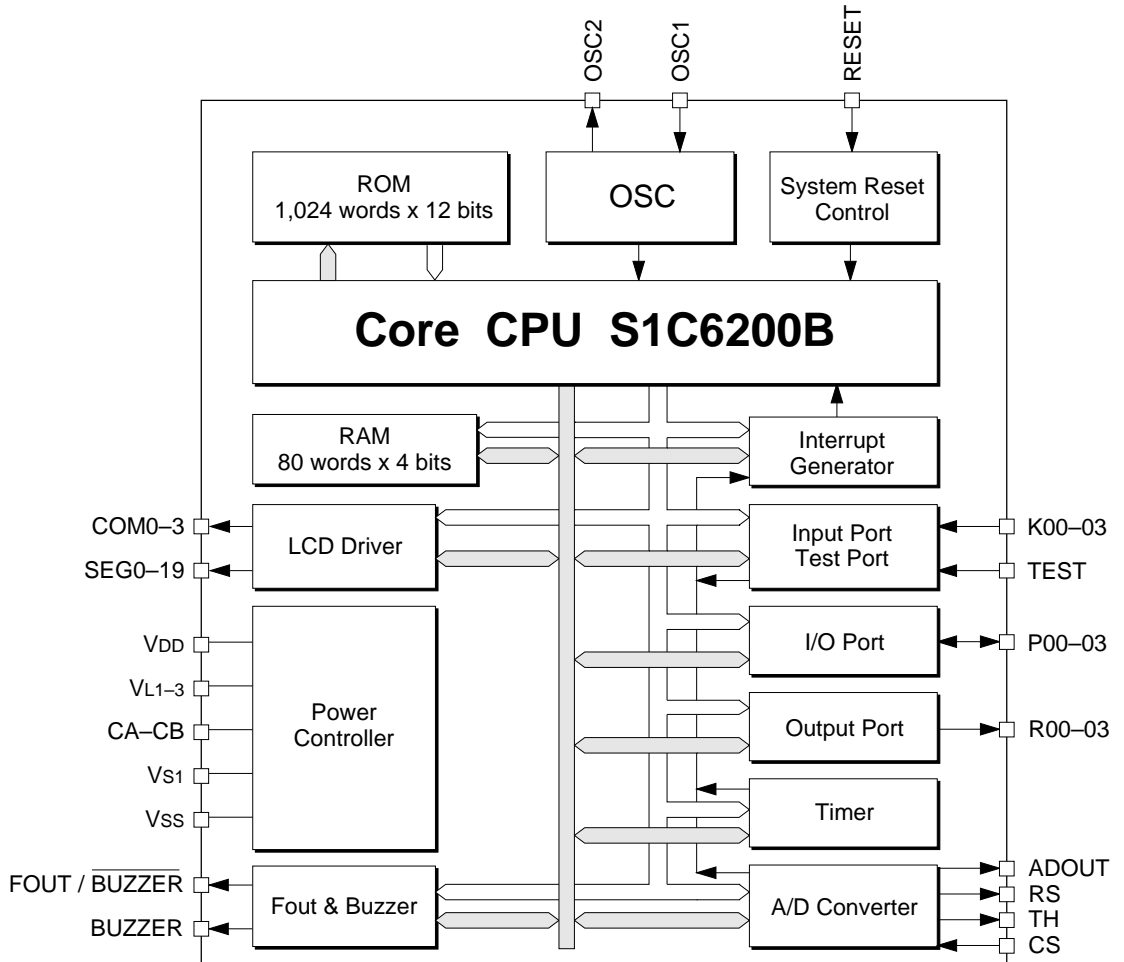
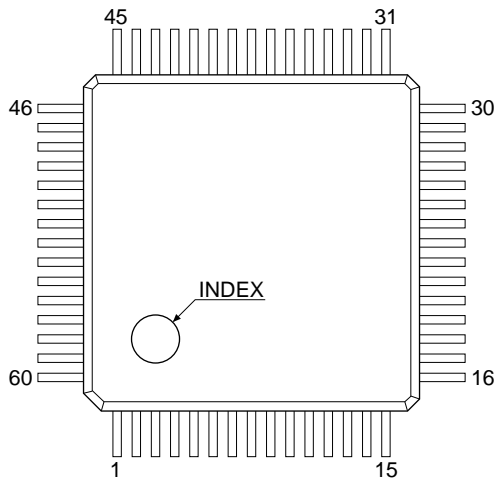


Fig. 1.3.1
Block diagram

1.4 Pin Layout Diagram

QFP6-60pin



| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | SEG0 | 16 | N.C. | 31 | N.C. | 46 | N.C. |
| 2 | SEG1 | 17 | TEST | 32 | VL3 | 47 | K00 |
| 3 | SEG2 | 18 | RESET | 33 | VL2 | 48 | K01 |
| 4 | SEG3 | 19 | SEG12 | 34 | VL1 | 49 | K02 |
| 5 | SEG4 | 20 | SEG13 | 35 | CA | 50 | K03 |
| 6 | SEG5 | 21 | SEG14 | 36 | CB | 51 | R00 |
| 7 | SEG6 | 22 | SEG15 | 37 | Vss | 52 | R01 |
| 8 | SEG7 | 23 | SEG16 | 38 | VDD | 53 | R02 |
| 9 | SEG8 | 24 | SEG17 | 39 | OSC1 | 54 | R03 |
| 10 | SEG9 | 25 | SEG18 | 40 | OSC2 | 55 | RS |
| 11 | SEG10 | 26 | SEG19 | 41 | Vs1 | 56 | TH |
| 12 | SEG11 | 27 | COM0 | 42 | P00 | 57 | CS |
| 13 | N.C. | 28 | COM1 | 43 | P01 | 58 | ADOUT |
| 14 | N.C. | 29 | COM2 | 44 | P02 | 59 | N.C. |
| 15 | N.C. | 30 | COM3 | 45 | P03 | 60 | N.C. |

N.C. = No connection

Fig. 1.4.1
Pin assignment

1.5 Pin Description

Table 1.5.1 Pin description

| Terminal name | Pin No. | Input/Output | Function |
|---------------|---------------|--------------|---|
| VDD | 38 | (I) | Power source (+) terminal |
| VSS | 37 | (I) | Power source (-) terminal |
| VS1 | 41 | O | Oscillation and internal logic system regulated voltage output terminal |
| VL1 | 34 | O | LCD system regulated voltage output terminal |
| VL2 | 33 | O | LCD system booster output terminal |
| VL3 | 32 | O | LCD system booster output terminal |
| CA, CB | 35, 36 | – | Booster capacitor connecting terminal |
| OSC1 | 39 | I | Crystal or CR oscillation input terminal |
| OSC2 | 40 | O | Crystal or CR oscillation output terminal |
| K00–K03 | 47–50 | I | Input terminal |
| P00–P03 | 42–45 | I/O | I/O terminal |
| R00–R03 | 51–54 | O | Output terminal |
| SEG0–19 | 1–12 19–26 | O | LCD segment output terminal (convertible to DC output terminal by mask option) |
| COM0–3 | 27–30 | O | LCD common output terminal |
| CS | 57 | I | A/D converter CR oscillation input terminal |
| RS | 55 | O | A/D converter CR oscillation output terminal |
| TH | 56 | O | A/D converter CR oscillation output terminal |
| ADOUT | 58 | O | A/D converter oscillation frequency output terminal |
| RESET | 18 | I | Initial setting input terminal |
| TEST | 17 | I | Test input terminal |

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (*1) supplied to VDD through VSS, the S1C60N02 Series generate the necessary internal voltages with the regulated voltage circuit (<VS1> for oscillators and internal circuit) and the voltage booster/reducer (<VL2, VL3 or VL1, VL3> for LCDs).

When the S1C60N02 LCD power is selected for 4.5 V LCD panel by mask option, the S1C60N02 short-circuits between <VL2> and <VSS> internally, and the voltage booster/reducer generates <VL1> and <VL3>. When 3.0 V LCD panel is selected, the S1C60N02 short-circuits between <VL3> and <VSS>, and the voltage reducer generates <VL1> and <VL2>. The S1C60L02 short-circuits between <VL1> and <VSS>, and the voltage booster generates <VL2> and <VL3>.

The voltage <VS1> for the internal circuit that is generated by the regulated voltage circuit is -1.2 V (VDD standard).

Figure 2.1.1 shows the power supply configuration of the S1C60N02 Series in each condition.

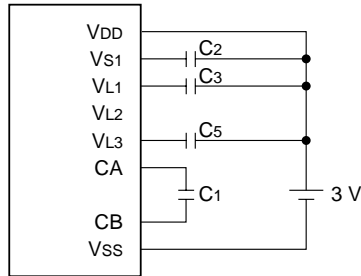
*1 Supply voltage: S1C60N02 3.0 V
S1C60L02 1.5 V

- Note*
- External loads cannot be driven by the output voltage of the regulated voltage circuit and the voltage booster/reducer.
 - See Chapter 6, "ELECTRICAL CHARACTERISTICS", for voltage values.

• **S1C60N02**

4.5 V LCD panel

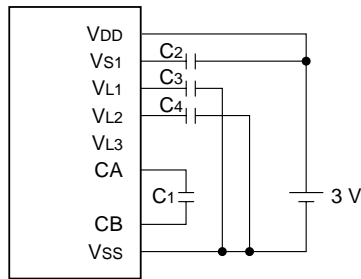
1/4, 1/3, 1/2 duty, 1/3 bias



Note: VL2 is shorted to Vss inside the IC.

3 V LCD panel

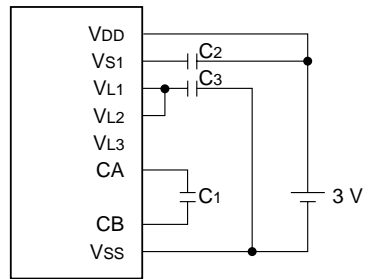
1/4, 1/3, 1/2 duty, 1/3 bias



Note: VL3 is shorted to Vss inside the IC.

3 V LCD panel

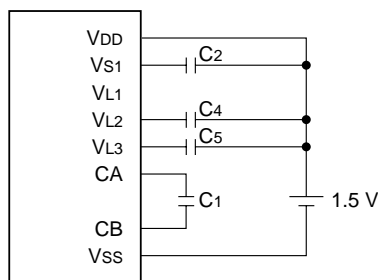
1/4, 1/3, 1/2 duty, 1/2 bias



• **S1C60L02**

4.5 V LCD panel

1/4, 1/3, 1/2 duty, 1/3 bias



Note: VL1 is shorted to Vss inside the IC.

3 V LCD panel

1/4, 1/3, 1/2 duty, 1/2 bias

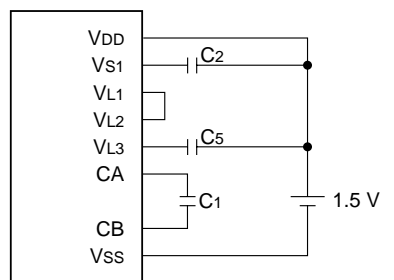


Fig. 2.1.1 External element configuration of power system

2.2 Initial Reset

To initialize the S1C60N02 Series circuits, an initial reset must be executed. There are three ways of doing this.

- (1) Initial reset by the oscillation detection circuit (*Note*)
- (2) External initial reset via the RESET pin
- (3) External initial reset by simultaneous high input to pins K00-K03 (depending on mask option)

Figure 2.2.1 shows the configuration of the initial reset circuit.

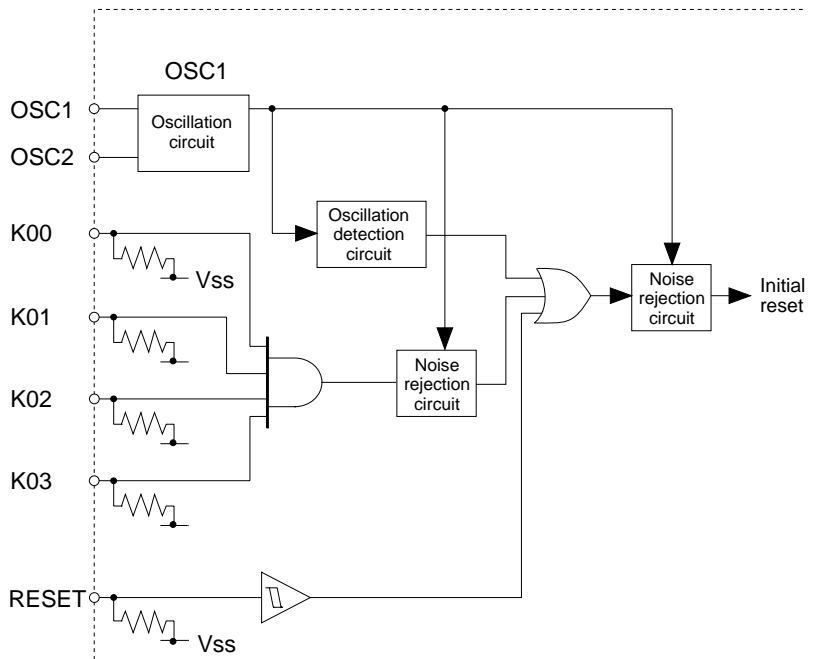


Fig. 2.2.1
Configuration of
initial reset circuit

Note Since the circuit may sometimes not operate normally with the initial resetting by the oscillation detection circuit indicated in number (1), depending on the method of making the power, you should utilize one of the initial resetting methods mentioned in numbers (2) and (3).

Oscillation detection circuit

When the oscillation circuit has been stopped until the oscillation circuit begins to oscillate when the power is turned on or for any other reason, the oscillation detection circuit will output an initial reset signal, but since the circuit may sometimes not operate normally with the initial resetting due to the oscillation detection circuit, depending on the method of making the power, you should utilize one of the initial resetting methods indicated hereafter.

Reset pin (RESET)

An initial reset can be invoked externally by making the reset pin high. This high level must be maintained for at least 5 ms (when oscillating frequency, $f_{osc} = 32$ kHz), because the initial reset circuit contains a noise rejection circuit. When the reset pin goes low the CPU begins to operate.

Simultaneous high input to input ports (K00–K03)

Another way of invoking an initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port pins must be kept high for at least 4 sec (when oscillating frequency $f_{osc} = 32$ kHz), because of the noise rejection circuit. Table 2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.1
Input port combinations

| | |
|---|-----------------|
| A | Not used |
| B | K00*K01 |
| C | K00*K01*K02 |
| D | K00*K01*K02*K03 |

When, for instance, mask option D (K00*K01*K02*K03) is selected, an initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time.

If you use this function, make sure that the specified ports do not go high at the same time during normal operation.

Internal register following initialization

An initial reset initializes the CPU as shown in the table below.

Table 2.2.2
Initial values

| CPU Core | | | |
|----------------------|--------|----------------|---------------|
| Name | Signal | Number of bits | Setting value |
| Program counter step | PCS | 8 | 00H |
| Program counter page | PCP | 4 | 1H |
| New page pointer | NPP | 4 | 1H |
| Stack pointer | SP | 8 | Undefined |
| Index register X | X | 8 | Undefined |
| Index register Y | Y | 8 | Undefined |
| Register pointer | RP | 4 | Undefined |
| General register A | A | 4 | Undefined |
| General register B | B | 4 | Undefined |
| Interrupt flag | I | 1 | 0 |
| Decimal flag | D | 1 | 0 |
| Zero flag | Z | 1 | Undefined |
| Carry flag | C | 1 | Undefined |

| Peripheral circuits | | |
|--------------------------|----------------|---------------|
| Name | Number of bits | Setting value |
| RAM | 80 × 4 | Undefined |
| Display memory | 20 × 4 | Undefined |
| Other peripheral circuit | – | *1 |

*1: See Section 4.1, "Memory Map"

2.3 Test Pin (TEST)

This pin is used when IC is inspected for shipment. During normal operation connect it to VSS.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C60N02 Series employs the S1C6200B core CPU, so that register configuration, instructions, and so forth are virtually identical to those in other processors in the family using the S1C6200B. Refer to the "S1C6200/6200A Core CPU Manual" for details of the S1C6200B.

Note the following points with regard to the S1C60N02 Series:

- (1) The SLEEP operation is not provided, so the SLP instruction cannot be used.
- (2) Because the ROM capacity is 1,024 words, 12 bits per word, bank bits are unnecessary, and PCB and NBP are not used.
- (3) The RAM page is set to 0 only, so the page part (XP, YP) of the index register that specifies addresses is invalid.

| | | | |
|------|------|------|------|
| PUSH | XP | PUSH | YP |
| POP | XP | POP | YP |
| LD | XP,r | LD | YP,r |
| LD | r,XP | LD | r,YP |

3.2 ROM

The built-in ROM, a mask ROM for the program, has a capacity of $1,024 \times 12$ -bit steps. The program area is 4 pages (0–3), each consisting of 256 steps (00H–FFH). After an initial reset, the program start address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 01H–07H.

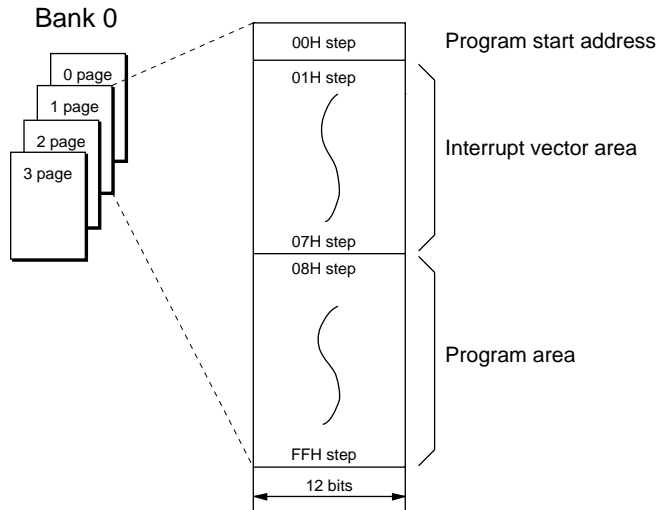


Fig. 3.2.1
ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 80 words, 4-bit words. When programming, keep the following points in mind:

- (1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.
- (2) Subroutine calls and interrupts take up three words on the stack.
- (3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the S1C60N02 Series are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the S1C60N02 Series has an address space of 154 words, of which 32 words are allocated to display memory and 26 words, to I/O memory. Figure 4.1.1 show the overall memory map for the S1C60N02 Series, and Tables 4.1.1(a) and (b), the memory maps for the peripheral circuits (I/O space).

| Address Page | Low | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|-----------------|------|---|----|-------------|----|-------------|----|-------------|----|-------------|----|-------------|----|-------------|----|-------------|----|
| | High | M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | M9 | MA | MB | MC | MD | ME | MF |
| 0 | 0 | M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | M9 | MA | MB | MC | MD | ME | MF |
| | 1 | RAM area (000H–04FH) 80 words x 4 bits (R/W) | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | |
| | 4 | | | | | | | | | | | | | | | | |
| | 5 | Unused area | | | | | | | | | | | | | | | |
| | 6 | | | | | | | | | | | | | | | | |
| | 7 | | | | | | | | | | | | | | | | |
| | 8 | | | | | | | | | | | | | | | | |
| | 9 | Display memory area (090H–0AFH) 32 words x 4 bits (Write only) | | | | | | | | | | | | | | | |
| | A | Unused area | | | | | | | | | | | | | | | |
| | B | | | | | | | | | | | | | | | | |
| | C | | | | | | | | | | | | | | | | |
| | D | | | | | | | | | | | | | | | | |
| | E | Unused area | | | | Unused area | | | | Unused area | | | | Unused area | | | |
| | F | Unused area | | Unused area | | Unused area | | Unused area | | Unused area | | Unused area | | Unused area | | Unused area | |
| | | I/O memory area Table 4.1.1(a), (b) | | | | | | | | | | | | | | | |

Fig. 4.1.1
Memory map

Unused area

Note Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Table 4.1.1(a) I/O memory map

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment | |
|---------|----------|-------|-------|-------|-------|---------|--------|------|---|----|
| | D3 | D2 | D1 | D0 | | | | | | |
| 0E0H | K03 | K02 | K01 | K00 | K03 | – *2 | High | Low | Input port data K03 | |
| | R | | | | K02 | – *2 | High | Low | Input port data K02 | |
| | | | | | K01 | – *2 | High | Low | Input port data K01 | |
| | | | | | K00 | – *2 | High | Low | Input port data K00 | |
| 0E3H | TM3 | TM2 | TM1 | TM0 | TM3 | – *3 | High | Low | Clock timer data 2 Hz | |
| | R | | | | TM2 | – *3 | High | Low | Clock timer data 4 Hz | |
| | | | | | TM1 | – *3 | High | Low | Clock timer data 8 Hz | |
| | | | | | TM0 | – *3 | High | Low | Clock timer data 16 Hz | |
| 0E4H | TC3 | TC2 | TC1 | TC0 | TC3 | – *3 | 1 | 0 | Up/down counter data TC3 | |
| | R/W | | | | TC2 | – *3 | 1 | 0 | Up/down counter data TC2 | |
| | | | | | TC1 | – *3 | 1 | 0 | Up/down counter data TC1 | |
| | | | | | TC0 | – *3 | 1 | 0 | Up/down counter data TC0 (LSB) | |
| 0E5H | TC7 | TC6 | TC5 | TC4 | TC7 | – *3 | 1 | 0 | Up/down counter data TC7 | |
| | R/W | | | | TC6 | – *3 | 1 | 0 | Up/down counter data TC6 | |
| | | | | | TC5 | – *3 | 1 | 0 | Up/down counter data TC5 | |
| | | | | | TC4 | – *3 | 1 | 0 | Up/down counter data TC4 | |
| 0E6H | TC11 | TC10 | TC9 | TC8 | TC11 | – *3 | 1 | 0 | Up/down counter data TC11 | |
| | R/W | | | | TC10 | – *3 | 1 | 0 | Up/down counter data TC10 | |
| | | | | | TC9 | – *3 | 1 | 0 | Up/down counter data TC9 | |
| | | | | | TC8 | – *3 | 1 | 0 | Up/down counter data TC8 | |
| 0E7H | TC15 | TC14 | TC13 | TC12 | TC15 | – *3 | 1 | 0 | Up/down counter data TC15 (MSB) | |
| | R/W | | | | TC14 | – *3 | 1 | 0 | Up/down counter data TC14 | |
| | | | | | TC13 | – *3 | 1 | 0 | Up/down counter data TC13 | |
| | | | | | TC12 | – *3 | 1 | 0 | Up/down counter data TC12 | |
| 0E8H | EIK03 | EIK02 | EIK01 | EIK00 | EIK03 | 0 | Enable | Mask | Interrupt mask register K03 | |
| | R/W | | | | EIK02 | 0 | Enable | Mask | Interrupt mask register K02 | |
| | | | | | EIK01 | 0 | Enable | Mask | Interrupt mask register K01 | |
| | | | | | EIK00 | 0 | Enable | Mask | Interrupt mask register K00 | |
| 0EBH | 0 | EIT2 | EIT8 | EIT32 | 0 | | | | *5 | |
| | R | R/W | | | EIT2 | 0 | Enable | Mask | Interrupt mask register (clock timer) 2 Hz | |
| | | | | | EIT8 | 0 | Enable | Mask | Interrupt mask register (clock timer) 8 Hz | |
| | | | | | EIT32 | 0 | Enable | Mask | Interrupt mask register (clock timer) 32 Hz | |
| 0ECH | 0 | 0 | 0 | EIAD | 0 | | | | *5 | |
| | R | | | R/W | 0 | | | | *5 | |
| | | | | | 0 | | | | *5 | |
| | | | | | EIAD | 0 | Enable | Mask | Interrupt mask register (A/D) | |
| 0EDH | 0 | 0 | 0 | IK0 | 0 | | | | *5 | |
| | R | | | | 0 | | | | *5 | |
| | | | | | 0 | | | | *5 | |
| | | | | | IK0 | 0 | Yes | No | Interrupt factor flag (K00–K03) | *4 |
| 0EFH | 0 | IT2 | IT8 | IT32 | 0 | | | | *5 | |
| | R | R | | | IT2 | 0 | Yes | No | Interrupt factor flag (clock timer) 2 Hz | *4 |
| | | | | | IT8 | 0 | Yes | No | Interrupt factor flag (clock timer) 8 Hz | *4 |
| | | | | | IT32 | 0 | Yes | No | Interrupt factor flag (clock timer) 32 Hz | *4 |

*1 Initial value following initial reset
 *2 Not set in the circuit
 *3 Undefined
 *4 Reset (0) immediately after being read
 *5 Always "0" when being read
 *6 Refer to main manual

Table 4.1.1(b) I/O memory map

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|----------|-----|--------|--------|--------|---------|--------|--------|-----------------------------------|
| | D3 | D2 | D1 | D0 | | | | | |
| 0F0H | 0 | 0 | 0 | IAD | 0 | | | | *5 |
| | R | | | | 0 | | | | *5 |
| 0F1H | 0 | 0 | 0 | ADRUN | 0 | | | | *5 |
| | R | | | R/W | ADRUN | 0 | Start | Stop | A/D conversion Start/Stop |
| 0F3H | R03 | R02 | R01 | R00 | R03 | 0 | High | Low | Output port data R03 |
| | BUZZER | | | | R02 | 0 | High | Low | Output port data R02 |
| | R/W | | | | R01 | 0 | High | Low | Output port data R01 |
| | R/W | | | | BUZZER | 0 | On | Off | Buzzer On/Off control register |
| | R/W | | | | R00 | 0 | High | Low | Output port data R00 |
| 0F4H | P03 | P02 | P01 | P00 | P03 | - *2 | High | Low | I/O port data P03 |
| | R/W | | | | P02 | - *2 | High | Low | I/O port data P02 |
| | R/W | | | | P01 | - *2 | High | Low | I/O port data P01 |
| | R/W | | | | P00 | - *2 | High | Low | I/O port data P00 |
| | R/W | | | | FOUT | 0 | On | Off | Frequency output control register |
| 0F5H | C3 | C2 | C1 | C0 | C3 | - *3 | 1 | 0 | Up-counter data C3 |
| | R/W | | | | C2 | - *3 | 1 | 0 | Up-counter data C2 |
| 0F6H | C7 | C6 | C5 | C4 | C7 | - *3 | 1 | 0 | Up-counter data C7 |
| | R/W | | | | C6 | - *3 | 1 | 0 | Up-counter data C6 |
| | R/W | | | | C5 | - *3 | 1 | 0 | Up-counter data C5 |
| | R/W | | | | C4 | - *3 | 1 | 0 | Up-counter data C4 |
| | R/W | | | | C0 | - *3 | 1 | 0 | Up-counter data C0 (LSB) |
| 0F7H | C11 | C10 | C9 | C8 | C7 | - *3 | 1 | 0 | Up-counter data C7 |
| | R/W | | | | C6 | - *3 | 1 | 0 | Up-counter data C6 |
| | R/W | | | | C5 | - *3 | 1 | 0 | Up-counter data C5 |
| | R/W | | | | C4 | - *3 | 1 | 0 | Up-counter data C4 |
| 0F8H | C15 | C14 | C13 | C12 | C11 | - *3 | 1 | 0 | Up-counter data C11 |
| | R/W | | | | C10 | - *3 | 1 | 0 | Up-counter data C10 |
| | R/W | | | | C9 | - *3 | 1 | 0 | Up-counter data C9 |
| | R/W | | | | C8 | - *3 | 1 | 0 | Up-counter data C8 |
| 0F9H | 0 | 0 | 0 | TMRST | C15 | - *3 | 1 | 0 | Up-counter data C15 (MSB) |
| | R | | | W | C14 | - *3 | 1 | 0 | Up-counter data C14 |
| | R | | | | C13 | - *3 | 1 | 0 | Up-counter data C13 |
| | R | | | | C12 | - *3 | 1 | 0 | Up-counter data C12 |
| 0FAH | HLMOD | 0 | 0 | 0 | 0 | | | | *5 |
| | R/W | R | | | 0 | | | | *5 |
| 0FBH | CSDC | 0 | 0 | 0 | 0 | | | | *5 |
| | R/W | R | | | 0 | | | | *5 |
| 0FCH | 0 | 0 | 0 | IOC | 0 | | | | *5 |
| | R | | | R/W | 0 | | | | *5 |
| 0FDH | 0 | 0 | 0 | IOC | 0 | 0 | Out | In | I/O port I/O control register |
| | XBZR | 0 | XFOUT1 | XFOUT0 | XBZR | 0 | 2 kHz | 4 kHz | Buzzer frequency control |
| | R/W | R | R/W | | XFOUT1 | 0 | | | FOUT frequency control |
| 0FEH | 0 | 0 | 0 | ADCLK | XFOUT0 | 0 | | | FOUT frequency control |
| | R | | | R/W | 0 | | | | *5 |
| | R | | | | ADCLK | 0 | 65 kHz | 32 kHz | A/D clock selection 65 kHz/32 kHz |

4.2 Oscillation Circuit

The S1C60N02 Series has a built-in oscillation circuit. For the oscillation circuit, either crystal oscillation or CR oscillation may be selected by a mask option.

Crystal oscillation circuit

The crystal oscillation circuit generates the operating clock for the CPU and peripheral circuit on connection to an external crystal oscillator (typ. 32.768 kHz) and trimmer capacitor (5–25 pF).

Figure 4.2.1 is the block diagram of the crystal oscillation circuit.

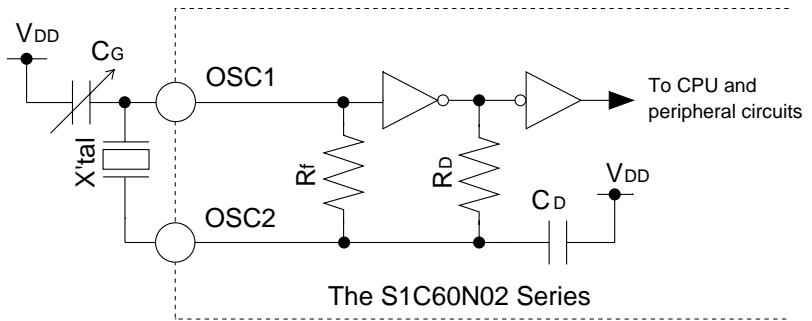


Fig. 4.2.1
Crystal oscillation circuit

As Figure 4.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between the OSC1 and OSC2 pins and the trimmer capacitor (CG) between the OSC1 and VDD pins.

CR oscillation circuit

For the S1C60N02 Series, CR oscillation circuit (typ. 65 kHz) may be selected by a mask option. Figure 4.2.2 is the block diagram of the CR oscillation circuit.

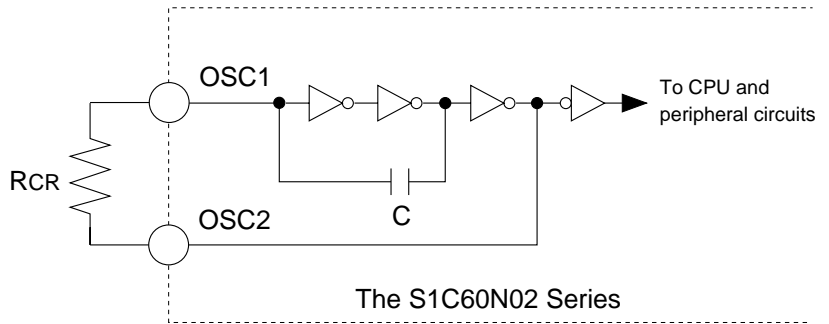


Fig. 4.2.2
CR oscillation circuit

As Figure 4.2.2 indicates, the CR oscillation circuit can be configured simply by connecting the register (RCR) between pins OSC1 and OSC2 since capacity (C) is built-in. See Chapter 6, "ELECTRICAL CHARACTERISTICS" for RCR value.

4.3 Input Ports (K00–K03)

Configuration of input ports

The S1C60N02 Series has a general-purpose input (4 bits). Each of the input port pins (K00–K03) has an internal pull-down resistance. The pull-down resistance can be selected for each bit with the mask option.

Figure 4.3.1 shows the configuration of input port.

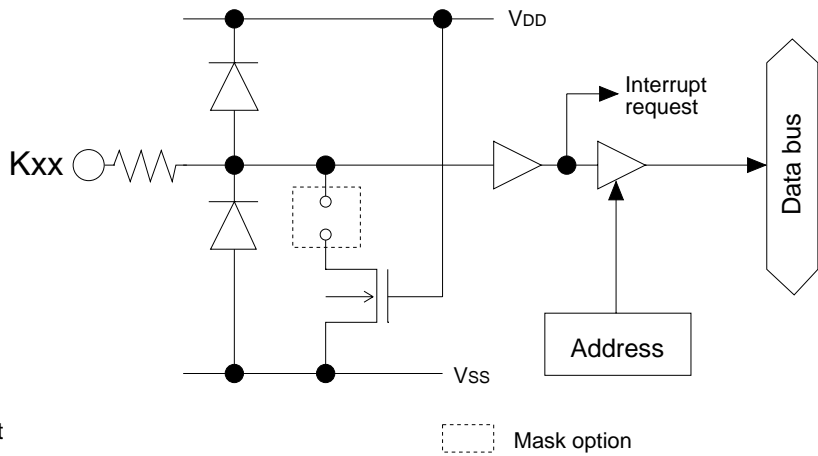


Fig. 4.3.1
Configuration of input port

Selecting "pull-down resistance enabled" with the mask option allows input from a push button, key matrix, and so forth. When "pull-down resistance disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs.

Input comparison registers and interrupt function

All four input port bits (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software for the four bits. Also, whether to mask the interrupt function can be selected individually for all four bits by the software. Figure 4.3.2 shows the configuration of K00–K03.

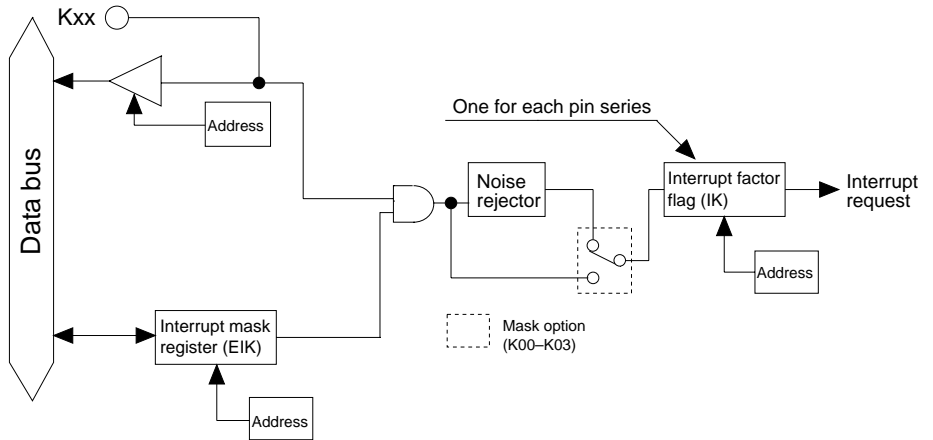


Fig. 4.3.2
Input interrupt circuit
configuration (K00–K03)

The interrupt mask registers (EIK00–EIK03) enable the interrupt mask to be selected individually for K00–K03. An interrupt occurs when the input value which are not masked change and the interrupt factor flag (IK0) is set to "1".

Mask option

The contents that can be selected with the input port mask option are as follows:

- (1) An internal pull-down resistance can be selected for each of the four bits of the input ports (K00–K03). Having selected "pull-down resistance disabled", take care that the input does not float. Select "pull-down resistance enabled" for input ports that are not being used.
- (2) The input interrupt circuit contains a noise rejection circuit to prevent interrupts from occurring through noise. The mask option enables selection of the noise rejection circuit for each separate pin series. When "use" is selected, a maximum delay of 0.5 ms ($f_{osc} = 32 \text{ kHz}$) occurs from the time an interrupt condition is established until the interrupt factor flag (IK) is set to "1".

Control of input ports Table 4.3.1 list the input port control bits and their addresses.

Table 4.3.1 Input port control bits

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|----------|-------|--------|-------|---------------------------------|---------|--------|------|-----------------------------|
| | D3 | D2 | D1 | D0 | | | | | |
| 0E0H | K03 | K02 | K01 | K00 | K03 | – *2 | High | Low | Input port data K03 |
| | R | | | | K02 | – *2 | High | Low | Input port data K02 |
| | | | | | K01 | – *2 | High | Low | Input port data K01 |
| | K00 | – *2 | High | Low | Input port data K00 | | | | |
| 0E8H | EIK03 | EIK02 | EIK01 | EIK00 | EIK03 | 0 | Enable | Mask | Interrupt mask register K03 |
| | R/W | | | | EIK02 | 0 | Enable | Mask | Interrupt mask register K02 |
| | | | | | EIK01 | 0 | Enable | Mask | Interrupt mask register K01 |
| | EIK00 | 0 | Enable | Mask | Interrupt mask register K00 | | | | |
| 0EDH | 0 | 0 | 0 | IK0 | 0 | | | | *5 |
| | R | | | | 0 | | | | *5 |
| | | | | | 0 | | | | *5 |
| | IK0 | 0 | Yes | No | Interrupt factor flag (K00–K03) | *4 | | | |

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

K00–K03 Input port data (0E0H)

The input data of the input port pins can be read with these registers.

When "1" is read: High level

When "0" is read: Low level

Writing: Invalid

The value read is "1" when the pin voltage of the four bits of the input ports (K00–K03) goes high (VDD), and "0" when the voltage goes low (VSS). These bits are reading, so writing cannot be done.

EIK00–EIK03 Interrupt mask registers (0E8H)

Masking the interrupt of the input port pins can be done with these registers.

When "1" is written: Enable

When "0" is written: Mask

Reading: Valid

With these registers, masking of the input port bits can be done for each of the four bits. After an initial reset, these registers are all set to "0".

IK0 Interrupt factor flags (0EDH D0)

These flags indicate the occurrence of an input interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

Writing: Invalid

The interrupt factor flag IK0 is associated with K00–K03, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred. These flags are reset when the software has read them. Reading of interrupt factor flags is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. After an initial reset, these flags are set to "0".

4.4 Output Ports (R00–R03)

Configuration of output ports

The S1C60N02 Series has 4 bits for general output ports (R00–R03).

Output specifications of the output ports can be selected individually with the mask option. Three kinds of output specifications are available: complementary output and Pch open drain output. Also, the mask option enables the output ports R00 and R01 to be used as special output ports. Figure 4.4.1 shows the configuration of the output ports.

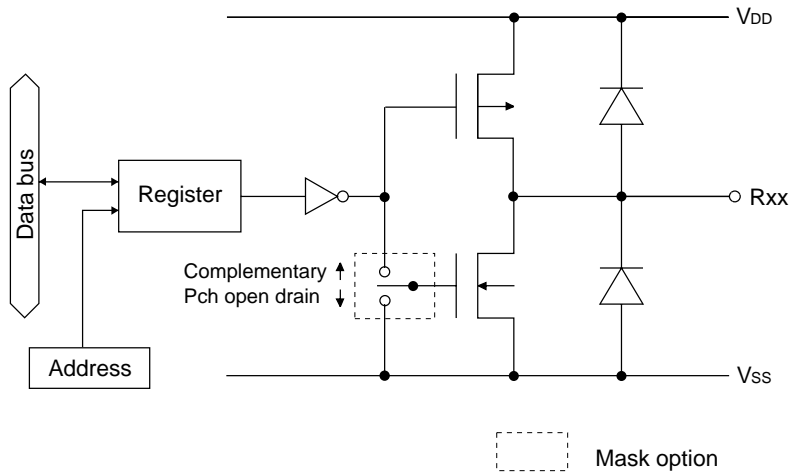


Fig. 4.4.1
Configuration of output ports

Mask option

The mask option enables the following output port selection.

(1) Output specifications of output ports

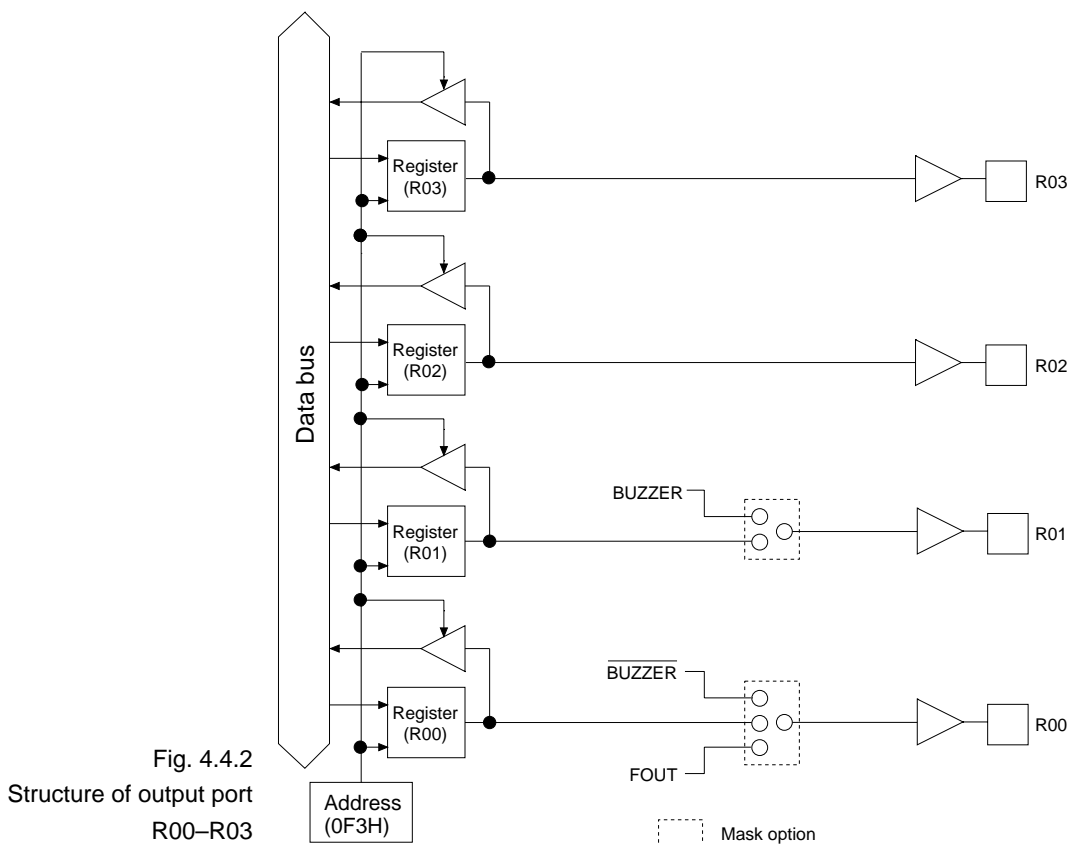
The output specifications for the output ports (R00–R03) may be either complementary output or Pch open drain output for each of the four bits. However, even when Pch open drain output is selected, a voltage exceeding the source voltage must not be applied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for output ports R00 and R01, as shown in Table 4.4.1. Figure 4.4.2 shows the structure of output ports R00–R03.

Table 4.4.1
Special output

| Pin name | When special output is selected |
|----------|------------------------------------|
| R00 | FOUT or $\overline{\text{BUZZER}}$ |
| R01 | BUZZER |



FOUT (R00) When output port R00 is set for FOUT output, this port will generate f_{osc} (CPU operating clock frequency) or clock frequency divided into f_{osc} . Clock frequency may be selected individually for F1–F4, from among 5 types by mask option; one among F1–F4 is selected by software and used. The types of frequency which may be selected are shown in Table 4.4.2.

Table 4.4.2
FOUT clock frequency

| Setting value | Clock frequency (Hz) $f_{osc} = 32,768$ | | | |
|---------------|---|---------------------------|---------------------------|---------------------------|
| | F1 | F2 | F3 | F4 |
| | (D1,D0)=(0,0) | (D1,D0)=(0,1) | (D1,D0)=(1,0) | (D1,D0)=(1,1) |
| 1 | 256 ($f_{osc}/128$) | 512 ($f_{osc}/64$) | 1,024 ($f_{osc}/32$) | 2,048 ($f_{osc}/16$) |
| 2 | 512 ($f_{osc}/64$) | 1,024 ($f_{osc}/32$) | 2,048 ($f_{osc}/16$) | 4,096 ($f_{osc}/8$) |
| 3 | 1,024 ($f_{osc}/32$) | 2,048 ($f_{osc}/16$) | 4,096 ($f_{osc}/8$) | 8,192 ($f_{osc}/4$) |
| 4 | 2,048 ($f_{osc}/16$) | 4,096 ($f_{osc}/8$) | 8,192 ($f_{osc}/4$) | 16,384 ($f_{osc}/2$) |
| 5 | 4,096 ($f_{osc}/8$) | 8,192 ($f_{osc}/4$) | 16,384 ($f_{osc}/2$) | 32,768 ($f_{osc}/1$) |

(D1, D0) = (XFOUT1, XFOUT0)

Note A hazard may occur when the FOUT signal is turned on or off.

BUZZER, $\overline{\text{BUZZER}}$ (R01, R00) Output ports R01 and R00 may be set to BUZZER output and $\overline{\text{BUZZER}}$ output ($\overline{\text{BUZZER}}$ reverse output), respectively, allowing for direct driving of the piezo-electric buzzer. $\overline{\text{BUZZER}}$ output (R00) may only be set if R01 is set to BUZZER output. In such case, whether ON/OFF of the $\overline{\text{BUZZER}}$ output is done through R00 register or is controlled through R01 simultaneously with BUZZER output is also selected by mask option. The frequency of buzzer output may be selected by software to be either 2 kHz or 4 kHz.

Control of output ports

Table 4.4.3 lists the output port control bits and their addresses.

Table 4.4.3 Control bits of output ports

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment | |
|---------|----------|-----|--------|--------|--------|---------|-------|-------|-----------------------------------|------------------------|
| | D3 | D2 | D1 | D0 | | | | | | |
| 0F3H | R03 | R02 | R01 | R00 | R03 | 0 | High | Low | Output port data R03 | |
| | | | BUZZER | FOUT | R02 | 0 | High | Low | Output port data R02 | |
| | R/W | | | | R01 | 0 | High | Low | Output port data R01 | |
| | | | | | BUZZER | 0 | On | Off | Buzzer On/Off control register | |
| | | | | | R00 | 0 | High | Low | Output port data R00 | |
| | R/W | | | | FOUT | 0 | On | Off | Frequency output control register | |
| | | | | | | | | | | |
| 0FDH | XBZR | 0 | XFOUT1 | XFOUT0 | XBZR | 0 | 2 kHz | 4 kHz | Buzzer frequency control | |
| | | | | | 0 | | | | *5 | |
| | R/W | R | R/W | | XFOUT1 | 0 | | | | FOUT frequency control |
| | | | | | XFOUT0 | 0 | | | | FOUT frequency control |

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

R00–R03 Output port data (0F3H)

Sets the output data for the output ports.

When "1" is written: High output

When "0" is written: Low output

Reading: Valid

The output port pins output the data written to the corresponding registers (R00–R03) without changing it. When "1" is written to the register, the output port pin goes high (VDD), and when "0" is written, the output port pin goes low (VSS). After an initial reset, all registers are set to "0".

R00 (when FOUT is selected) Special output port data (0F3H D0)
 Controls the FOUT (clock) output.

- When "1" is written: Clock output
- When "0" is written: Low level (DC) output
- Reading: Valid

FOUT output can be controlled by writing data to R00. After an initial reset, this register is set to "0".

Figure 4.4.3 shows the output waveform for FOUT output.

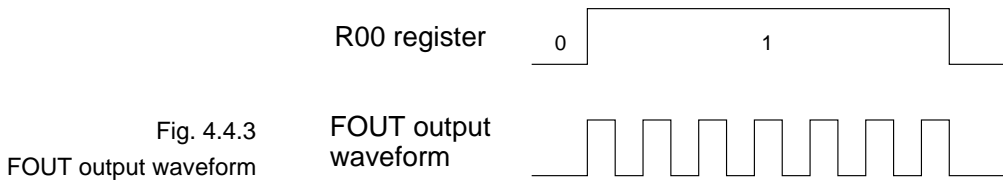


Fig. 4.4.3
 FOUT output waveform

XFOUT0, XFOUT1 FOUT frequency control (0FDH D0, 0FDH D1)
 Selects the output frequency when R00 port is set for FOUT output.

Table 4.4.4
 FOUT frequency selection

| XFOUT1 | XFOUT0 | Frequency selection |
|--------|--------|---------------------|
| 0 | 0 | F1 |
| 0 | 1 | F2 |
| 1 | 0 | F3 |
| 1 | 1 | F4 |

After an initial reset, these registers are set to "0".

R00, R01 (when $\overline{\text{BUZZER}}$ and BUZZER is selected) Special output port data (0F3H D0, 0F3H D1)
 Controls the buzzer output.

When "1" is written: Buzzer output
 When "0" is written: Low level (DC) output
 Reading: Valid

$\overline{\text{BUZZER}}$ and BUZZER output can be controlled by writing data to R00 and R01.

When $\overline{\text{BUZZER}}$ output by R01 register control is selected by mask option, BUZZER output and $\overline{\text{BUZZER}}$ output can be controlled simultaneously by writing data to R01 register. After an initial reset, these registers are set to "0".

Figure 4.4.4 shows the output waveform for buzzer output.

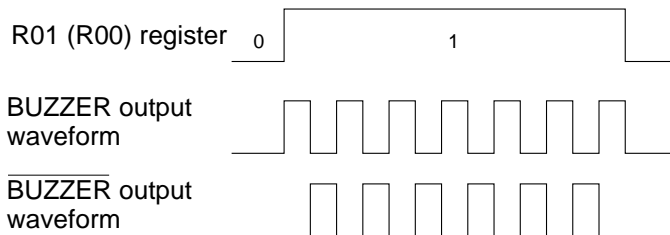


Fig. 4.4.4
 Buzzer output waveform

XBZR Buzzer frequency control (0FDH D3)
 Selects the frequency of the buzzer signal.

When "1" is written: 2 kHz
 When "0" is written: 4 kHz
 Reading: Valid

When R00 and R01 port is set to buzzer output, the frequency of the buzzer signal can be selected by this register. When "1" is written to this register, the frequency is set in 2 kHz, and in 4 kHz when "0" is written. After an initial reset, this register is set to "0".

4.5 I/O Ports (P00–P03)

Configuration of I/O ports

The S1C60N02 Series has a 4-bit general-purpose I/O port. Figure 4.5.1 shows the configuration of the I/O port. The four bits of the I/O port P00–P03 can be set to either input mode or output mode. The mode can be set by writing data to the I/O control register (IOC).

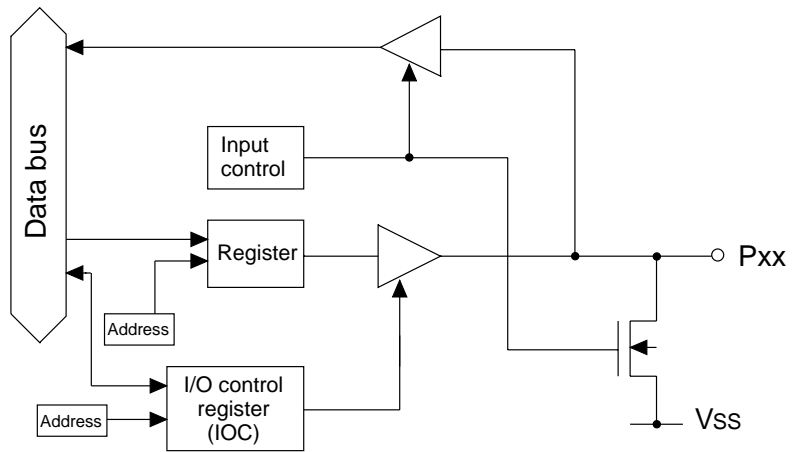


Fig. 4.5.1
Configuration of I/O port

I/O control register and I/O mode

Input or output mode can be set for the four bits of I/O port P00–P03 by writing data into I/O control register IOC. To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, its impedance becomes high and it works as an input port. However, the input line is pulled down when input data is read.

The output mode is set when "1" is written to the I/O control register (IOC). When an I/O port set to output mode works as an output port, it outputs a high signal (VDD) when the port output data is "1", and a low signal (VSS) when the port output data is "0".

After an initial reset, the I/O control register is set to "0", and the I/O port enters the input mode.

Mask option

The output specification during output mode (IOC = "1") of the I/O port can be set with the mask option for either complementary output or Pch open drain output. This setting can be performed for each bit of the I/O port. However, when Pch open drain output has been selected, voltage in excess of the supply voltage must not be applied to the port.

Control of I/O ports

Table 4.5.1 lists the I/O port control bits and their addresses.

Table 4.5.1 I/O port control bits

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|----------|-----|-----|-----|------|---------|------|-----|-------------------------------|
| | D3 | D2 | D1 | D0 | | | | | |
| 0F4H | P03 | P02 | P01 | P00 | P03 | - *2 | High | Low | I/O port data P03 |
| | | | | | P02 | - *2 | High | Low | I/O port data P02 |
| | R/W | | | | P01 | - *2 | High | Low | I/O port data P01 |
| | | | | | P00 | - *2 | High | Low | I/O port data P00 |
| 0FCH | 0 | 0 | 0 | IOC | 0 | | | | *5 |
| | | | | | 0 | | | | *5 |
| | R | | | R/W | 0 | | | | *5 |
| | | | | | IOC | 0 | Out | In | I/O port I/O control register |

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

P00–P03 I/O port data (0F4H)

I/O port data can be read and output data can be written through the port.

- When writing data

When "1" is written: High level

When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output from the I/O port pin unchanged. When "1" is written as the port data, the port pin goes high (VDD), and when "0" is written, the level goes low (VSS). Port data can also be written in the input mode.

- When reading data

When "1" is read: High level

When "0" is read: Low level

The pin voltage level of the I/O port is read. When the I/O port is in the input mode the voltage level being input to the port pin can be read; in the output mode the output voltage level can be read. When the pin voltage is high (VDD) the port data read is "1", and when the pin voltage is low (VSS) the data is "0". Also, the built-in pull-down resistance functions during reading, so the I/O port pin is pulled down.

- Note*
- When the I/O port is set to the output mode and a low-impedance load is connected to the port pin, the data written to the register may differ from the data read.
 - When the I/O port is set to the input mode and a low-level voltage (Vss) is input by the built-in pull-down resistance, an erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistance load is greater than the read-out time. When the input data is being read, the time that the input line is pulled down is equivalent to 0.5 cycles of the CPU system clock. Hence, the electric potential of the pins must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-down resistance externally, or performing multiple read-outs.

IOC I/O control register (0FCH D0)

The input or output I/O port mode can be set with this register.

When "1" is written: Output mode

When "0" is written: Input mode

Reading: Valid

The input or output mode of the I/O port is set in units of four bits. For instance, IOC sets the mode for P00-P03. Writing "1" to the I/O control register makes the I/O port enter the output mode, and writing "0", the input mode. After an initial reset, the IOC register is set to "0", so the I/O port is in the input mode.

4.6 LCD Driver (COM0–COM3, SEG0–SEG19)

Configuration of LCD driver

The S1C60N02 Series has four common pins and 20 (SEG0–SEG19) segment pins, so that an LCD with a maximum of 80 (20×4) segments can be driven. The power for driving the LCD is generated by the CPU internal circuit, so there is no need to supply power externally.

The driving method is 1/4 duty (or 1/3, 1/2 duty by mask option) dynamic drive, adopting the four types of potential (1/3 bias), V_{DD} , V_{L1} , V_{L2} and V_{L3} . Moreover, the 1/2 bias dynamic drive that uses three types of potential, V_{DD} , $V_{L1} = V_{L2}$ and V_{L3} , can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2). 1/2 bias drive is effective when the LCD system regulated voltage circuit is not used. The V_{L1} terminal and the V_{L2} terminal should be connected outside of the IC.

The frame frequency is 32 Hz for 1/4 duty and 1/2 duty, and 42.7 Hz for 1/3 duty (in the case of $f_{osc} = 32.768$ kHz). Figure 4.6.1 shows the drive waveform for 1/4 duty (1/3 bias), Figure 4.6.2 shows the drive waveform for 1/3 duty (1/3 bias), Figure 4.6.3 shows the drive waveform for 1/2 duty (1/3 bias), Figure 4.6.4 shows the drive waveform for 1/4 duty (1/2 bias), Figure 4.6.5 shows the drive waveform for 1/3 duty (1/2 bias) and Figure 4.6.6 shows the drive waveform for 1/2 duty (1/2 bias).

Note f_{osc} indicates the oscillation frequency of the oscillation circuit.

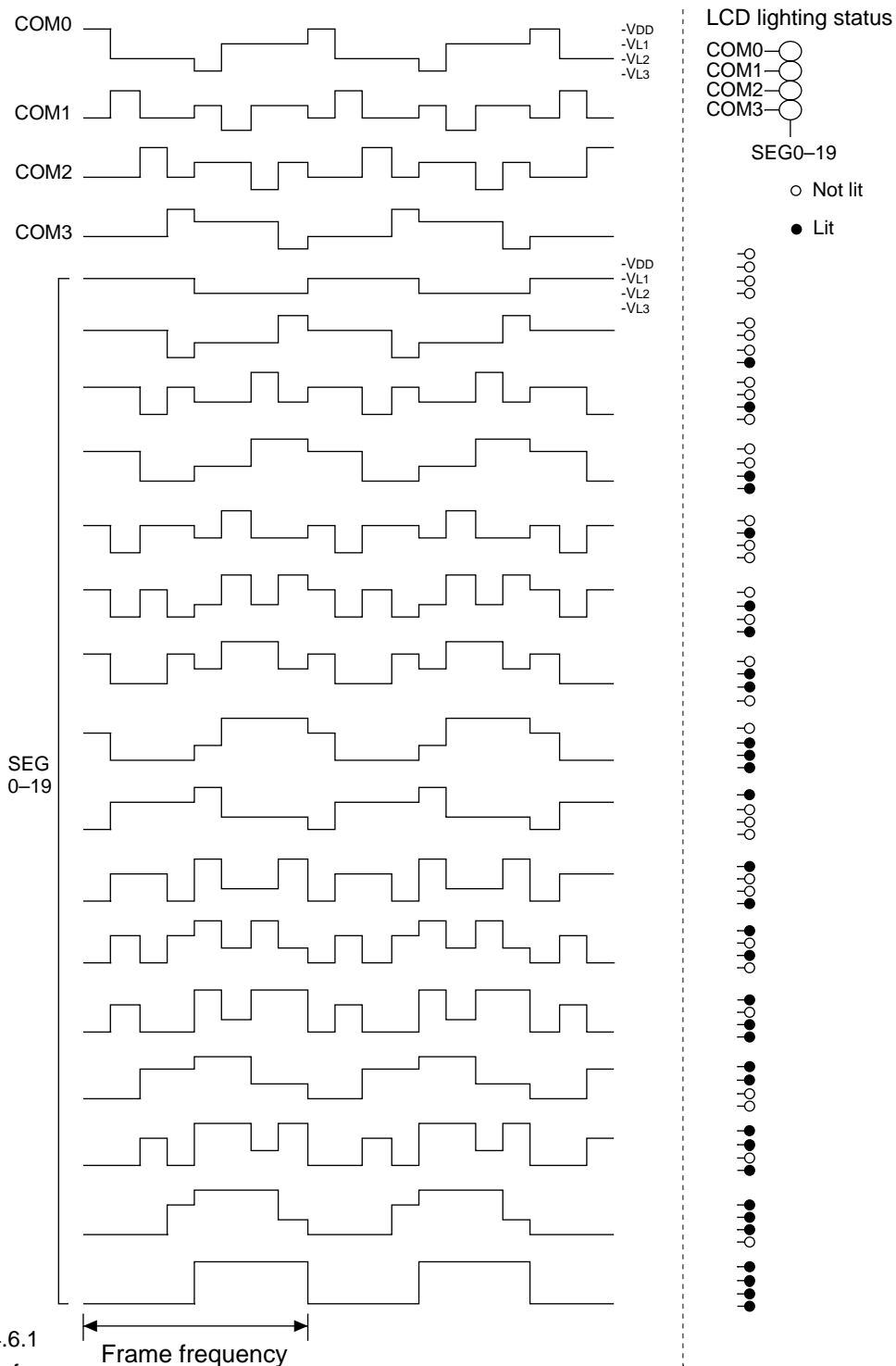


Fig. 4.6.1
Drive waveform for
1/4 duty (1/3 bias)

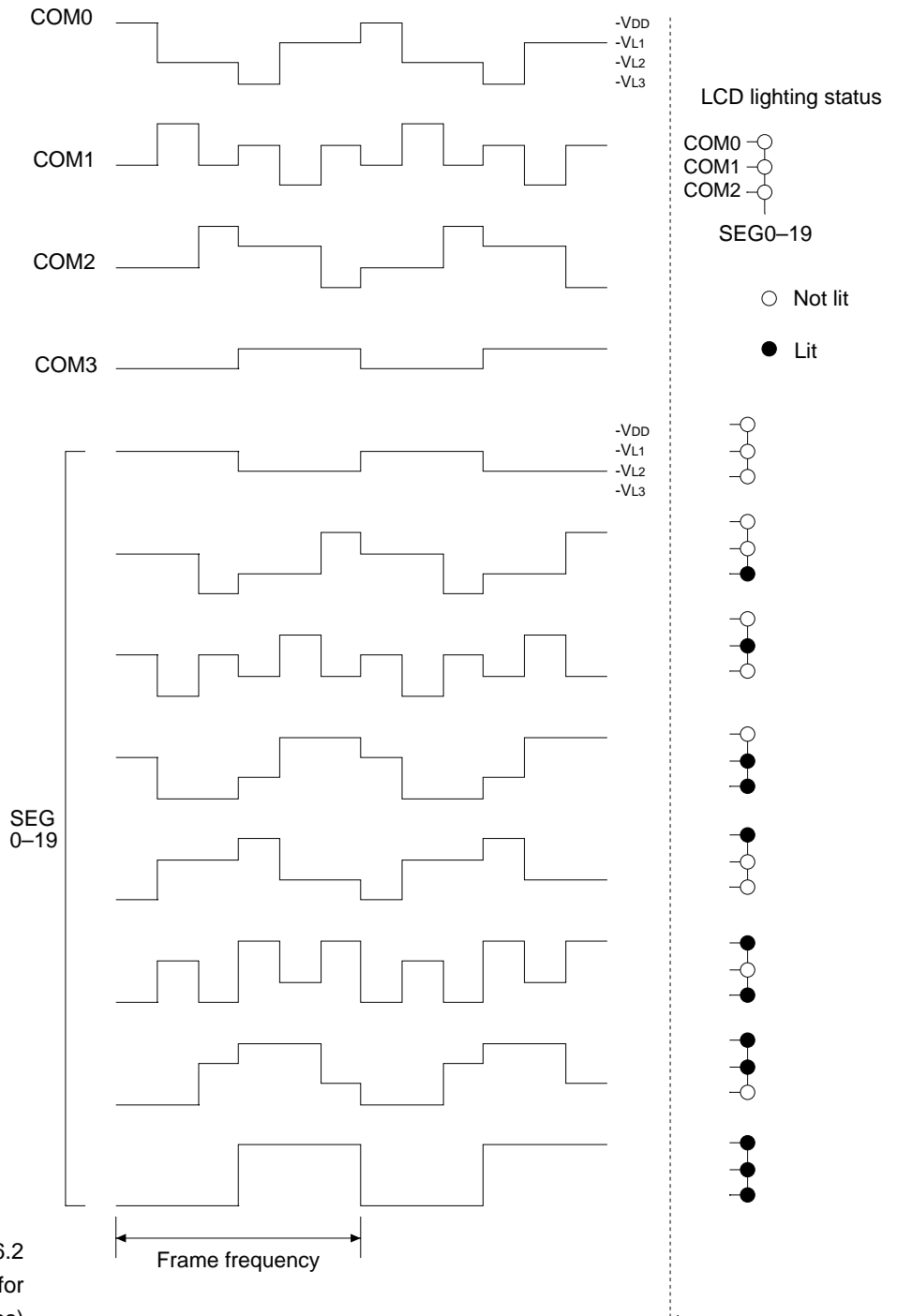


Fig. 4.6.2
Drive waveform for
1/3 duty (1/3 bias)

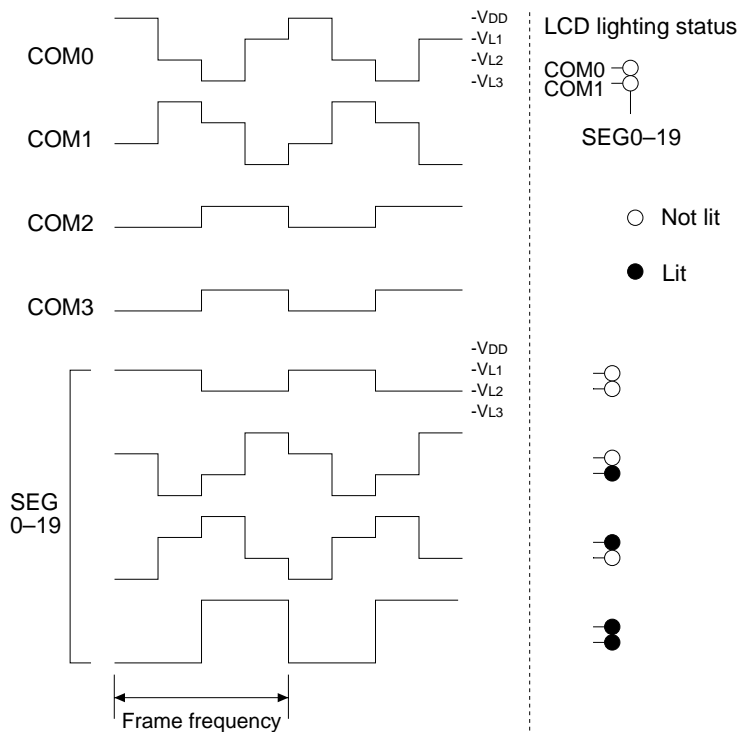


Fig. 4.6.3
Drive waveform for
1/2 duty (1/3 bias)

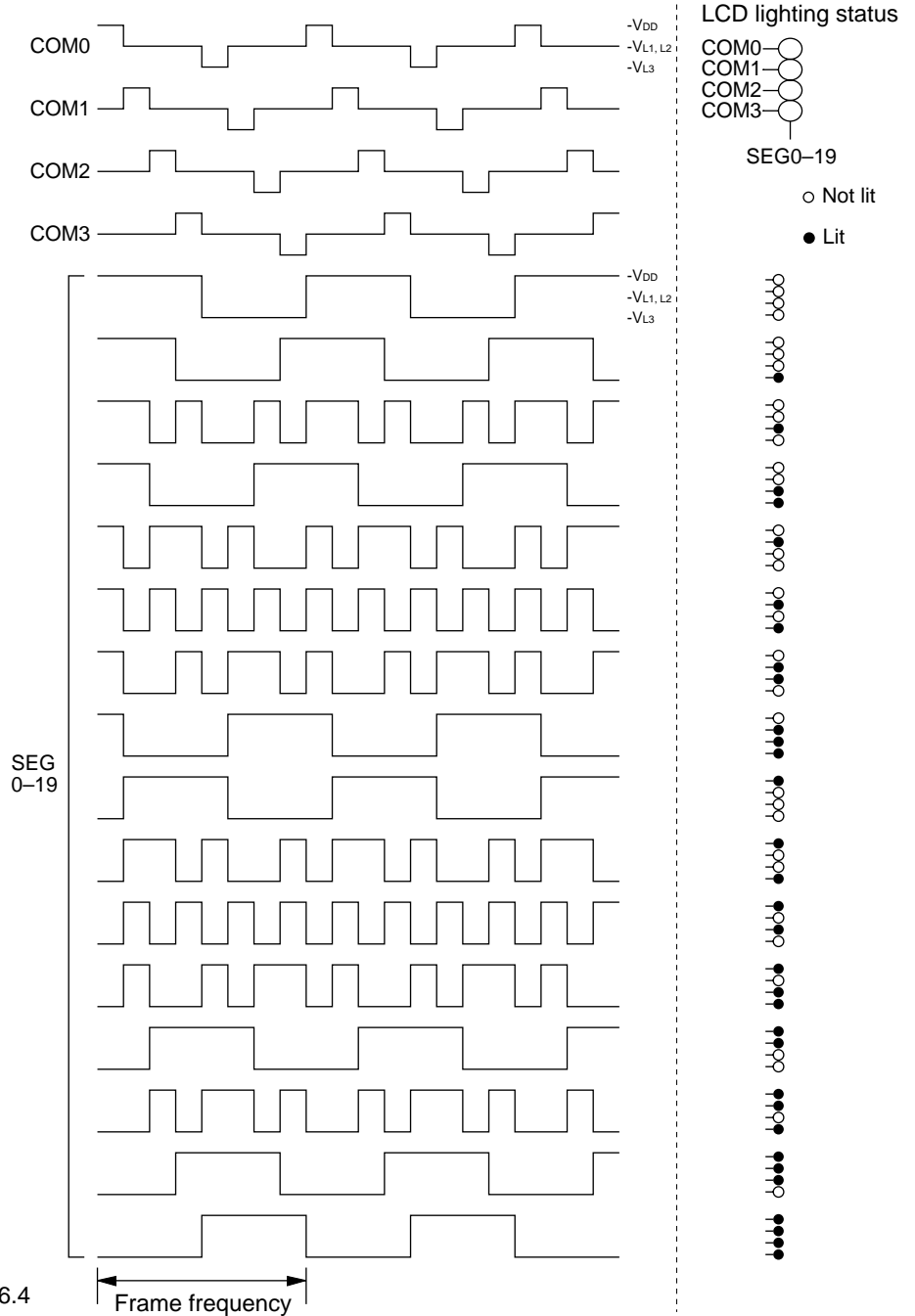


Fig. 4.6.4
Drive waveform for
1/4 duty (1/2 bias)

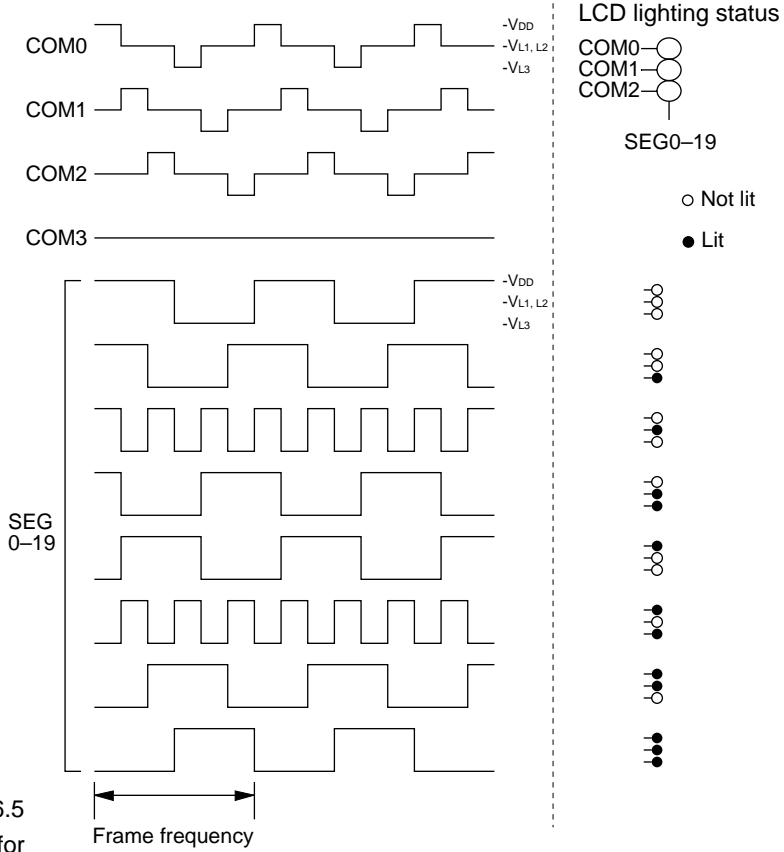


Fig. 4.6.5
Drive waveform for
1/3 duty (1/2 bias)

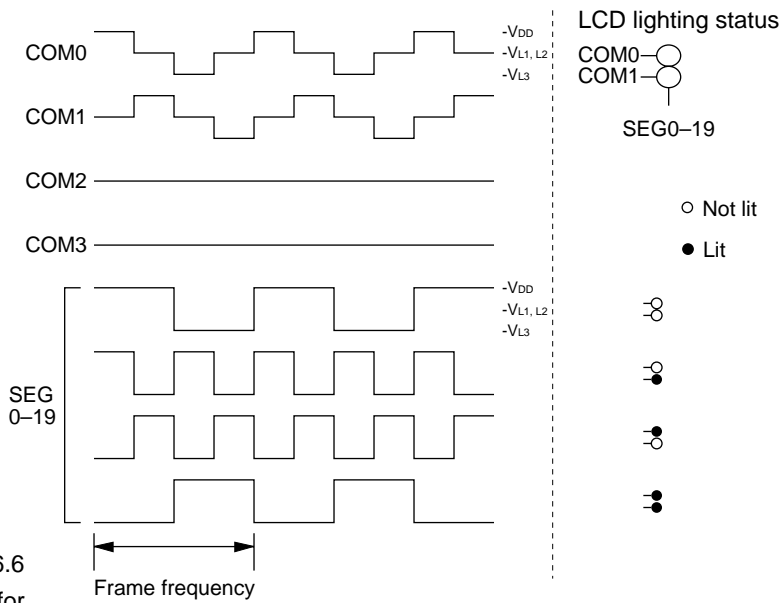


Fig. 4.6.6
Drive waveform for
1/2 duty (1/2 bias)

Cadence adjustment of oscillation frequency

In the S1C60N02 Series, the LCD drive duty can be set to 1/1 duty by software. This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the OSC circuit.

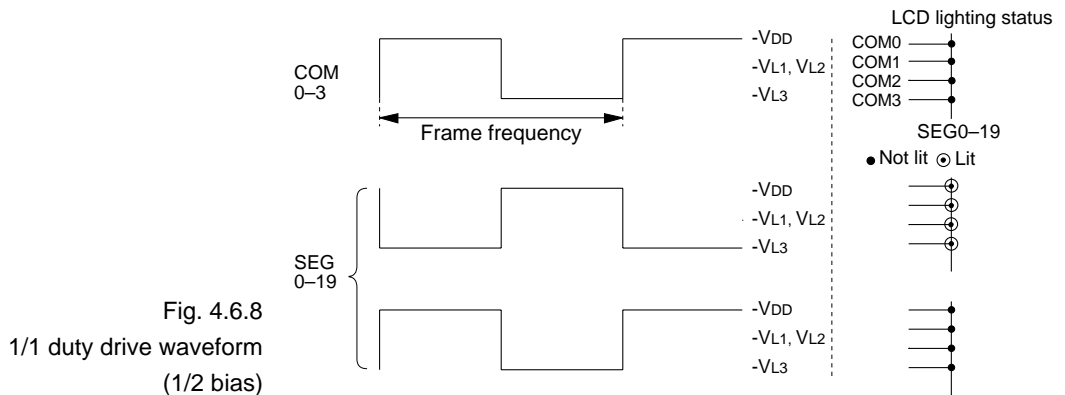
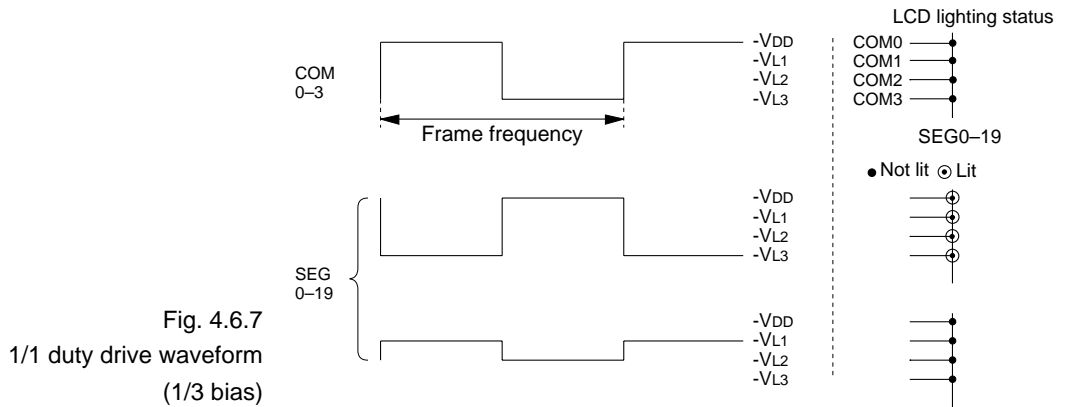
The procedure to set to 1/1 duty drive is as follows:

- ① Write "1" to the CSDC register at address "0FBH D3".
- ② Write the same value to all registers corresponding to COMs 0 through 3 of the display memory.

The frame frequency is 32 Hz ($f_{OSC1}/1,024$, when $f_{OSC1} = 32.768$ kHz).

- Note*
- Even when 1/3 or 1/2 duty is selected by the mask option, the display data corresponding to all COM are valid during 1/1 duty driving. Hence, for 1/1 duty drive, set the same value for all display memory corresponding to COMs 0 through 3.
 - For cadence adjustment, set the display data corresponding to COMs 0 through 3, so that all the LCD segments go on.

Figure 4.6.7 shows the 1/1 duty drive waveform (1/3 bias).
 Figure 4.6.8 shows the 1/1 duty drive waveform (1/2 bias).



Mask option
(segment allocation)

(1) Segment allocation

As shown in Figure 4.1.1, the S1C60N02 Series display data is decided by the display data written to the display memory (write-only) at address "090H-0AFH".

The address and bits of the display memory can be made to correspond to the segment pins (SEG0-SEG19) in any combination through mask option. This simplifies design by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.6.9 shows an example of the relationship between the LCD segments (on the panel) and the display memory in the case of 1/3 duty.

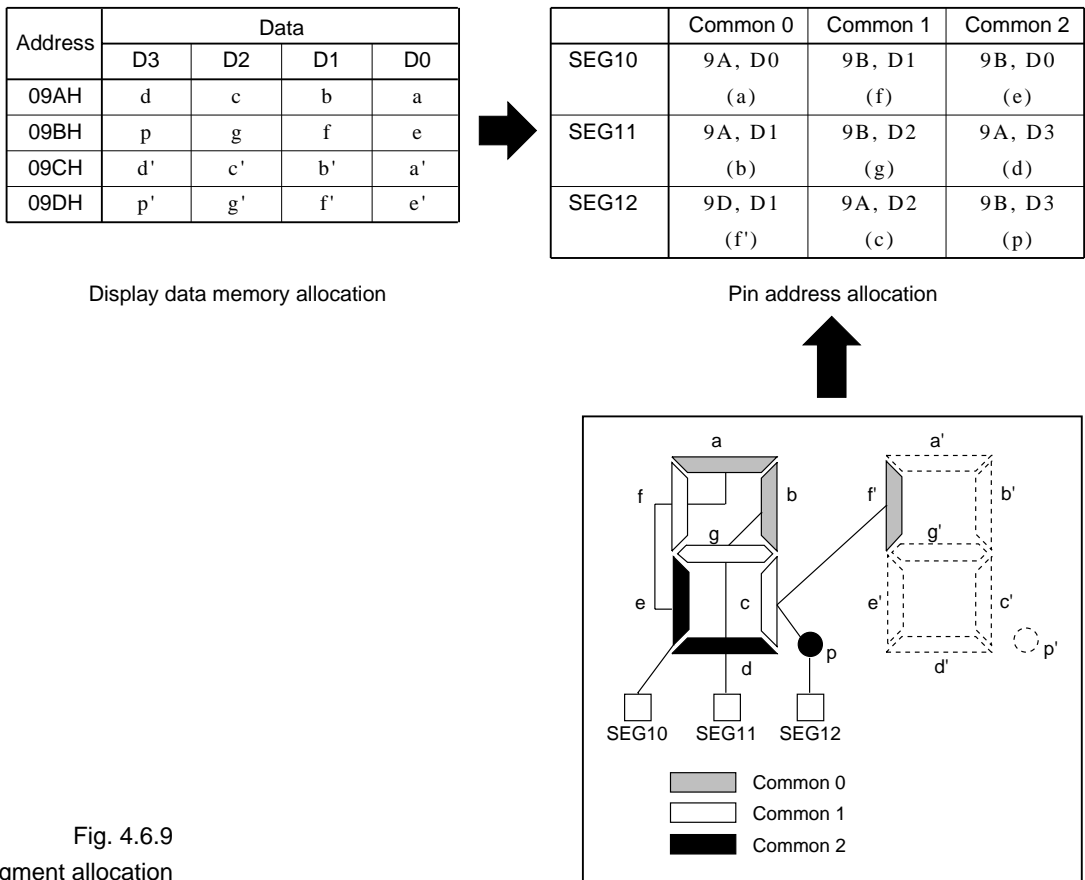


Fig. 4.6.9
Segment allocation

(2) Drive duty

According to the mask option, either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty.

Table 4.6.1 shows the differences in the number of segments according to the selected duty.

Table 4.6.1
Differences according to
selected duty

| Duty | Pins used in common | Maximum number of segments | Frame frequency (when fosc = 32 kHz) |
|------|---------------------|----------------------------|--------------------------------------|
| 1/4 | COM0–3 | 80 (20 × 4) | 32 Hz |
| 1/3 | COM0–2 | 60 (20 × 3) | 42.7 Hz |
| 1/2 | COM0–1 | 40 (20 × 2) | 32 Hz |

(3) Output specification

- ① The segment pins (SEG0–SEG19) are selected by mask option in pairs for either segment signal output or DC output (VDD and VSS binary output). When DC output is selected, the data corresponding to COM0 of each segment pin is output.
- ② When DC output is selected, either complementary output or Pch open drain output can be selected for each pin by mask option.

Note The pin pairs are the combination of SEG (2*n) and SEG (2*n + 1) (where n is an integer from 0 to 12).

(4) Drive bias

For the drive bias of the S1C60N02 or the S1C60L02, either 1/3 bias or 1/2 bias can be selected by the mask option.

Control of LCD driver

Table 4.6.2 shows the control bits of the LCD driver and their addresses. Figure 4.6.10 shows the display memory map.

Table 4.6.2 Control bits of LCD driver

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|----------|----|----|----|------|---------|--------|---------|------------------|
| | D3 | D2 | D1 | D0 | | | | | |
| 0FBH | CSDC | 0 | 0 | 0 | CSDC | 0 | Static | Dynamic | LCD drive switch |
| | R/W | R | | | 0 | | | | *5 |
| | | | | | 0 | | | | *5 |
| | | | | 0 | | | | *5 | |

- *1 Initial value following initial reset
- *2 Not set in the circuit
- *3 Undefined
- *4 Reset (0) immediately after being read
- *5 Always "0" when being read
- *6 Refer to main manual

Fig. 4.6.10 Display memory map

| Address | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---------|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 090 | Display memory (Write only) 32 words x 4 bits | | | | | | | | | | | | | | | |
| 0A0 | | | | | | | | | | | | | | | | |

CSDC LCD drive switch (0FBH D3)

The LCD drive format can be selected with this switch.

- When "1" is written: Static drive
- When "0" is written: Dynamic drive
- Reading: Valid

After an initial reset, dynamic drive (CSDC = "0") is selected.

Display memory (090H–0AFH)

The LCD segments are turned on or off according to this data.

- When "1" is written: On
- When "0" is written: Off
- Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be turned on or off. After an initial reset, the contents of the display memory are undefined.

4.7 Clock Timer

Configuration of clock timer

The S1C60N02 Series has a built-in clock timer driven by the source oscillator. The clock timer is configured as a seven-bit binary counter that serves as a frequency divider taking a 256 Hz source clock from a prescaler. The four high-order bits (16 Hz–2 Hz) can be read by the software. Figure 4.7.1 is the block diagram of the clock timer.

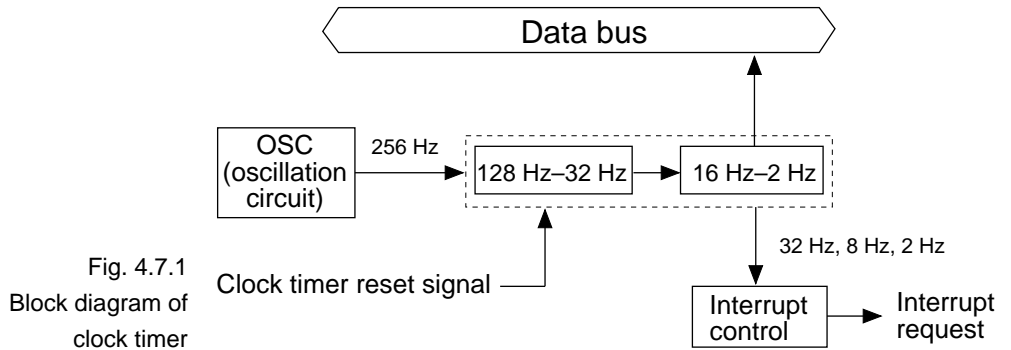


Fig. 4.7.1
Block diagram of clock timer

Normally, this clock timer is used for all kinds of timing purpose, such as clocks.

Interrupt function

The clock timer can interrupt on the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. The software can mask any of these interrupt signals.

Figure 4.7.2 is the timing chart of the clock timer.

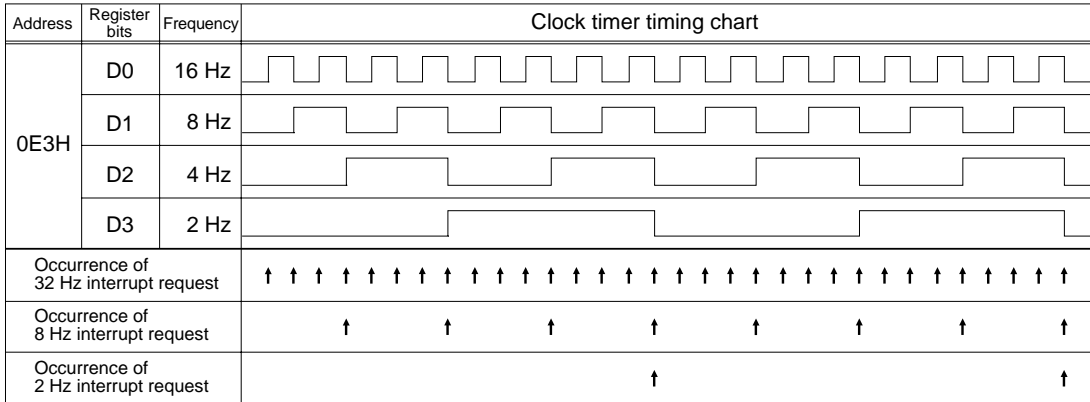


Fig. 4.7.2 Timing chart of the clock timer

As shown in Figure 4.7.2, an interrupt is generated on the falling edge of the 32 Hz, 8 Hz, and 2 Hz frequencies. When this happens, the corresponding interrupt event flag (IT32, IT8, IT2) is set to "1". Masking the separate interrupts can be done with the interrupt mask register (EIT32, EIT8, EIT2). However, regardless of the interrupt mask register setting, the interrupt event flags will be set to "1" on the falling edge of their corresponding signal (e.g. the falling edge of the 2 Hz signal sets the 2 Hz interrupt factor flag to "1").

Note Write to the interrupt mask register (EIT32, EIT8, EIT2) only in the DI status (interrupt flag = "0"). Otherwise, it causes malfunction.

Control of clock timer

Table 4.7.1 shows the clock timer control bits and their addresses.

Table 4.7.1 Control bits of clock timer

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|----------|-------|------|--------|-------|---|--------|------|---|
| | D3 | D2 | D1 | D0 | | | | | |
| 0E3H | TM3 | TM2 | TM1 | TM0 | TM3 | – *3 | High | Low | Clock timer data 2 Hz |
| | | | | | TM2 | – *3 | High | Low | Clock timer data 4 Hz |
| | R | | | | TM1 | – *3 | High | Low | Clock timer data 8 Hz |
| | | | | | TM0 | – *3 | High | Low | Clock timer data 16 Hz |
| 0EBH | 0 | EIT2 | EIT8 | EIT32 | 0 | 0 | Enable | Mask | Interrupt mask register (clock timer) 2 Hz *5 |
| | R | R/W | | | EIT8 | 0 | Enable | Mask | Interrupt mask register (clock timer) 8 Hz |
| | | EIT32 | 0 | Enable | Mask | Interrupt mask register (clock timer) 32 Hz | | | |
| 0EFH | 0 | IT2 | IT8 | IT32 | 0 | | | | *5 |
| | | | | | IT2 | 0 | Yes | No | Interrupt factor flag (clock timer) 2 Hz *4 |
| | R | | | | IT8 | 0 | Yes | No | Interrupt factor flag (clock timer) 8 Hz *4 |
| | | | | | IT32 | 0 | Yes | No | Interrupt factor flag (clock timer) 32 Hz *4 |
| 0F9H | 0 | 0 | 0 | TMRST | 0 | | | | *5 |
| | | | | | 0 | | | | *5 |
| | R | | | W | 0 | | | | *5 |
| | | | | TMRST | Reset | Reset | – | | Clock timer reset *5 |

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

TM0–TM3 Timer data (0E3H)

The 16 Hz to 2 Hz timer data of the clock timer can be read from this register. These four bits are read-only, and write operations are invalid.

After an initial reset, the timer data is initialized to "0H".

EIT32, EIT8, EIT2 Interrupt mask registers (0EBH D0–D2)

These registers are used to mask the clock timer interrupt.

When "1" is written: Enabled

When "0" is written: Masked

Reading: Valid

The interrupt mask register bits (EIT32, EIT8, EIT2) mask the corresponding interrupt frequencies (32 Hz, 8 Hz, 2 Hz). After an initial reset, these registers are all set to "0".

IT32, IT8, IT2 Interrupt factor flags (0EFH D0–D2)

These flags indicate the status of the clock timer interrupt.

- When "1" is read: Interrupt has occurred
- When "0" is read: Interrupt has not occurred
- Writing: Invalid

The interrupt factor flags (IT32, IT8, IT2) correspond to the clock timer interrupts (32 Hz, 8 Hz, 2 Hz). The software can determine from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" on the falling edge of the signal. These flags can be reset when the register is read by the software. Reading of interrupt factor flags is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

After an initial reset, these flags are set to "0".

TMRST Clock timer reset (0F9H D0)

This bit resets the clock timer.

- When "1" is written: Clock timer reset
- When "0" is written: No operation
- Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" when read.

4.8 A/D Converter

Configuration of A/D converter

The S1C60N02 Series has a CR oscillation type A/D converter. This A/D converter is equipped with two CR oscillation circuit systems and a counter that measures their oscillation frequency. Counted values represent connected resistance values converted into digital values. Connect a reference resistance that does not change oscillation frequency according to temperature between the RS and CS terminals and a sensor that does change resistance values according to temperature between the TH and CS terminals. Then, oscillate them alternately. The difference in the counted value can be evaluated as the difference between the respective oscillation frequencies. Therefore, various sensor circuit such as a temperature-measuring circuit using a thermistor can be easily created, for example. The configuration of the A/D converter is shown in Figure 4.8.1.

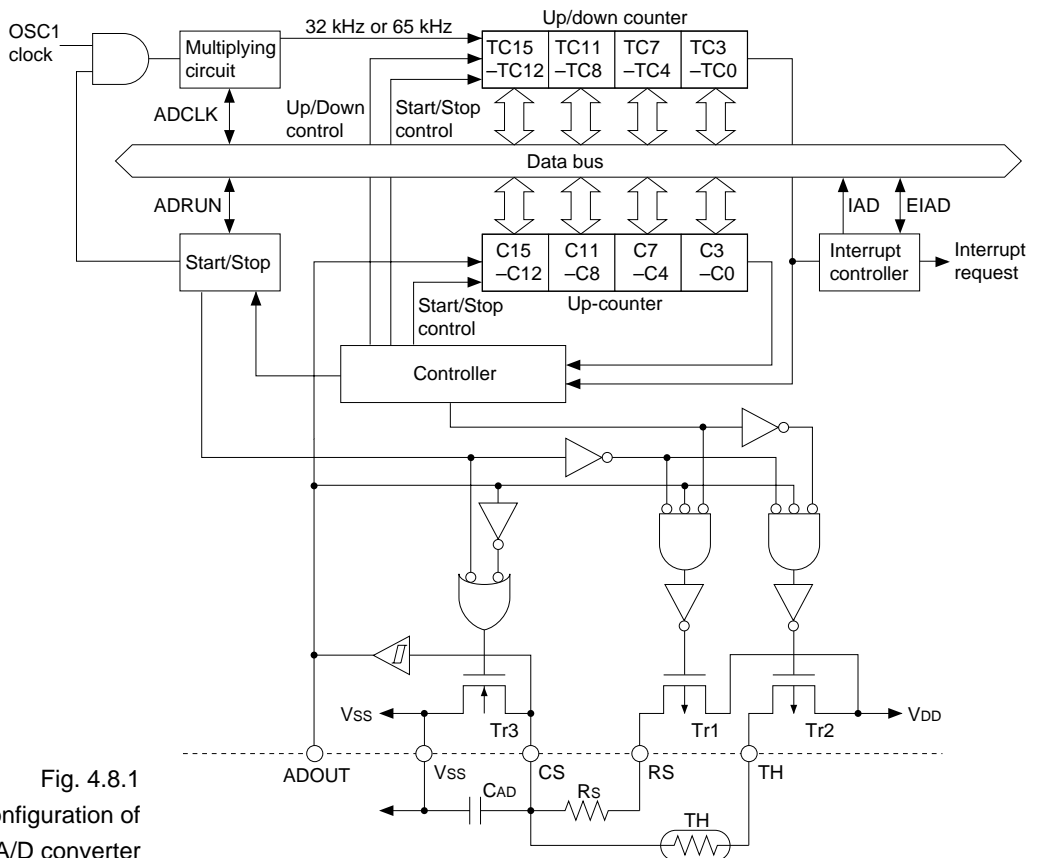


Fig. 4.8.1
Configuration of
A/D converter

Connect a reference resistance that only slightly changes resistance values according to environmental conditions between the oscillating I/O terminals RS and CS. Connect a sensor that changes resistance values between the TH and CS terminals. Furthermore, by connecting a condenser between the CS and VSS, a CR oscillation circuit is completed.

Operation of A/D converter

This A/D converter performs CR oscillation using one of the two resistances connected to external devices. Their oscillation frequency serves as a clock from which the oscillation frequency is counted. Difference in counted oscillation frequency can be evaluated in terms of the difference between the respective resistance values. Measurement results can be obtained from the changes in resistance values after correcting the difference according to the program.

(1) External resistances and condenser

Connect a sensor (a variable resistance element such as a thermistor) between the TH and CS terminals.

Next, set the reference value of the item to be measured (e.g. reference temperature in the case of temperature measurement) and connect the reference resistance equivalent to the sensor resistance value at the above reference value between the RS and CS terminals. An element that does not change due to temperature or other environmental conditions must be used as the reference resistance.

Connect an oscillating condenser that is used for CR oscillation of both the reference resistance and the sensor between the CS and VSS terminals.

(2) Oscillation circuit

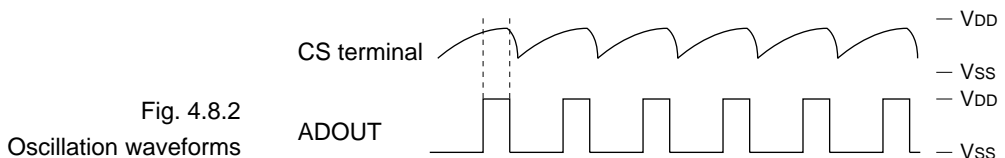
The CR oscillation circuit is designed so that either the reference resistance side or the sensor side can be operated independently by the oscillation control circuit. A/D conversion begins when "1" is written in the ADRUN register (0F1H D0). At the same time, the oscillation circuit also turns on. At first, the circuit of the reference resistance side (RS) is operated by the oscillation control circuit. Then, the circuit of the sensor side (TH) turns on when counting by the oscillation clock of the reference resistance is terminated.

Each circuit performs the same oscillating operation as follows:

The Tr1 (Tr2) turns on first, and the condenser connected between the CS and VSS terminals is charged through the reference resistance (sensor). If the voltage level of the CS terminal decreases, the Tr1 (Tr2) turns off and the Tr3 turns on. As a result, the condenser becomes discharged, and oscillation is performed according to CR time constant. The time constant changes as the sensor resistance value fluctuates, producing a difference from the oscillation frequency of the reference resistance.

Oscillation waveforms are shaped by the Schmitt trigger and transmitted to counter. The clock transmitted to the counter is also output from the ADOUT terminal. As a result, oscillation frequency can be identified by the oscilloscope. Since this monitor has no effect on oscillation frequency, it can be used to adjust CR oscillation frequency.

Oscillation waveforms and waveforms output from the ADOUT terminal are shown in Figure 4.8.2.



(3) Counter

The A/D converter incorporates two types of 16-bit counters. One is the up-counter C0-C15 that counts the aforementioned oscillation clock, and the other is up/down counter TC0-TC15 that counts the internal clock for reference counting. Each counter permits reading and writing on a 4-bit basis.

The input unit of the up/down counter TC0-TC15 incorporates a multiplying circuit so that either the OSC1 clock (Typ. 32.768 kHz) or its multiplication clock (Typ. 65.536 kHz) can be selected as an input clock.

When A/D conversion is initiated by the ADRUN register, oscillation by the reference resistance begins first, and the up-counter C0-C15 starts counting up according to the oscillation clock. At the same time, the up/down counter TC0-TC15 starts counting up.

Timing in starting oscillation and starting counting up are shown in Figure 4.8.3.

The up-counter becomes ENABLE at the falling edge of the first clock after CR oscillation is initiated and starts counting up from the falling edge of the next clock.

The up/down counter becomes ENABLE at the falling edge of the internal clock which is input immediately after the first CR oscillation clock has fallen. Then, it starts counting up from the falling edge of the next internal clock.

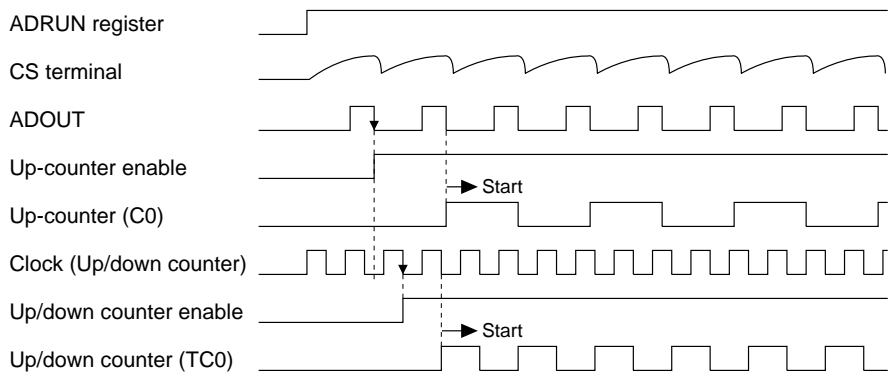


Fig. 4.8.3
Counting up start
timing

If the up-counter C0–C15 becomes "0000H" due to overflow, the sensor side of the oscillation circuit turns on, and the up-counter starts counting up according to the oscillation clock on the sensor side.

The up/down counter TC0–TC15 shifts to the counting-down mode at this point and starts counting down from the value measured as a result of oscillation by the reference resistance.

Timing in starting counting when oscillation is switched, is same as Figure 4.8.3.

When the up/down counter TC0–TC15 has counted down to "0000H", the counting operation of both counters and CR oscillation stops, and an interrupt occurs. At the same time, the ADRUN register is set to "0", and the A/D converter circuit stops operation completely.

The sensor is oscillated for the same period of time as the reference resistance is oscillated after the up/down counter TC0–TC15 is set to "0000H" prior to A/D conversion. Therefore, the difference in oscillation frequency can be measured from the values counted by the up-counter C0–C15.

Since the reference resistance is oscillated until the up-counter C0–C15 overflows, an appropriate initial value needs to be set before A/D conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. Likewise, if the input clock of the up/down counter TC0–TC15 is set at 65 kHz, the degree of precision is reduced. However, since CR oscillation frequency is normally set lower than the clock frequency of the up/down counter TC0–TC15 to ensure accurate measurement, the up/down counter TC0–TC15 may overflow while counting the oscillation frequency of the reference resistance.

If an overflow occurs, CR oscillation and A/D conversion is terminated immediately. Also in such cases, the up/down counter indicates "0000H", and interrupt occurs. However, it is impossible to judge whether the interrupt has occurred due to an overflow or normal termination.

Note that correct measurement is impossible if an overflow occurs. The initial value to be set depends on the measurable range by the sensor or where to set the reference resistance value within that range.

The initial value must be set taking the above into consideration.

Convert the initial value into a complement (value subtracted from 0000H) before setting it on the up-counter C0–C15. Since the data output from the up-counter C0–C15 after A/D conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value. The above operations are shown in Figure 4.8.4.

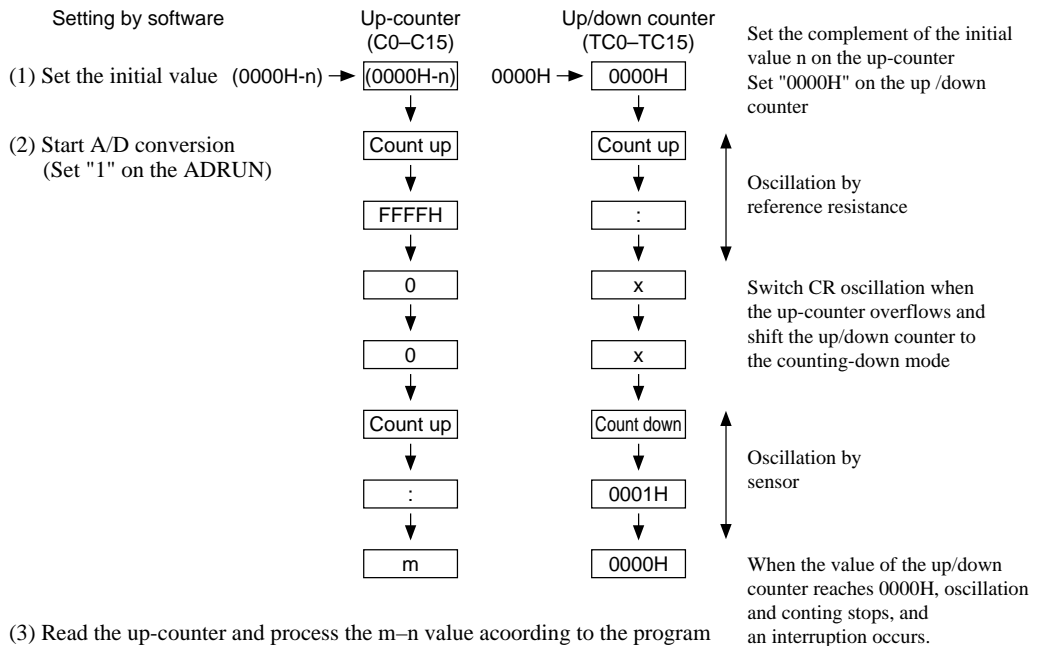


Fig. 4.8.4

Sequence of A/D conversion

Note - Set the initial value of the up-counter C0–C15 taking into account the measurable range and the overflow of the up/down counter TC0–TC15.

- If the up/down counter TC0–TC15 is measured after A/D conversion, it may not indicate "0000H". This is not due to incorrect timing in terminating A/D conversion but because the counting down clock is input after the control signal is output to the up-counter to terminate counting.

Interrupt function

The A/D converter has a function which allows interrupt to occur after A/D conversion.

When the up/down counter TC0-TC15 is counted down to "0000H", both counters stop counting. The interrupt factor flag IAD is set to "1" at the falling edge of the next clock. If the up/down counter TC0-TC15 overflow during counting-up operation, the interrupt factor flag is set to "1" at the rising edge of the clock immediately after the counter reaches "0000H".

This interrupt factor allows masking by the interrupt mask register EIAD. If the EIAD is set at "1", an interrupt occurs in the CPU. If the EIAD is set at "0", the interrupt factor flag is set to "1". However, no interrupt will occur in the CPU. The interrupt factor flag is reset to "0" by a reading operation.

Timing of interrupt by the A/D converter is shown in Figure 4.8.5.

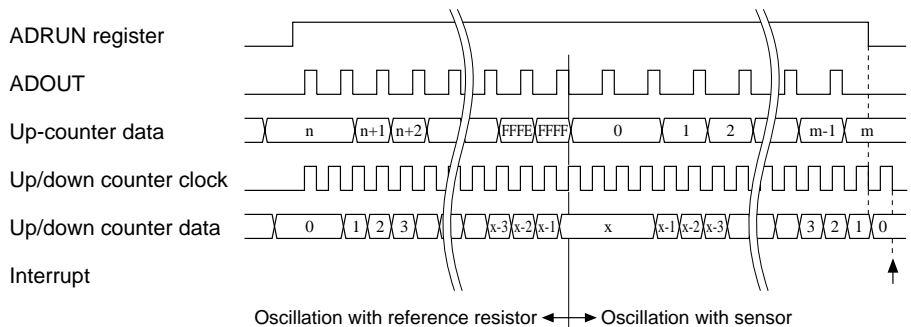


Fig. 4.8.5
Timing of A/D
converter interrupt

Usage example of the A/D converter

Temperature measurement is possible with the A/D converter in which a thermistor is used as a sensor. Elements to be connected and counter setting in the case of temperature measurement are as follows:

Example: Temperature measurement at -20°C to 70°C
Reference resistance 49.8 kΩ
Thermistor 50 kΩ
Oscillating condenser 2,200 pF

When the above elements are connected, the oscillation frequency of the reference resistance becomes about 10 kHz, and the oscillation frequency of the thermistor varies within the range of about 1 kHz to 50 kHz at -20°C to 70°C. Reference resistance is adjusted to the thermistor resistance value at 25°C.

In addition, Figure 4.8.6 indicates the resistance and oscillation frequency ratio TYP at the time of A/D conversion.

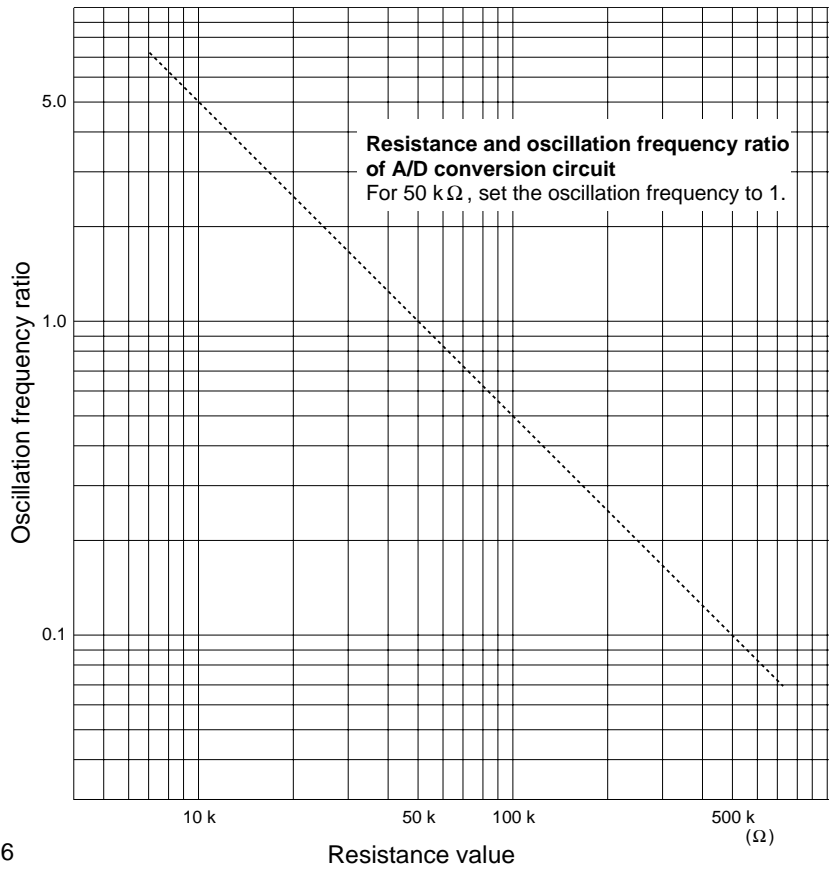


Fig. 4.8.6
Resistance and oscillation frequency ratio

Control of A/D
converter

Table 4.8.2 shows the A/D converter control bits and their addresses.

Table 4.8.2 Control bits of clock timer

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment | |
|---------|----------|------|------|-------|-------|---------|--------|--------|-----------------------------------|----|
| | D3 | D2 | D1 | D0 | | | | | | |
| 0E4H | TC3 | TC2 | TC1 | TC0 | TC3 | – *3 | 1 | 0 | Up/down counter data TC3 | |
| | R/W | | | | TC2 | – *3 | 1 | 0 | Up/down counter data TC2 | |
| | | | | | TC1 | – *3 | 1 | 0 | Up/down counter data TC1 | |
| | R/W | | | | TC0 | – *3 | 1 | 0 | Up/down counter data TC0 (LSB) | |
| | | | | | | | | | | |
| 0E5H | TC7 | TC6 | TC5 | TC4 | TC7 | – *3 | 1 | 0 | Up/down counter data TC7 | |
| | R/W | | | | TC6 | – *3 | 1 | 0 | Up/down counter data TC6 | |
| | | | | | TC5 | – *3 | 1 | 0 | Up/down counter data TC5 | |
| | R/W | | | | TC4 | – *3 | 1 | 0 | Up/down counter data TC4 | |
| | | | | | | | | | | |
| 0E6H | TC11 | TC10 | TC9 | TC8 | TC11 | – *3 | 1 | 0 | Up/down counter data TC11 | |
| | R/W | | | | TC10 | – *3 | 1 | 0 | Up/down counter data TC10 | |
| | | | | | TC9 | – *3 | 1 | 0 | Up/down counter data TC9 | |
| | R/W | | | | TC8 | – *3 | 1 | 0 | Up/down counter data TC8 | |
| | | | | | | | | | | |
| 0E7H | TC15 | TC14 | TC13 | TC12 | TC15 | – *3 | 1 | 0 | Up/down counter data TC15 (MSB) | |
| | R/W | | | | TC14 | – *3 | 1 | 0 | Up/down counter data TC14 | |
| | | | | | TC13 | – *3 | 1 | 0 | Up/down counter data TC13 | |
| | R/W | | | | TC12 | – *3 | 1 | 0 | Up/down counter data TC12 | |
| | | | | | | | | | | |
| 0F5H | C3 | C2 | C1 | C0 | C3 | – *3 | 1 | 0 | Up-counter data C3 | |
| | R/W | | | | C2 | – *3 | 1 | 0 | Up-counter data C2 | |
| | | | | | C1 | – *3 | 1 | 0 | Up-counter data C1 | |
| | R/W | | | | C0 | – *3 | 1 | 0 | Up-counter data C0 (LSB) | |
| | | | | | | | | | | |
| 0F6H | C7 | C6 | C5 | C4 | C7 | – *3 | 1 | 0 | Up-counter data C7 | |
| | R/W | | | | C6 | – *3 | 1 | 0 | Up-counter data C6 | |
| | | | | | C5 | – *3 | 1 | 0 | Up-counter data C5 | |
| | R/W | | | | C4 | – *3 | 1 | 0 | Up-counter data C4 | |
| | | | | | | | | | | |
| 0F7H | C11 | C10 | C9 | C8 | C11 | – *3 | 1 | 0 | Up-counter data C11 | |
| | R/W | | | | C10 | – *3 | 1 | 0 | Up-counter data C10 | |
| | | | | | C9 | – *3 | 1 | 0 | Up-counter data C9 | |
| | R/W | | | | C8 | – *3 | 1 | 0 | Up-counter data C8 | |
| | | | | | | | | | | |
| 0F8H | C15 | C14 | C13 | C12 | C15 | – *3 | 1 | 0 | Up-counter data C15 (MSB) | |
| | R/W | | | | C14 | – *3 | 1 | 0 | Up-counter data C14 | |
| | | | | | C13 | – *3 | 1 | 0 | Up-counter data C13 | |
| | R/W | | | | C12 | – *3 | 1 | 0 | Up-counter data C12 | |
| | | | | | | | | | | |
| 0F1H | 0 | 0 | 0 | ADRUN | 0 | | | | *5 | |
| | R | | | R/W | ADRUN | 0 | Start | Stop | A/D conversion Start/Stop | *5 |
| | | | | | | | | | *5 | |
| 0FEH | 0 | 0 | 0 | ADCLK | 0 | | | | *5 | |
| | R | | | R/W | ADCLK | 0 | 65 kHz | 32 kHz | A/D clock selection 65 kHz/32 kHz | *5 |
| | | | | | | | | | *5 | |
| 0ECH | 0 | 0 | 0 | EIAD | 0 | | | | *5 | |
| | R | | | R/W | EIAD | 0 | Enable | Mask | Interrupt mask register (A/D) | *5 |
| | | | | | | | | | *5 | |
| 0F0H | 0 | 0 | 0 | IAD | 0 | | | | *5 | |
| | R | | | R/W | IAD | 0 | Yes | No | Interrupt factor flag (A/D) | *5 |
| | | | | | | | | | *5 | |

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

TC0–TC15 Up/down counter (0E4H–0E7H)

Writing and reading is possible on a 4-bit basis by the up/down counter that is used to adjust the CR oscillation time between the reference resistance and the variable resistance elements.

The up/down counter counts up during oscillation of the reference resistance and counts down from the value it reached when counting up to "0000H" during oscillation of the sensor.

"0000H" needs to be entered in the counter prior to A/D conversion in order to adjust the counting time of both counts.

After an initial reset, data in this counter become indefinite.

C0–C15 Up-counter (0F5H–0F8H)

This counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis.

The complement of the number of clocks to be counted by the oscillation of the reference resistance, must be entered in this counter prior to A/D conversion.

If A/D conversion is initiated, the counter counts up from the set initial value, first according to the oscillation clock of the reference resistance. When the counter reaches "0000H" due to overflow, the oscillation of the reference resistance stops, and the sensor starts oscillating. The counter continues counting according to the sensor oscillation clock.

Counting time during the oscillation of the reference resistance is calculated by the up/down counter TC0–TC15. Up-counter C0–C15 stops counting when the same period of time elapses. Difference from the reference resistance can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above difference according to the program.

Measurable range and the overflow of the up/down counter TC0–TC15 must be taken into account when setting an initial value to be entered prior to A/D conversion.

After an initial reset, data in this counter become indefinite.

ADCLK Input clock selection (0FEH D0)

Select the input clock of the up/down counter TC0–TC15.

When "1" is written: 65 kHz

When "0" is written: 32 kHz

Reading: Valid

Select the output clock of the multiplying circuit for the counting operation of the up/down counter TC0–TC15.

When "1" is written in the ADCLK, 65 kHz, a multitude of the OSC1 clock is selected. When "0" is written, the OSC1 clock is selected at 32 kHz.

If 65 kHz is selected, A/D conversion becomes more accurate. However, the initial value must be set on the up-counter C0–C15 so that the up/down counter TC0–TC15 will not overflow while CR oscillation is being counted.

After an initial reset, ADCLK is set to "0".

ADRUN A/D conversion START/STOP (0F1H D0)

Start A/D conversion.

When "1" is written: A/D conversion starts

When "0" is written: A/D conversion stops

Reading: Valid

When "1" is written in the ADRUN, A/D conversion begins.

The register remains at "1" during A/D conversion and is set to "0" when A/D conversion is terminated.

When "0" is written in the ADRUN during A/D conversion, A/D conversion is paused.

ADRUN is set to "0" at initial reset, when the up/down counter overflows or when measurement is finished.

EIAD Interrupt mask register (0ECH D0)

Select whether to mask interrupt with the A/D converter.

When "1" is written: Enable

When "0" is written: Mask

Reading: Valid

The A/D converter interrupt is permitted when "1" is written in the EIAD. When "0" is written, interrupt is masked.

After an initial reset, this register is set to "0".

IAD Interrupt factor flag (0F0H D0)

This flag indicates interrupt caused by the A/D converter.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

Writing: Invalid

IAD is set to "1" when A/D conversion is terminated (when the up/down counter counted up or down to "0000H"). From the status of this flag, the software can decide whether an A/D converter interrupt has occurred.

This flag is reset when the software has read it.

Reading of interrupt factor flag is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

After an initial reset, this flag is set to "0".

4.9 Heavy Load Protection Function

Operation of heavy load protection function

The S1C60N02 Series has a heavy load protection function for when the battery load becomes heavy and the supply voltage drops, such as when an external buzzer sounds or an external lamp lights. This function works in the heavy load protection mode.

The normal mode changes to the heavy load protection mode in the following case:

- When the software changes the mode to the heavy load protection mode (HLMOD = "1")

In the heavy load protection mode, the internally regulated voltage is switched to the high-stability mode from the low current consumption mode. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

Control of heavy load protection function

Table 4.9.1 shows the control bits and their addresses for the heavy load protection function.

Table 4.9.1 Control bits for heavy load protection function

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|----------|----|----|----|-------|---------|-------|--------|-------------------------------------|
| | D3 | D2 | D1 | D0 | | | | | |
| 0FAH | HLMOD | 0 | 0 | 0 | HLMOD | 0 | Heavy | Normal | Heavy load protection mode register |
| | R/W | R | | | 0 | | | | *5 |
| | | | | | 0 | | | | *5 |
| | | | | 0 | | | | *5 | |

- *1 Initial value following initial reset
- *2 Not set in the circuit
- *3 Undefined
- *4 Reset (0) immediately after being read
- *5 Always "0" when being read
- *6 Refer to main manual

HLMOD Heavy load protection mode on/off (0FAH D3)

When "1" is written: Heavy load protection mode on
 When "0" is written: Heavy load protection mode off
 Reading: Valid

When HLMOD is set to "1", the IC enters the heavy load protection mode.

In the heavy load protection mode, the consumed current becomes larger. Unless necessary, do not select the heavy load protection mode with the software.

4.10 Interrupt and HALT

The S1C60N02 Series provides the following interrupt settings, each of which is maskable.

External interrupt: Input interrupt (one)
 Internal interrupt: Timer interrupt (one)
 A/D converter interrupt (one)

To enable interrupts, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable). When an interrupt occurs, the interrupt flag is automatically reset to "0" (DI) and interrupts after that are inhibited.

When a HALT instruction is input, the CPU operating clock stops and the CPU enters the halt state. The CPU is reactivated from the halt state when an interrupt request occurs.

Figure 4.10.1 shows the configuration of the interrupt circuit.

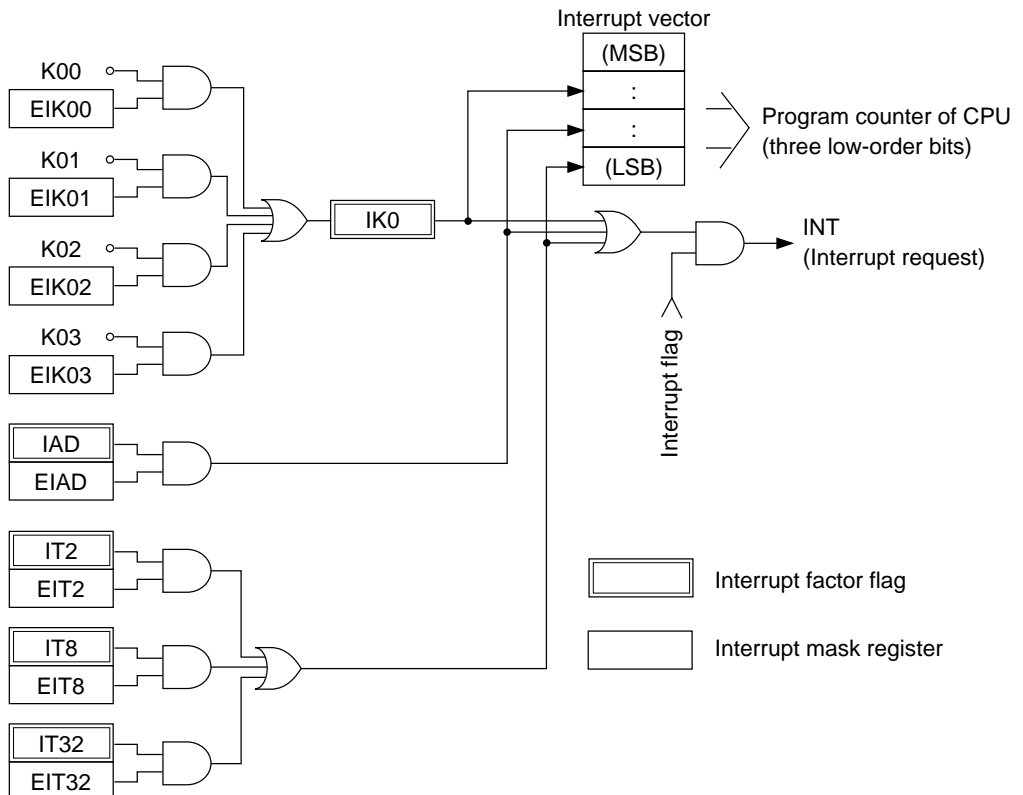


Fig. 4.10.1
 Configuration of
 interrupt circuit

Interrupt factors

Table 4.10.1 shows the factors that generate interrupt requests.

The interrupt factor flags are set to "1" depending on the corresponding interrupt factors.

The CPU is interrupted when the following two conditions occur and an interrupt factor flag is set to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read.

After an initial reset, the interrupt factor flags are reset to "0".

*Note Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.*

Table 4.10.1
Interrupt factors

| Interrupt factor | Interrupt factor flag |
|--|-----------------------|
| Colck timer 2 Hz falling edge | IT2 (0EFH D2) |
| Colck timer 8 Hz falling edge | IT8 (0EFH D1) |
| Colck timer 32 Hz falling edge | IT32 (0EFH D0) |
| A/D converter A/D conversion completion | IAD (0F0H D0) |
| Input data (K00–K03) Rising edge | IK0 (0EDH D0) |

Specific masks and factor flags for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers. The interrupt mask registers are read/write registers. They are enabled (interrupt enabled) when "1" is written to them, and masked (interrupt disabled) when "0" is written to them. After an initial reset, the interrupt mask register is set to "0".

Table 4.10.2 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.10.2
Interrupt mask registers and
interrupt factor flags

| Interrupt mask register | | Interrupt factor flag | |
|-------------------------|-----------|-----------------------|-----------|
| EIT2 | (0EBH D2) | IT2 | (0EFH D2) |
| EIT8 | (0EBH D1) | IT8 | (0EFH D1) |
| EIT32 | (0EBH D0) | IT32 | (0EFH D0) |
| EIAD | (0ECH D0) | IAD | (0F0H D0) |
| EIK03* | (0E8H D3) | IK0 | (0EDH D0) |
| EIK02* | (0E8H D2) | | |
| EIK01* | (0E8H D1) | | |
| EIK00* | (0E8H D0) | | |

* There is an interrupt mask register for each input port pin.

Interrupt vectors

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is suspended, interrupt processing is executed in the following order:

- ① The address data (value of the program counter) of the program step to be executed next is saved on the stack (RAM).
- ② The interrupt request causes the value of the interrupt vector (page 1, 01H-07H) to be loaded into the program counter.
- ③ The program at the specified address is executed (execution of interrupt processing routine).

Note The processing in steps 1 and 2, above, takes 12 cycles of the CPU system clock.

Control of interrupt Table 4.10.3 shows the interrupt control bits and their addresses.

Table 4.10.3 Interrupt control bits

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|----------|-------|-------|-------|-------|---------|--------|--|---|
| | D3 | D2 | D1 | D0 | | | | | |
| 0E8H | EIK03 | EIK02 | EIK01 | EIK00 | EIK03 | 0 | Enable | Mask | Interrupt mask register K03 |
| | | | | | EIK02 | 0 | Enable | Mask | Interrupt mask register K02 |
| | R/W | | | | EIK01 | 0 | Enable | Mask | Interrupt mask register K01 |
| | | | | | EIK00 | 0 | Enable | Mask | Interrupt mask register K00 |
| 0EBH | 0 | EIT2 | EIT8 | EIT32 | 0 | 0 | Enable | Mask | Interrupt mask register (clock timer) 2 Hz *5 |
| | R | R/W | | | EIT8 | 0 | Enable | Mask | Interrupt mask register (clock timer) 8 Hz |
| | | | | | EIT32 | 0 | Enable | Mask | Interrupt mask register (clock timer) 32 Hz |
| 0ECH | 0 | 0 | 0 | EIAD | 0 | | | | *5 |
| | R | | | | 0 | | | | *5 |
| | | | | | 0 | | | | *5 |
| | | | | EIAD | 0 | Enable | Mask | Interrupt mask register (A/D) | |
| 0EDH | 0 | 0 | 0 | IK0 | 0 | | | | *5 |
| | R | | | | 0 | | | | *5 |
| | | | | | 0 | | | | *5 |
| | | | | IK0 | 0 | Yes | No | Interrupt factor flag (K00–K03) | *4 |
| 0EFH | 0 | IT2 | IT8 | IT32 | 0 | | | | *5 |
| | R | | | | IT2 | 0 | Yes | No | Interrupt factor flag (clock timer) 2 Hz *4 |
| | | | | | IT8 | 0 | Yes | No | Interrupt factor flag (clock timer) 8 Hz *4 |
| | | | | IT32 | 0 | Yes | No | Interrupt factor flag (clock timer) 32 Hz *4 | |
| 0F0H | 0 | 0 | 0 | IAD | 0 | | | | *5 |
| | R | | | | 0 | | | | *5 |
| | | | | | 0 | | | | *5 |
| | | | | IAD | 0 | Yes | No | Interrupt factor flag (A/D) | *4 |

- *1 Initial value following initial reset
- *2 Not set in the circuit
- *3 Undefined
- *4 Reset (0) immediately after being read
- *5 Always "0" when being read
- *6 Refer to main manual

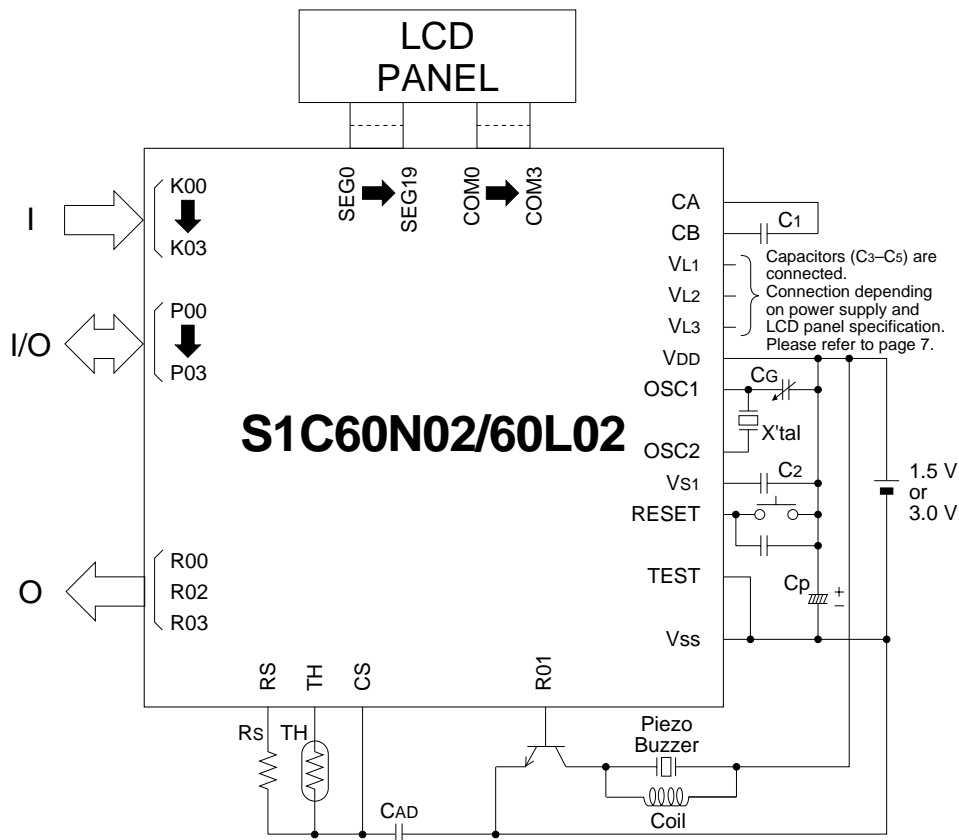
EIT32, EIT8, EIT2 Interrupt mask registers (0EBH D0–D2)
 IT32, IT8, IT2 Interrupt factor flags (0EFH D0–D2)
 See 4.7, "Clock Timer".

EIAD Interrupt mask register (0ECH D0)
 IAD Interrupt factor flag (0F0H D0)
 See 4.8, "A/D Converter".

EIK00–EIK03 Interrupt mask registers (0E8H)
 IK0 Interrupt factor flag (0EDH D0)
 See 4.3, "Input Ports".

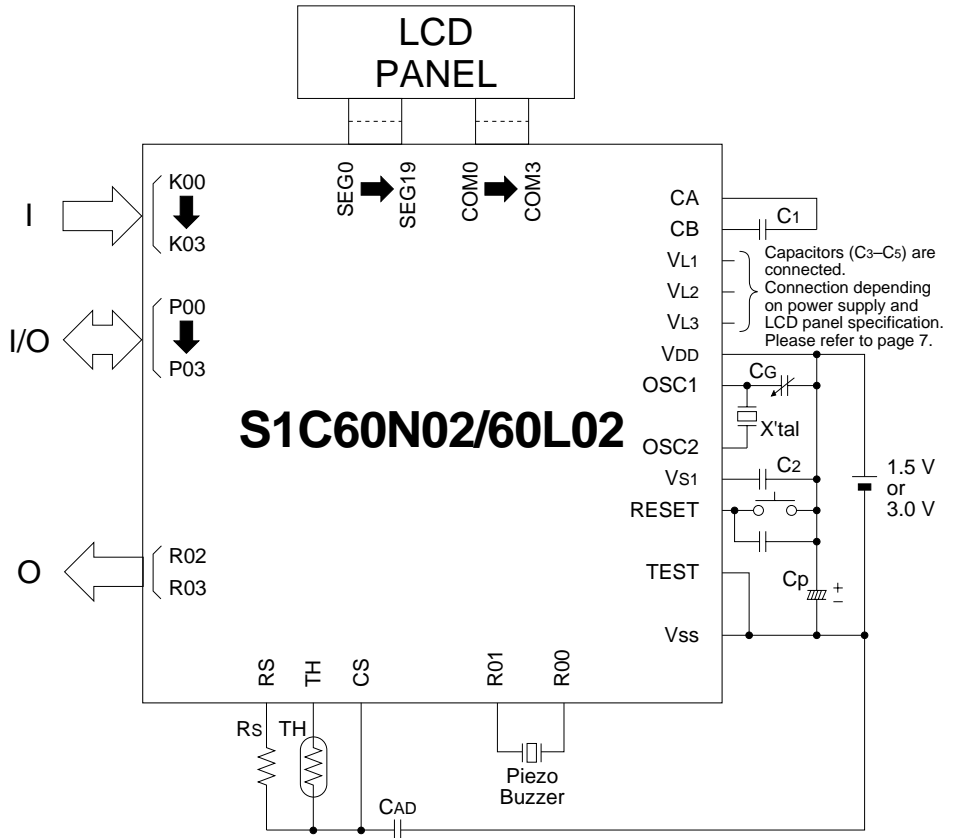
CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM

(1) Piezo Buzzer Single Terminal Driving



| | | | |
|-------|--------------------|-----------|-----------------|
| X'tal | Crystal oscillator | 32,768 Hz | CI(MAX) = 35 kΩ |
| CG | Trimmer capacitor | 5–25 pF | |
| C1–C5 | Capacitor | 0.1 μF | |
| Cp | Capacitor | 3.3 μF | |
| TH | Thermistor | 50 kΩ | |
| Rs | Resistor | 49.8 kΩ | |
| CAD | Capacitor | 2,200 pF | |

(2) Piezo Buzzer Direct Driving



| | | | |
|-------|--------------------|-----------|-----------------|
| X'tal | Crystal oscillator | 32,768 Hz | CI(MAX) = 35 kΩ |
| CG | Trimmer capacitor | 5–25 pF | |
| C1–C5 | Capacitor | 0.1 μF | |
| Cp | Capacitor | 3.3 μF | |
| TH | Thermistor | 50 kΩ | |
| Rs | Resistor | 49.8 kΩ | |
| CAD | Capacitor | 2,200 pF | |

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

S1C60N02

(V_{DD}=0V)

| Item | Symbol | Rated value | Unit |
|-------------------------------------|-------------------|-----------------------------|------|
| Power voltage | V _{SS} | -5.0 to 0.5 | V |
| Input voltage (1) | V _I | V _{SS} -0.3 to 0.5 | V |
| Input voltage (2) | V _{IOSC} | V _{SS} -0.3 to 0.5 | V |
| Operating temperature | T _{opr} | -20 to 70 | °C |
| Storage temperature | T _{stg} | -65 to 150 | °C |
| Soldering temperature / Time | T _{sol} | 260°C, 10sec (lead section) | – |
| Allowable dissipation ^{*1} | PD | 250 | mW |

*1 In case of QFP6-60 pin plastic package

S1C60L02

(V_{DD}=0V)

| Item | Symbol | Rated value | Unit |
|-------------------------------------|-------------------|-----------------------------|------|
| Power voltage | V _{SS} | -5.0 to 0.5 | V |
| Input voltage (1) | V _I | V _{SS} -0.3 to 0.5 | V |
| Input voltage (2) | V _{IOSC} | V _{SS} -0.3 to 0.5 | V |
| Operating temperature | T _{opr} | -20 to 70 | °C |
| Storage temperature | T _{stg} | -65 to 150 | °C |
| Soldering temperature / Time | T _{sol} | 260°C, 10sec (lead section) | – |
| Allowable dissipation ^{*1} | PD | 250 | mW |

*1 In case of QFP6-60 pin plastic package

6.2 Recommended Operating Conditions

S1C60N02

(Ta=-20 to 70°C)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|-------------------------------|--------|-------------------------|------|--------|------|------|
| Power voltage | VSS | VDD=0V | -3.5 | -3.0 | -1.8 | V |
| Oscillation frequency | fOSC1 | Crystal oscillation | | 32,768 | | Hz |
| | fOSC2 | CR oscillation, R=420kΩ | | 65 | 80 | kHz |
| Booster capacitor | C1 | | 0.1 | | | μF |
| Capacitor between VDD and VS1 | C2 | | 0.1 | | | μF |

S1C60L02

(Ta=-20 to 70°C)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|-------------------------------|--------|---|------|--------|---------|------|
| Power voltage | VSS | VDD=0V *3 | -2.0 | -1.5 | -1.2 | V |
| | | VDD=0V, With software correspondence *1 | -2.0 | -1.5 | -0.9 *2 | V |
| Oscillation frequency | fOSC1 | Crystal oscillation | | 32,768 | | Hz |
| | fOSC2 | CR oscillation, R=420kΩ | | 65 | 80 | kHz |
| Booster capacitor | C1 | | 0.1 | | | μF |
| Capacitor between VDD and VS1 | C2 | | 0.1 | | | μF |

*1 When switching to the heavy load protection mode.

(For details, refer to Section 4.9).

*2 The voltage which can be displayed on the LCD panel will differ according to the characteristics of the LCD panel.

*3 When there is no software correspondence during CR oscillation or crystal oscillation.

6.3 DC Characteristics

S1C60N02

Unless otherwise specified

$V_{DD}=0\text{ V}$, $V_{SS}=-3.0\text{ V}$, $f_{osc}=32,768\text{ Hz}$, $T_a=25^\circ\text{C}$, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1\ \mu\text{F}$

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|-----------|--|---------------------|-----|---------------------|---------------|
| High level input voltage (1) | V_{IH1} | K00–K03, P00–P03 | $0.2 \cdot V_{SS}$ | | 0 | V |
| High level input voltage (2) | V_{IH2} | RESET, TEST | $0.15 \cdot V_{SS}$ | | 0 | V |
| Low level input voltage (1) | V_{IL1} | K00–K03, P00–P03 | V_{SS} | | $0.8 \cdot V_{SS}$ | V |
| Low level input voltage (2) | V_{IL2} | RESET, TEST | V_{SS} | | $0.85 \cdot V_{SS}$ | V |
| High level input current (1) | I_{IH1} | $V_{IH1}=0\text{V}$ Without pull down resistor | 0 | | 0.5 | μA |
| High level input current (2) | I_{IH2} | $V_{IH2}=0\text{V}$ With pull down resistor | 5 | | 16 | μA |
| High level input current (3) | I_{IH3} | $V_{IH3}=0\text{V}$ With pull down resistor | 30 | | 100 | μA |
| Low level input current | I_{IL} | $V_{IL}=V_{SS}$ | -0.5 | | 0 | μA |
| High level output current (1) | I_{OH1} | $V_{OH1}=0.1 \cdot V_{SS}$ | | | -1.0 | mA |
| High level output current (2) | I_{OH2} | $V_{OH2}=0.1 \cdot V_{SS}$ (built-in protection resistance) | | | -1.0 | mA |
| High level output current (3) | I_{OH3} | $V_{OH3}=-1.0\text{V}$ | | | -1.0 | mA |
| Low level output current (1) | I_{OL1} | $V_{OL1}=0.9 \cdot V_{SS}$ | 3.0 | | | mA |
| Low level output current (2) | I_{OL2} | $V_{OL2}=0.9 \cdot V_{SS}$ (built-in protection resistance) | 3.0 | | | mA |
| Low level output current (3) | I_{OL3} | $V_{OL3}=-2.0\text{V}$ | 3.0 | | | mA |
| Common output current | I_{OH4} | $V_{OH4}=-0.05\text{V}$ | | | -3 | μA |
| | I_{OL4} | $V_{OL4}=V_{L3}+0.05\text{V}$ | 3 | | | μA |
| Segment output current (during LCD output) | I_{OH5} | $V_{OH5}=-0.05\text{V}$ | | | -3 | μA |
| | I_{OL5} | $V_{OL5}=V_{L3}+0.05\text{V}$ | 3 | | | μA |
| Segment output current (during DC output) | I_{OH6} | $V_{OH6}=0.1 \cdot V_{SS}$ | | | -300 | μA |
| | I_{OL6} | $V_{OL6}=0.9 \cdot V_{SS}$ | 300 | | | μA |

S1C60L02

Unless otherwise specified

$V_{DD}=0\text{ V}$, $V_{SS}=-1.5\text{ V}$, $f_{osc}=32,768\text{ Hz}$, $T_a=25^\circ\text{C}$, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1\ \mu\text{F}$

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|-----------|--|---------------------|-----|---------------------|---------------|
| High level input voltage (1) | V_{IH1} | K00–K03, P00–P03 | $0.2 \cdot V_{SS}$ | | 0 | V |
| High level input voltage (2) | V_{IH2} | RESET, TEST | $0.15 \cdot V_{SS}$ | | 0 | V |
| Low level input voltage (1) | V_{IL1} | K00–K03, P00–P03 | V_{SS} | | $0.8 \cdot V_{SS}$ | V |
| Low level input voltage (2) | V_{IL2} | RESET, TEST | V_{SS} | | $0.85 \cdot V_{SS}$ | V |
| High level input current (1) | I_{IH1} | $V_{IH1}=0\text{V}$ Without pull down resistor | 0 | | 0.5 | μA |
| High level input current (2) | I_{IH2} | $V_{IH2}=0\text{V}$ With pull down resistor | 2.0 | | 16 | μA |
| High level input current (3) | I_{IH3} | $V_{IH3}=0\text{V}$ With pull down resistor | 9.0 | | 100 | μA |
| Low level input current | I_{IL} | $V_{IL}=V_{SS}$ | -0.5 | | 0 | μA |
| High level output current (1) | I_{OH1} | $V_{OH1}=0.1 \cdot V_{SS}$ | | | -200 | μA |
| High level output current (2) | I_{OH2} | $V_{OH2}=0.1 \cdot V_{SS}$ (built-in protection resistance) | | | -200 | μA |
| High level output current (3) | I_{OH3} | $V_{OH3}=-0.5\text{V}$ | | | -200 | μA |
| Low level output current (1) | I_{OL1} | $V_{OL1}=0.9 \cdot V_{SS}$ | 700 | | | μA |
| Low level output current (2) | I_{OL2} | $V_{OL2}=0.9 \cdot V_{SS}$ (built-in protection resistance) | 700 | | | μA |
| Low level output current (3) | I_{OL3} | $V_{OL3}=-1.0\text{V}$ | 700 | | | μA |
| Common output current | I_{OH4} | $V_{OH4}=-0.05\text{V}$ | | | -3 | μA |
| | I_{OL4} | $V_{OL4}=V_{L3}+0.05\text{V}$ | 3 | | | μA |
| Segment output current (during LCD output) | I_{OH5} | $V_{OH5}=-0.05\text{V}$ | | | -3 | μA |
| | I_{OL5} | $V_{OL5}=V_{L3}+0.05\text{V}$ | 3 | | | μA |
| Segment output current (during DC output) | I_{OH6} | $V_{OH6}=0.1 \cdot V_{SS}$ | | | -100 | μA |
| | I_{OL6} | $V_{OL6}=0.9 \cdot V_{SS}$ | 130 | | | μA |

6.4 Analog Circuit Characteristics and Power Current Consumption

S1C60N02 (Normal Operating Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-3.0$ V, $f_{osc}=32,768$ Hz, $T_a=25^{\circ}\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---|----------------------------|----------|------------------------------------|---------------|
| Internal voltage | V_{L1} | Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L1} (without panel load) | $1/2 \cdot V_{L2}$ -0.1 | | $1/2 \cdot V_{L2}$ $\times 0.9$ | V |
| | V_{L2} | Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L2} (without panel load) | | V_{SS} | | V |
| | V_{L3} | Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L3} (without panel load) | $3/2 \cdot V_{L2}$ -0.1 | | $3/2 \cdot V_{L2}$ $\times 0.9$ | V |
| Power current consumption | IOP | During HALT | | 1.0 | 2.5 | μA |
| | | During execution | Without panel load | 2.5 | 5.0 | μA |
| | | During A/D conversion (HALT) | | 30 | 40 | μA |

S1C60N02 (Heavy Load Protection Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-3.0$ V, $f_{osc}=32,768$ Hz, $T_a=25^{\circ}\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---|----------------------------|----------|-------------------------------------|---------------|
| Internal voltage | V_{L1} | Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L1} (without panel load) | $1/2 \cdot V_{L2}$ -0.1 | | $1/2 \cdot V_{L2}$ $\times 0.85$ | V |
| | V_{L2} | Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L2} (without panel load) | | V_{SS} | | V |
| | V_{L3} | Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L3} (without panel load) | $3/2 \cdot V_{L2}$ -0.1 | | $3/2 \cdot V_{L2}$ $\times 0.85$ | V |
| Power current consumption | IOP | During HALT | | 2.0 | 5.5 | μA |
| | | During execution | Without panel load | 5.5 | 10.0 | μA |
| | | During A/D conversion (HALT) | | 31 | 41.5 | μA |

S1C60L02 (Normal Operating Mode)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, fosc=32,768 Hz, Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=0.1 μF

(During A/D conversion: RS=49.8 kΩ, TH=50 kΩ, CAD=2,200 pF)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|--------|--|--------------------|-----|----------------|------|
| Internal voltage | VL1 | Connect 1MΩ load resistor between VDD and VL1 (without panel load) | | VSS | | V |
| | VL2 | Connect 1MΩ load resistor between VDD and VL2 (without panel load) | 2•VL1 -0.1 | | 2•VL1 × 0.9 | V |
| | VL3 | Connect 1MΩ load resistor between VDD and VL3 (without panel load) | 3•VL1 -0.1 | | 3•VL1 × 0.9 | V |
| Power current consumption | IOP | During HALT | | 1.0 | 2.5 | μA |
| | | During execution | Without panel load | 2.5 | 5.0 | μA |
| | | During A/D conversion (HALT) | | 30 | 40 | μA |

S1C60L02 (Heavy Load Protection Mode)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, fosc=32,768 Hz, Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=0.1 μF

(During A/D conversion: RS=49.8 kΩ, TH=50 kΩ, CAD=2,200 pF)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|--------|--|--------------------|-----|-----------------|------|
| Internal voltage | VL1 | Connect 1MΩ load resistor between VDD and VL1 (without panel load) | | VSS | | V |
| | VL2 | Connect 1MΩ load resistor between VDD and VL2 (without panel load) | 2•VL1 -0.1 | | 2•VL1 × 0.85 | V |
| | VL3 | Connect 1MΩ load resistor between VDD and VL3 (without panel load) | 3•VL1 -0.1 | | 3•VL1 × 0.85 | V |
| Power current consumption | IOP | During HALT | | 2.0 | 5.5 | μA |
| | | During execution | Without panel load | 5.5 | 10.0 | μA |
| | | During A/D conversion (HALT) | | 31 | 41.5 | μA |

S1C60N02 (CR, Normal Operating Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-3.0$ V, $f_{osc}=65$ kHz, $T_a=25^\circ\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF , Recommended external resistance for CR oscillation = 420 k Ω

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---|----------------------------|----------|------------------------------------|---------------|
| Internal voltage | V_{L1} | Connect 1M Ω load resistor between V_{DD} and V_{L1} (without panel load) | $1/2 \cdot V_{L2}$ -0.1 | | $1/2 \cdot V_{L2}$ $\times 0.9$ | V |
| | V_{L2} | Connect 1M Ω load resistor between V_{DD} and V_{L2} (without panel load) | | V_{SS} | | V |
| | V_{L3} | Connect 1M Ω load resistor between V_{DD} and V_{L3} (without panel load) | $3/2 \cdot V_{L2}$ -0.1 | | $3/2 \cdot V_{L2}$ $\times 0.9$ | V |
| Power current consumption | IOP | During HALT | Without panel load | 8.0 | 15.0 | μA |
| | | During execution | | 15.0 | 20.0 | μA |
| | | During A/D conversion (HALT) | | 37 | 52.5 | μA |

S1C60N02 (CR, Heavy Load Protection Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-3.0$ V, $f_{osc}=65$ kHz, $T_a=25^\circ\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF , Recommended external resistance for CR oscillation = 420 k Ω

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---|----------------------------|----------|-------------------------------------|---------------|
| Internal voltage | V_{L1} | Connect 1M Ω load resistor between V_{DD} and V_{L1} (without panel load) | $1/2 \cdot V_{L2}$ -0.1 | | $1/2 \cdot V_{L2}$ $\times 0.85$ | V |
| | V_{L2} | Connect 1M Ω load resistor between V_{DD} and V_{L2} (without panel load) | | V_{SS} | | V |
| | V_{L3} | Connect 1M Ω load resistor between V_{DD} and V_{L3} (without panel load) | $3/2 \cdot V_{L2}$ -0.1 | | $3/2 \cdot V_{L2}$ $\times 0.85$ | V |
| Power current consumption | IOP | During HALT | Without panel load | 16.0 | 30.0 | μA |
| | | During execution | | 30.0 | 40.0 | μA |
| | | During A/D conversion (HALT) | | 45 | 57.5 | μA |

S1C60L02 (CR, Normal Operating Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-1.5$ V, $f_{osc}=65$ kHz, $T_a=25^\circ\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF , Recommended external resistance for CR oscillation = 420 k Ω

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---|--------------------------|----------|----------------------------------|---------------|
| Internal voltage | V_{L1} | Connect 1M Ω load resistor between V_{DD} and V_{L1} (without panel load) | | V_{SS} | | V |
| | V_{L2} | Connect 1M Ω load resistor between V_{DD} and V_{L2} (without panel load) | $2 \cdot V_{L1}$ -0.1 | | $2 \cdot V_{L1}$ $\times 0.9$ | V |
| | V_{L3} | Connect 1M Ω load resistor between V_{DD} and V_{L3} (without panel load) | $3 \cdot V_{L1}$ -0.1 | | $3 \cdot V_{L1}$ $\times 0.9$ | V |
| Power current consumption | IOP | During HALT | Without panel load | 8.0 | 15.0 | μA |
| | | During execution | | 15.0 | 20.0 | μA |
| | | During A/D conversion (HALT) | | 37 | 52.5 | μA |

S1C60L02 (CR, Heavy Load Protection Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-1.5$ V, $f_{osc}=65$ kHz, $T_a=25^\circ\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF , Recommended external resistance for CR oscillation = 420 k Ω

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---|--------------------------|----------|-----------------------------------|---------------|
| Internal voltage | V_{L1} | Connect 1M Ω load resistor between V_{DD} and V_{L1} (without panel load) | | V_{SS} | | V |
| | V_{L2} | Connect 1M Ω load resistor between V_{DD} and V_{L2} (without panel load) | $2 \cdot V_{L1}$ -0.1 | | $2 \cdot V_{L1}$ $\times 0.85$ | V |
| | V_{L3} | Connect 1M Ω load resistor between V_{DD} and V_{L3} (without panel load) | $3 \cdot V_{L1}$ -0.1 | | $3 \cdot V_{L1}$ $\times 0.85$ | V |
| Power current consumption | IOP | During HALT | Without panel load | 16.0 | 30.0 | μA |
| | | During execution | | 30.0 | 40.0 | μA |
| | | During A/D conversion (HALT) | | 45 | 57.5 | μA |

6.5 Oscillation Characteristics

Oscillation characteristics will vary according to different conditions. Use the following characteristics as reference values.

S1C60N02

Unless otherwise specified

VDD=0 V, VSS=-3.0 V, Crystal: Q13MC146, CG=25 pF, CD=built-in, Ta=25°C

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---------------|---|------|-----|------|------|
| Oscillation start voltage | Vsta (Vss) | tsta≤5sec | -1.8 | | | V |
| Oscillation stop voltage | Vstp (Vss) | tstp≤10sec | -1.8 | | | V |
| Built-in capacity (drain) | CD | Including the parasitic capacity inside the IC | | 20 | | pF |
| Frequency voltage deviation | f/V | Vss=-1.8 to -3.5V | | | 5 | ppm |
| Frequency IC deviation | f/IC | | -10 | | 10 | ppm |
| Frequency adjustment range | f/CG | CG=5-25pF | 40 | | | ppm |
| Higher harmonic oscillation start voltage | Vhho (Vss) | CG=5pF | | | -3.6 | V |
| Allowable leak resistance | Rleak | Between OSC1 and VDD, and between VSS and OSC1 | 200 | | | MΩ |

S1C60L02

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, Crystal: Q13MC146, CG=25 pF, CD=built-in, Ta=25°C

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---------------|---|------|-----|------|------|
| Oscillation start voltage | Vsta (Vss) | tsta≤5sec | -1.2 | | | V |
| Oscillation stop voltage | Vstp (Vss) | tstp≤10sec | -1.2 | | | V |
| Built-in capacity (drain) | CD | Including the parasitic capacity inside the IC | | 20 | | pF |
| Frequency voltage deviation | f/V | Vss=-1.2 to -2.0V (-0.9)*1 | | | 5 | ppm |
| Frequency IC deviation | f/IC | | -10 | | 10 | ppm |
| Frequency adjustment range | f/CG | CG=5-25pF | 40 | | | ppm |
| Higher harmonic oscillation start voltage | Vhho (Vss) | CG=5pF | | | -2.0 | V |
| Allowable leak resistance | Rleak | Between OSC1 and VDD, and between VSS and OSC1 | 200 | | | MΩ |

*1 Items enclosed in parentheses () are those used when operating at heavy load protection mode.

S1C60N02 (CR)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, R_{CR}=420 kΩ, T_a=25°C

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|--------|--------------------------------|------|-------|-----|------|
| Oscillation frequency dispersion | fosc | | -20 | 65kHz | 20 | % |
| Oscillation start voltage | Vsta | | -1.8 | | | V |
| Oscillation start time | tsta | V _{SS} =-1.8 to -3.5V | | 3 | | ms |
| Oscillation stop voltage | Vstp | | -1.8 | | | V |

S1C60L02 (CR)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-1.5 V, R_{CR}=420 kΩ, T_a=25°C

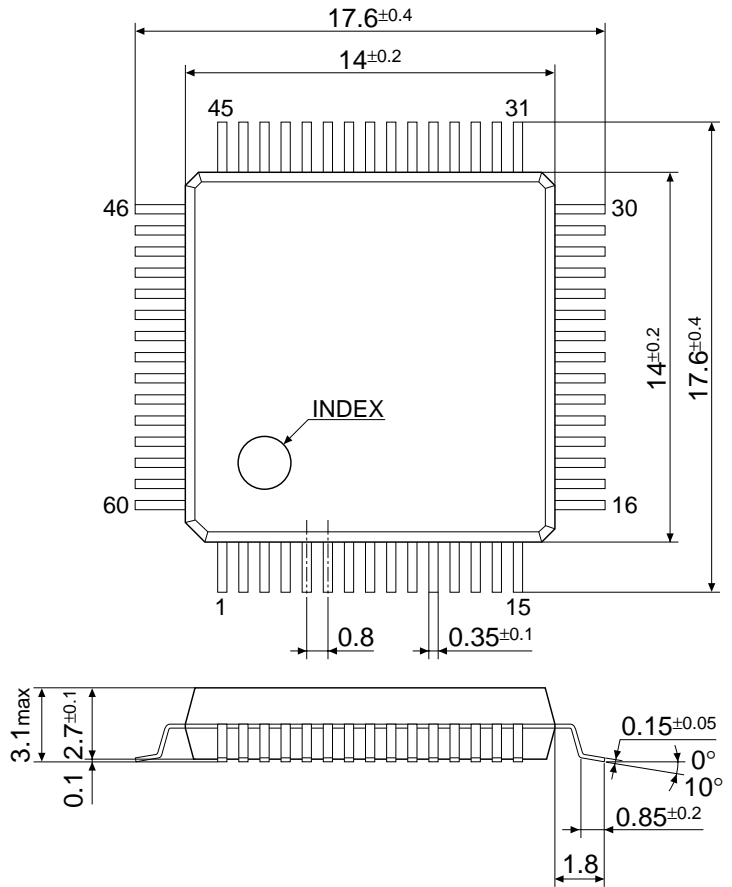
| Item | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|--------|--------------------------------|------|-------|-----|------|
| Oscillation frequency dispersion | fosc | | -20 | 65kHz | 20 | % |
| Oscillation start voltage | Vsta | | -1.2 | | | V |
| Oscillation start time | tsta | V _{SS} =-1.2 to -2.0V | | 3 | | ms |
| Oscillation stop voltage | Vstp | | -1.2 | | | V |

CHAPTER 7 PACKAGE

7.1 Plastic Package

QFP6-60pin

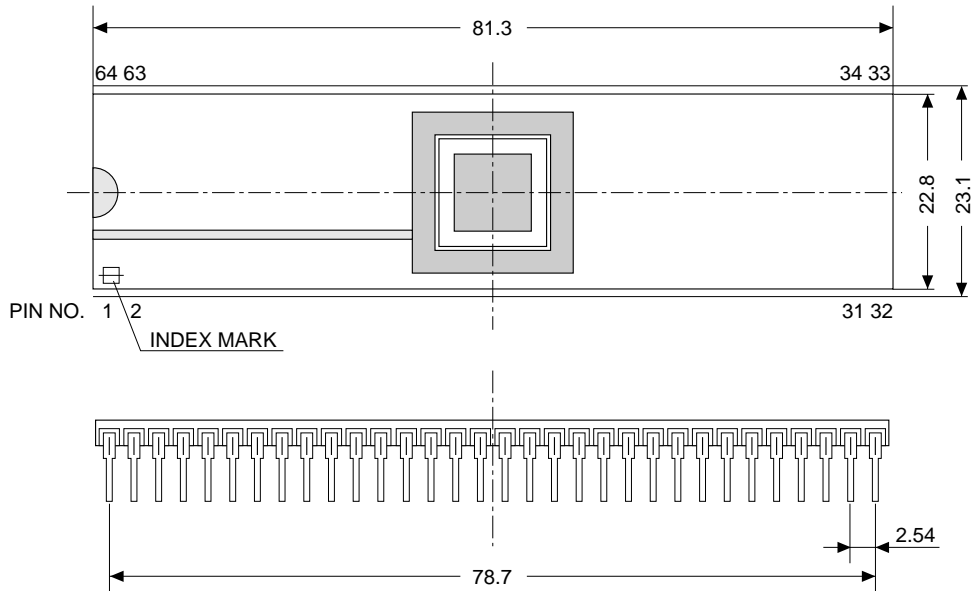
(Unit: mm)



7.2 Ceramic Package for Test Samples

DIP-64pin

(Unit: mm)

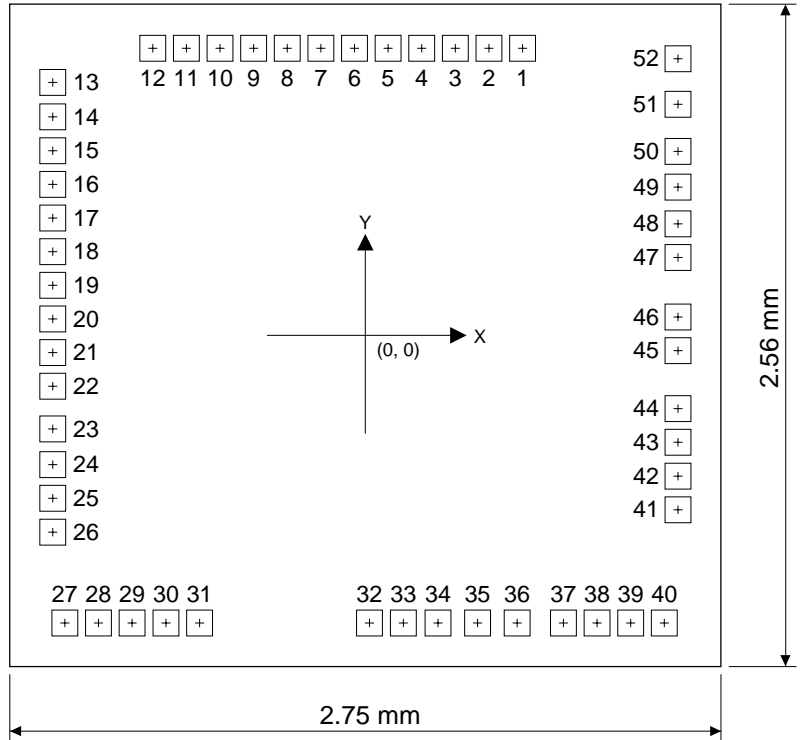


| No. | Pin name | No. | Pin name | No. | Pin name | No. | Pin name |
|-----|----------|-----|----------|-----|----------|-----|----------|
| 1 | N.C. | 17 | OSC1 | 33 | R02 | 49 | SEG6 |
| 2 | SEG17 | 18 | OSC2 | 34 | R03 | 50 | SEG7 |
| 3 | SEG18 | 19 | Vs1 | 35 | RS | 51 | SEG8 |
| 4 | SEG19 | 20 | P00 | 36 | TH | 52 | SEG9 |
| 5 | COM0 | 21 | P01 | 37 | CS | 53 | SEG10 |
| 6 | COM1 | 22 | P02 | 38 | ADOUT | 54 | SEG11 |
| 7 | COM2 | 23 | P03 | 39 | N.C. | 55 | N.C. |
| 8 | COM3 | 24 | N.C. | 40 | N.C. | 56 | N.C. |
| 9 | N.C. | 25 | N.C. | 41 | N.C. | 57 | TEST |
| 10 | VL3 | 26 | N.C. | 42 | N.C. | 58 | RESET |
| 11 | VL2 | 27 | K00 | 43 | SEG0 | 59 | SEG12 |
| 12 | VL1 | 28 | K01 | 44 | SEG1 | 60 | SEG13 |
| 13 | CA | 29 | K02 | 45 | SEG2 | 61 | SEG14 |
| 14 | CB | 30 | K03 | 46 | SEG3 | 62 | SEG15 |
| 15 | VSS | 31 | R00 | 47 | SEG4 | 63 | SEG16 |
| 16 | VDD | 32 | R01 | 48 | SEG5 | 64 | N.C. |

N.C. = No Connection

CHAPTER 8 PAD LAYOUT

8.1 Diagram of Pad Layout



8.2 Pad Coordinates

| Pad No | Pad name | X | Y | Pad No | Pad name | X | Y |
|--------|----------|--------|-------|--------|----------|--------|--------|
| 1 | SEG0 | 608 | 1,111 | 27 | VL3 | -1,162 | -1,111 |
| 2 | SEG1 | 478 | 1,111 | 28 | VL2 | -1,032 | -1,111 |
| 3 | SEG2 | 348 | 1,111 | 29 | VL1 | -902 | -1,111 |
| 4 | SEG3 | 218 | 1,111 | 30 | CA | -771 | -1,111 |
| 5 | SEG4 | 88 | 1,111 | 31 | CB | -641 | -1,111 |
| 6 | SEG5 | -42 | 1,111 | 32 | Vss | 16 | -1,111 |
| 7 | SEG6 | -172 | 1,111 | 33 | VDD | 147 | -1,111 |
| 8 | SEG7 | -302 | 1,111 | 34 | OSC1 | 281 | -1,111 |
| 9 | SEG8 | -432 | 1,111 | 35 | OSC2 | 434 | -1,111 |
| 10 | SEG9 | -562 | 1,111 | 36 | Vs1 | 587 | -1,111 |
| 11 | SEG10 | -692 | 1,111 | 37 | P00 | 766 | -1,111 |
| 12 | SEG11 | -822 | 1,111 | 38 | P01 | 896 | -1,111 |
| 13 | TEST | -1,209 | 978 | 39 | P02 | 1,026 | -1,111 |
| 14 | RESET | -1,209 | 845 | 40 | P03 | 1,156 | -1,111 |
| 15 | SEG12 | -1,209 | 714 | 41 | K00 | 1,209 | -674 |
| 16 | SEG13 | -1,209 | 584 | 42 | K01 | 1,209 | -544 |
| 17 | SEG14 | -1,209 | 454 | 43 | K02 | 1,209 | -413 |
| 18 | SEG15 | -1,209 | 324 | 44 | K03 | 1,209 | -283 |
| 19 | SEG16 | -1,209 | 194 | 45 | R00 | 1,209 | -59 |
| 20 | SEG17 | -1,209 | 64 | 46 | R01 | 1,209 | 71 |
| 21 | SEG18 | -1,209 | -66 | 47 | R02 | 1,209 | 301 |
| 22 | SEG19 | -1,209 | -196 | 48 | R03 | 1,209 | 431 |
| 23 | COM0 | -1,209 | -361 | 49 | RS | 1,209 | 573 |
| 24 | COM1 | -1,209 | -499 | 50 | TH | 1,209 | 711 |
| 25 | COM2 | -1,209 | -629 | 51 | CS | 1,209 | 893 |
| 26 | COM3 | -1,209 | -760 | 52 | ADOUT | 1,209 | 1,069 |

(Unit: μm)

Appendices TECHNICAL INFORMATION

This chapter presents the information necessary for designing a thermometer using a Seiko Epson S1C60N02 and a Thermistor manufactured by Ishizuka Denshi Inc.

Appendix A Design Steps for Designing Thermometer

This section describes the design steps for the thermometer using the S1C60N02 and the Thermistor.

Thermometer design steps

The following shows the design steps:

- (1) Obtain the external capacitor value and the oscillation frequency.
- (2) Obtain the initial value that is set to the up-counter of the A/D converter.
- (3) After A/D conversion, calculate the displayed temperature from the counter value that has been set in the up-counter.

Details of these steps are described in later sections.

Before designing the thermometer, the measured temperature range, standard temperature, and thermistor to be used have to be determined.

Measured temperature range Determine for your application.

Standard temperature The standard temperature is the most precise value. Determine the standard temperature as the temperature that you want to be the most precise.

Thermistor Select the thermistor considering the measured temperature range and the standard temperature. It also should match the IC.

Note that this document assumes the following:

Measured temperature range: -30°C – 70°C

Standard temperature: 20°C

Thermistor: Thermistor 103AT (Compatibility with S1C60N02)

The following A/D converter circuit diagram is shown for your reference.

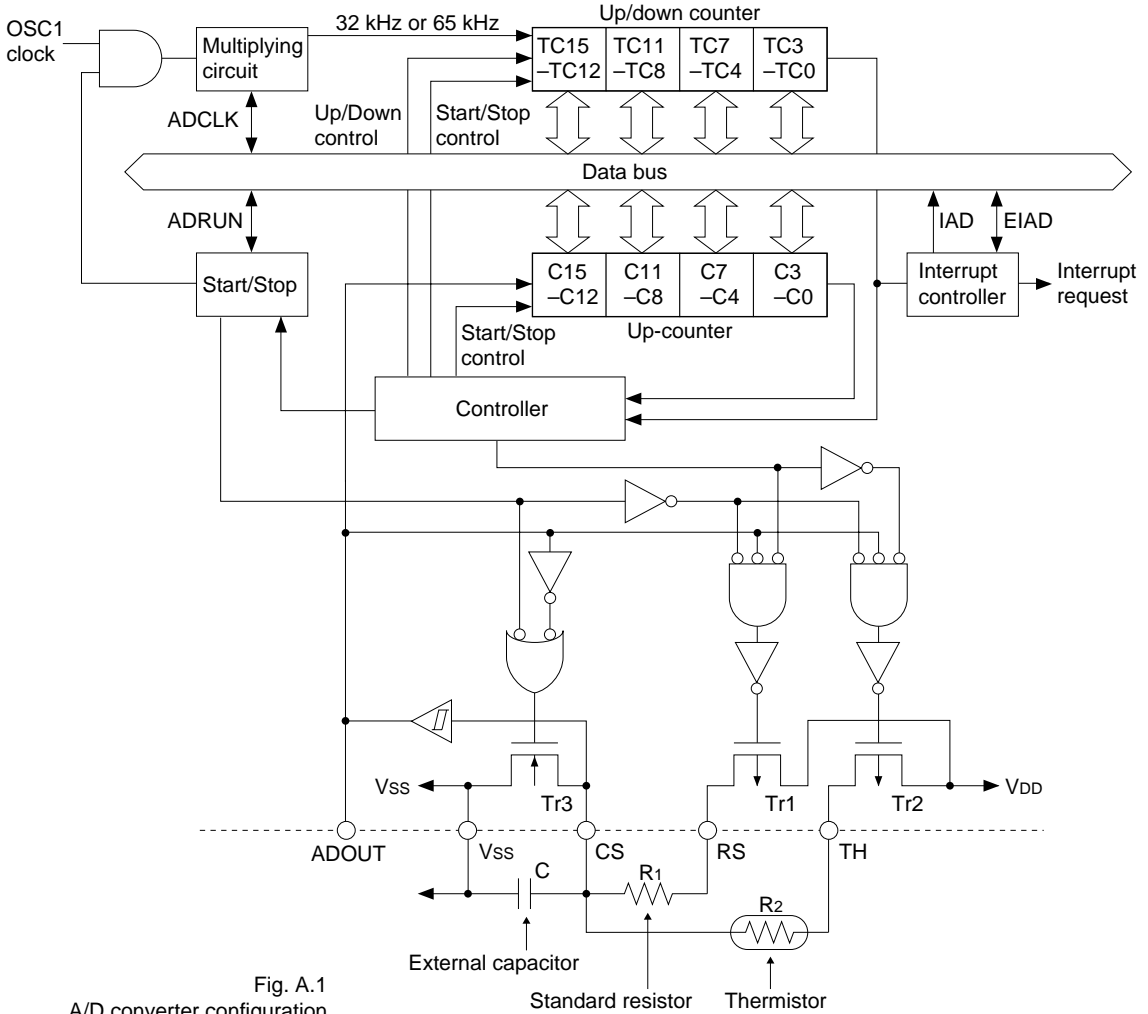


Fig. A.1
A/D converter configuration

How to obtain capacitor value and oscillation frequency

The standard resistor and the thermistor are oscillated according to S1C60N02 A/D converter principles. It is necessary to determine the value of the external capacitor for the oscillation. This section describes how to determine the standard resistor value, the external capacitor value and the CR oscillation frequency.

Table A.1

| Item | Description | Thermistor 103AT usage example |
|---|--|--|
| Standard resistor value (R1) | Thermistor resistance value at the standard temperature. | At 25°C, the 103AT resistance is 10 kΩ. Thus the standard resistance is 10 kΩ. |
| Computation of capacitor for oscillation | <p>The relationship between the frequency, capacitor, and the resistor is as follows:</p> $f = \frac{K}{CR}$ <p>f: Oscillation frequency K: CR oscillation frequency coefficient C: Capacitor R: Resistance</p> <p>From the equation above, C can be obtained based on f and K conditions of S1C60N02. If the C value is smaller within the conditions, the precision is higher.</p> | <p>The f and K conditions of S1C60N02 are as follows:</p> <p>f(max) = 85 kHz (limit of IC operation) 1 ≤ K ≤ 3 (Oscillation coefficient in S1C60N02)</p> <p>With these conditions, the following equation can be derived:</p> $85 \text{ kHz} \geq \frac{K}{CR_{2(TMAX)}}$ <p>R_{2(TMAX)}: Minimum resistance of Thermistor</p> <p>K=3 is the worst condition, then</p> $C \geq \frac{3}{85 \times 10^3 \times 2.23 \times 10^3} = 15,800 \text{ (pF)}$ <p>As a result, the following is determined: C = 22,000 (pF) (Value for general purpose product)</p> |
| Computation of frequency from the standard resistance | <p>If the C value is determined by the above equation, the frequency (f_{CR1}) by the standard resistance can be obtained by the following equation:</p> $f_{CR1} \text{ (kHz)} = \frac{K}{CR_1}$ | <p>The following is obtained:</p> $f_{CR1} = \frac{(1 \text{ to } 3)}{22,000 \times 10^{-12} \times 10 \times 10^3} = 4.5 \text{ to } 13.5 \text{ (kHz)}$ |

By the above equations, the capacitor value (22,000 pF) and the oscillation frequency (4.5–13.5 kHz) by the standard resistance are determined.

For the details of 103AT, see Appendix C.

Setting up counter initial value

The capacitor value and the oscillation frequency by the standard resistance are determined in the previous section. This section describes how to set the initial value of the A/D converter's up counter. For A/D converter principals, see the technical manual for the S1C60N02.

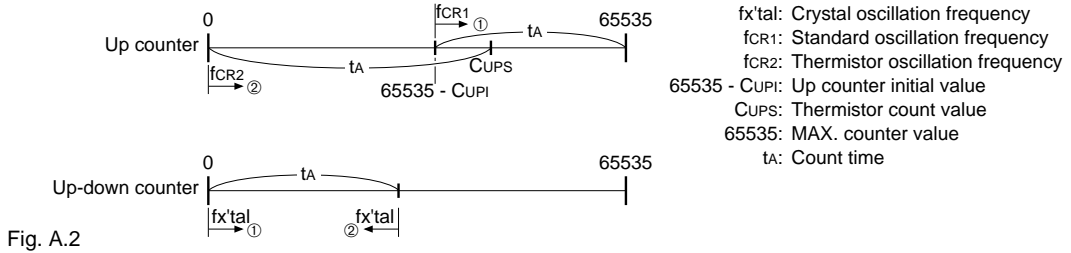


Figure A.2 shows the relationship between the up counter and the up-down counter.

The following conditions should be satisfied:

- Condition (A): The up-down counter should not overflow during an up-count
- Condition (B): The up counter should not overflow during a down-count

With these conditions, the up counter initial value can be obtained with the following equations:

Table A.2

| Item | Description | Thermistor 103AT usage example |
|--|--|--|
| Obtain the up counter initial value from the condition (A) | From the condition (A) the following equation is derived: $65535 > t_A \cdot f_{x'tal} = \frac{65535 - CUP_i}{f_{CR1}} \times f_{x'tal}$ $CUP_i > (1 - \frac{f_{CR1}}{f_{x'tal}}) \times 65535$ Initial value $\leq 65535 - CUP_i \dots(a)$ | From $f_{x'tal} = 65 \text{ kHz}$, $f_{CR1} = 4.5\text{--}13.5 \text{ kHz}$ $CUP_i = (1 - \frac{4.5 \times 10^3}{65 \times 10^3}) \times 65535 \approx 59571$ $CUP_i = (1 - \frac{13.5 \times 10^3}{65 \times 10^3}) \times 65535 \approx 50707$ Initial value $\leq 65535 - 59571 = 5964 \dots(a)'$ |
| Obtain the up counter initial value from the condition (B) | From the condition (B) the following equation is derived: $65535 > CUPS = t_A \times f_{CR2}$ $= \frac{f_{CR2}}{f_{CR1}} \times (65535 - CUP_i)$ $CUP_i = (1 - \frac{f_{CR1}}{f_{CR2}}) \times 65535$ Initial value $\leq 65535 - CUP_i \dots(b)$ From the above equations (a) and (b) the initial value can be determined. | $f_{CR1} = 4.5\text{--}13.5 \text{ kHz}$, $f_{CR2} = 85 \text{ kHz}$ (IC operational maximum) $CUP_i = (1 - \frac{4.5 \times 10^3}{85 \times 10^3}) \times 65535 \approx 60608$ $CUP_i = (1 - \frac{13.5 \times 10^3}{85 \times 10^3}) \times 65535 \approx 53837$ Initial value $\leq 65535 - 60608 = 4927 \dots(b)'$ From (a)' and (b)', the initial value should be set less than 4927. Here, it is set to 3000. (Under the conditions, if the initial value is smaller, the precision is higher.) |

The initial value (3,000) for the up counter is derived from the above equations.

Computation method of displayed temperature by linear approximation

The following shows the linear approximation equation to derive the displayed temperature.

Displayed temperature (°C) = (Count after A/D conversion - Count for minimum in the temperature range) × linear approximation coefficient + minimum value of the temperature range

This equation derives the displayed temperature. The following shows the method. First, each value is described.

[Count value after A/D conversion]

This is the up counter value after an A/D conversion.

[Count for the minimum value of the temperature range]

[Minimum value of the temperature range]

To derive the displayed temperature by the linear approximation, the temperature range must be determined for the linear approximation. In this example, the measured temperature range is -30 to 70°C.

If the temperature range for the linear approximation is set for every 10°C, the temperature range is -30 to -20°C, -20 to -10°C, and so on. The smallest value of each temperature range segment is the minimum value of the temperature range. The largest value is the maximum value of the temperature range.

The count value for the minimum value for the temperature range is expressed by the following equation:

$$\begin{aligned} \text{A/D converter count value} &= \frac{f_{CR2}}{f_{CR1}} \times \text{up counter initial value} \\ &= \frac{(K/CR2)}{(K/CR1)} \times \text{up counter initial value} \\ &= \frac{R1}{R2} \times \text{up counter initial value} \end{aligned}$$

By substituting R₂ (Thermistor resistance), R₁ (standard resistance), and the up counter initial value with actual values, the count value for the minimum of the temperature range is obtained.

[Linear approximation coefficient]

The linear approximation coefficient is the value that shows how many degrees (centigrade) for one count in the temperature range. The linear approximation coefficient is expressed by the following equation:

$$\text{Linear approximation coefficient} = \frac{\text{Temperature range}}{\text{Count for max. of temperature range} - \text{Count for min. of temperature range}}$$

(As you can see, the temperature range is smaller, the precision is higher.)

The following table shows the various values for every 10°C.

Table A.3

| Temperature (°C) | 103AT Thermistor R ₂ resistance (kΩ) | Linear approximation coefficient in the specified temperature range | Count value |
|------------------|---|---|-------------|
| -30 | 111.3 | 0.0575 | 269 |
| -20 | 67.74 | 0.0380 | 443 |
| -10 | 42.45 | 0.0254 | 706 |
| 0 | 27.28 | 0.0175 | 1099 |
| 10 | 17.96 | 0.0123 | 1670 |
| 20 | 12.09 | 0.00887 | 2481 |
| 30 | 8.313 | 0.00650 | 3608 |
| 40 | 5.828 | 0.00485 | 5147 |
| 50 | 4.161 | 0.00368 | 7209 |
| 60 | 3.021 | 0.00283 | 9930 |
| 70 | 2.229 | | 13459 |

The following example derives a displayed temperature using the values in the above table.

Example: Assume the count value after an A/D conversion is 3200. Then, it is between 3608 and 2481 in the table. As a result the temperature range is 20° to 30°C.

- The count value for the minimum value of the temperature range: 2481
- The count value for the maximum value of the temperature range: 3608

Then, the linear approximation coefficient of the temperature range is 0.00887.

As a result, the displayed temperature is derived as follows:

$$\text{Displayed temperature} = (3200 - 2481) \times 0.00887 + 20 \text{ (°C)} = 26.377 \text{ (°C)}$$

Appendix B Error Factors

When a temperature is computed using the S1C60N02 A/D converter and the Thermistor, the following error factors should be taken in account:

Thermistor resistance dispersion

The Thermistor manufacturer should guarantee the precision.

A/D converter error factors

Error (circuit) by A/D conversion in R1 (standard resistance) and R2 (Thermistor)

By the CR oscillation at the standard resistor (R1), the up counter and the up-down counter increment the counter with the timing shown below.

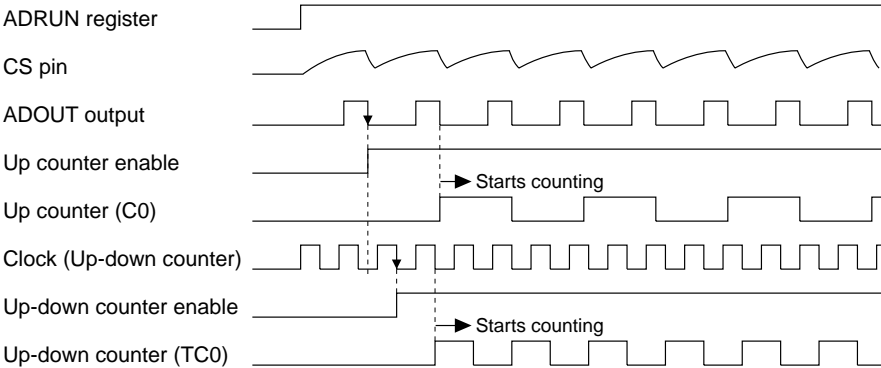


Fig. B.1

After the A/D RUN, the first trailing edge of the CS pin triggers the up counter enable. From the next trailing edge, the up counter starts to count. In addition, the first trailing edge of the clock after the up counter is enabled, the up-down counter is enabled and it starts to count from the next trailing edge.

When the up counter value becomes 0, the up counter is disabled. The next trailing edge of the clock disables the up-down counter. If this situation occurs, the error described below will result.

| | | |
|----------|--------------------------------|-------------------------|
| Started: | Min. ≈ 0 | } Total up-down counter |
| | Max. Up-down counter - 1 count | |
| Stopped: | Min ≈ 0 | } - 2 counts |
| | Max. Up-down counter - 1 count | |

The same is true in the CR oscillation by Thermistor R2, and a similar error occurs. Exception: because the up-down counter is down-counted the following counting error occurs:

| | | |
|----------|--------------------------------|-------------------------|
| Started: | Min. ≈ 0 | } Total up-down counter |
| | Max. Up-down counter - 1 count | |
| Stopped: | Min ≈ 0 | } - 2 counts |
| | Max. Up-down counter - 1 count | |

Therefore, as for the error from the circuit, a maximum of 2 count errors results.

The effect of the maximum 2 count error is given below.

$$\Delta_1\text{MAX} (\%) = \frac{2}{(f_{\text{CLK}}/f_{\text{CR1}}) \times \text{CUP11}} \times 100 \text{ --- (1)}$$

$$\Delta_2\text{MAX} (\%) = \frac{2}{(f_{\text{CLK}}/f_{\text{CR2}}) \times \text{CUPS}} \times 100 \text{ --- (2)}$$

- fCLK: Clock frequency (32 kHz/64 kHz)
- fCR1: CR oscillation frequency by standard resistor
- CUP11: Up counter initial value (times)
- Δ1MAX: Maximum error (%) at CR oscillation by standard resistor
- fCR2: CR oscillation frequency by Thermistor
- CUPS: Thermistor count (times)
- Δ2MAX: Maximum error (%) at CR oscillation by Thermistor

In addition, the number of counts of the up-down counter should be the same. Then the following equation is true:

$$\frac{f_{\text{CLK}}}{f_{\text{CR1}}} \times \text{CUP11} = \frac{f_{\text{CLK}}}{f_{\text{CR2}}} \times \text{CUPS} \text{ --- (3)}$$

Then, from (3), assume the up-down counter counts shifted 2 counts, the following equations are true:

$$\frac{f_{\text{CLK}}}{f_{\text{CR1}}} \times \text{CUP11} = \frac{f_{\text{CLK}}}{f_{\text{CR2}}} \times \text{CUPS} \pm 2$$

$$\frac{f_{\text{CR2}}}{f_{\text{CR1}}} = \frac{\text{CUPS} \pm 2 \times (f_{\text{CR2}}/f_{\text{CLK}})}{\text{CUP11}} \text{ --- (3)'}$$

- (1) is the count error at the CR oscillation by the standard resistor.
 - (2) is the count error at the CR oscillation by Thermistor.
- The total error is expressed by the equation (3)' with the ratio of fCR1 and fCR2.

The segment that represents the error in the equation (3)' is $\pm 2 \times (f_{\text{CR2}}/f_{\text{CLK}})$. If the values CUP11 and CUPS are large, this error factor may be ignored.

For how to determine the initial value (CUP11) of the up counter, see the section describing thermometer design steps.

CR oscillation constant (K) error

The constant, K, is determined by the logic level of the internal Schmidt trigger of the IC. However, in S1C60N02, the Schmidt trigger shares the circuit with the standard resistor and Thermistor. As a result, oscillation is canceled and no error occurs.

Error by transistor ON resistance

The transistor ON resistance is directly connected to the standard resistor and Thermistor; this may cause an error.

See the circuit shown next to Figure B.2 below. In this circuit, the capacitor is charged by Tr1, T2 ON and Tr3 OFF. If the voltage at the CS pin changes to a certain level, the capacitor charge is drained by Tr1, Tr2 OFF and Tr3 ON. As a result, the CR oscillation is generated as in Figure B.3.

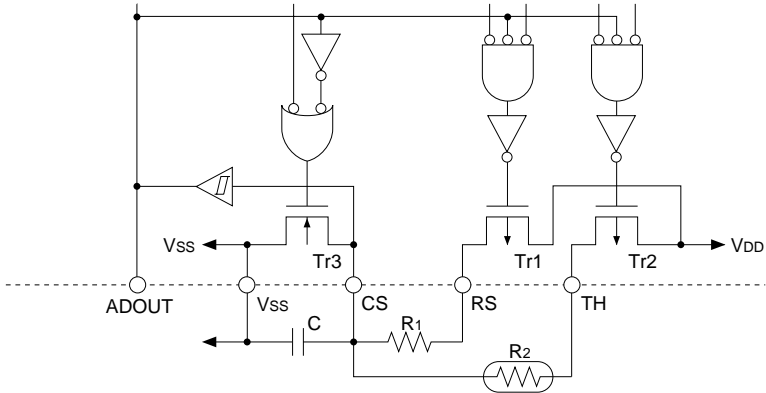


Fig. B.2

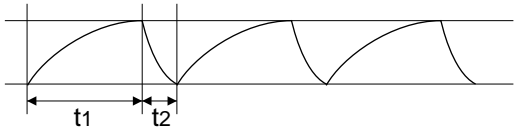


Fig. B.3

At this time, if the ON resistance of Tr1 and Tr2 ON is t1 and the ON resistance of Tr3 is t2, the constance may be effected.

The S1C60N02 transistors are standardized to have a maximum of 100 Ω.

This standard includes dispersion by temperature characteristics, Pch and Nch.

The Evaluation board transistor uses standard ICs and the actual resistance is about 1 kΩ. (This is not guaranteed and should be regarded as just a reference.)

The error by ON resistance of this transistor is expressed by the following equations:

$$\Delta_3 (\%) = \frac{\text{Up counter count} - \text{Actual upcounter count}}{\text{Up counter count}} \times 100$$

$$= \frac{K}{\text{CUP11} - \frac{C(R_1 + R_{Tr})}{f_{CR1}}} \times \text{CUP11} \times 100 = \left\{ 1 - \frac{R_1}{(R_1 + R_{Tr})} \right\} \times 100$$

$$\Delta_4 (\%) = \frac{\text{Up counter count} - \text{Actual upcounter count}}{\text{Up counter count}} \times 100$$

$$= \frac{K}{\text{CUPS} - \frac{C(R_2 + R_{Tr})}{f_{CR2}}} \times \text{CUP11} \times 100 = \left\{ 1 - \frac{R_2}{(R_2 + R_{Tr})} \right\} \times 100$$

- Δ3: Error (%) by transistor ON resistance (CR oscillation by standard resistance)
- Δ4: Error (%) by transistor ON resistance (CR oscillation by Thermistor)
- CUP11: Up counter initial value (times)
- CUPS: Thermistor count value (times)
- RTr: Transistor ON resistance (Ω)
- fCR1: Oscillation frequency (Hz) (CR oscillation by standard resistance)
- fCR2: Oscillation frequency (Hz) (CR oscillation by Thermistor)

Example: Transistor ON resistance error when Thermistor 103AT measures 60°C

$$\Delta_3 = \left\{ 1 - \frac{10 \times 10^3}{(10 \times 10^3 + 100)} \right\} \times 100 \approx 1\%$$

$$\Delta_4 = \left\{ 1 - \frac{3.217 \times 10^3}{(3.217 \times 10^3 + 100)} \right\} \times 100 \approx 3\%$$

As a result, the following errors occur by directly connecting the transistor ON resistance:

- 1% at CR oscillation on the standard resistor
- 3% at CR oscillation on Thermistor

The transistor ON resistance effect is smaller if R1 and R2 are larger. (See Equation Δ3 and Δ4.)

In the high temperature range, the R2 value becomes small and Δ4 becomes large. This causes precision degradation. Compensation is needed to implement a user's required precision.

Figure B.4 shows the A/D converter ON resistance errors (Δ4 - Δ3) of the Evaluation board and the actual IC when the thermistor 103AT is used.

ON resistance errors when thermistor 103AT is used

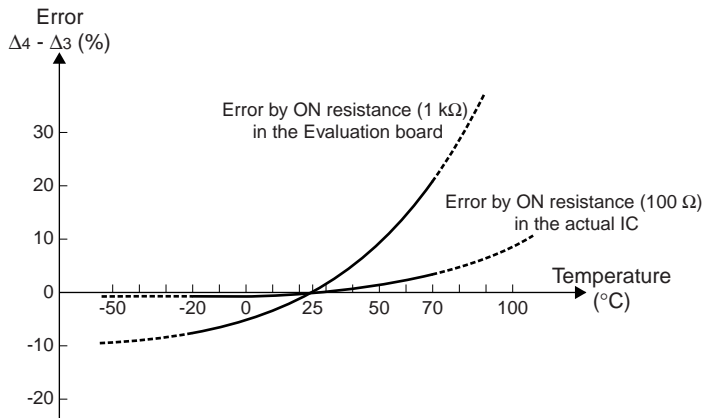


Fig. B.4

This figure shows the plot of errors when the ON resistance in the Evaluation board is 1 kΩ and that of the actual IC is 100 Ω. As shown in the figure, the Evaluation board's error is larger than the actual IC, therefore, programs evaluated using the Evaluation board may not operate normally in the actual IC.

To avoid this problem, it is necessary to reduce the ON resistance error.

Choose a thermistor resistance as large as possible to reduce the ON resistance error. At least 10 kΩ (Ta = 25°C) of resistance is required. The plot (Figure B.4) in this case shows a 10 kΩ thermistor resistance that satisfies the minimum resistance condition, note, however, that there is a large error increase in temperature over 60°C.

For example, when using a 10 k Ω ($T_a = 25^\circ\text{C}$) thermistor for the actual IC, the ON resistance in the Evaluation board can be close to that of the actual IC by connecting 10 thermistors in series to configure a 100 k Ω ($T_a = 25^\circ\text{C}$) thermistor and by using a 100 k Ω reference resistance and reducing the capacitance to 1/10.

However, ON resistance is so susceptible to source voltage levels and board mount conditions affect the conversion results, therefore, it is impossible to obtain exactly the same results between the Evaluation board and the actual IC even if the methods described above are used. It is necessary to evaluate the A/D conversion using the results of several samples from the final product.

Error by floating capacity

The floating capacity of the inside of an IC, board, lead of a sensor and others may be an error factor. Floating capacity inside an IC may be several pF and it may be ignored by increasing the capacitor value.

Software error

In the software, it is normal to convert the counter value to an actual temperature by a linear approximation. In this method, an error may be caused by the linear approximation in the temperature measured range.

As shown in Figure B.5 below, if the temperature range measured is 20°C to 30°C, the weight of 1 count differs between 20°C and 29°C.

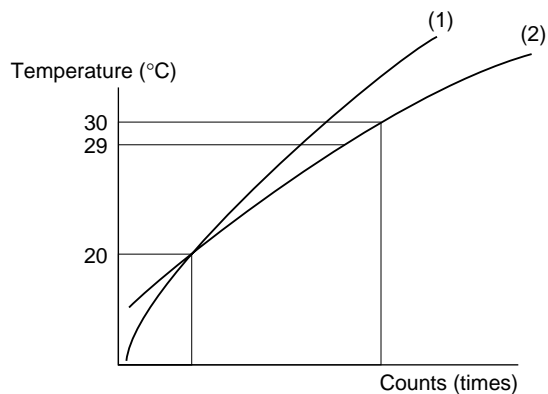


Fig. B.5

On the slope (1), the linear approximation coefficient in this segment for 1 count is large, and the slope (2) has a smaller coefficient.

For example, if this segment (20°C to 30°C) is calculated by the same linear approximation coefficient, and if the 20°C is the reference point, then, at 29°C, the linear approximation coefficient becomes the largest and, at 29°C, the error is maximum.

The error may differ depending on the temperature measured by the software, up counter initial value and Thermistor type.

Appendix C AT Thermistor

High precision thermistor

Features The AT Thermistor has a high precision thermistor with small resistance and B constant error margin. Using the AT Thermistor as a temperature sensor does not require adjustment between a control circuit and the sensor; and the AT Thermistor provides a temperature precision of $\pm 0.3^\circ\text{C}$. As a result, a high precision temperature control and temperature display are possible.

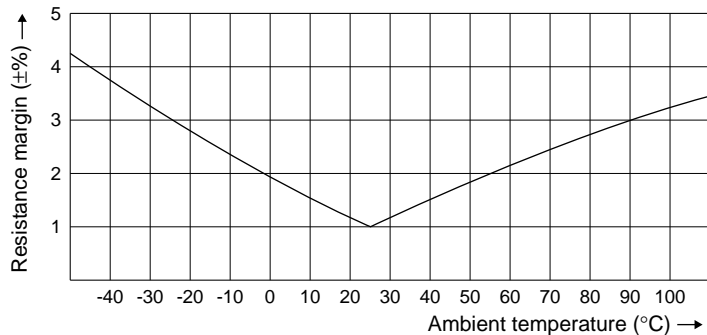
- Error margins of resistance and temperature characteristics are very small.
- Small age-based change and high reliability
- Low price
- High durability

Usage Air conditioners, fan heaters, FF heaters, refrigerators, water heaters, boiler/kitchen appliances, copiers, printers, facsimiles, automatic vending machines, agricultural equipment, automobiles (for external temperature, internal temperature, air flow sensor), portable thermometers, medical equipment, thermos-type containers, solar heating system, automatic toilet seats, fire alarms, home automation

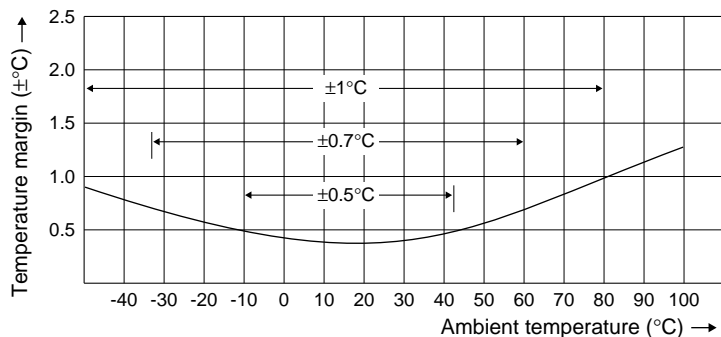
Type number **103 AT - 2**

- └ External type
- └ High precision AT Thermistor
- └ Zero load resistance (25°C) 103: 10 kΩ

Resistance margin graph



Temperature precision graph



Comparison between AT type and others

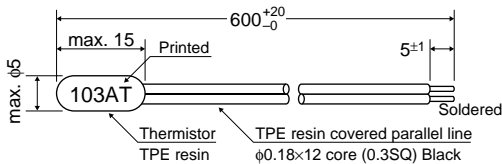
| Thermistor | R25 margin | B margin | Temperature margin (25°C) | Temperature control (display) for every 1°C |
|------------|------------|----------|---------------------------|---|
| AT type | ±1% | ±1% | ±0.3°C | Circuit adjustment - not required |
| Other type | ±5% | ±3% | ±1.3°C | Circuit adjustment - required |

Ratings

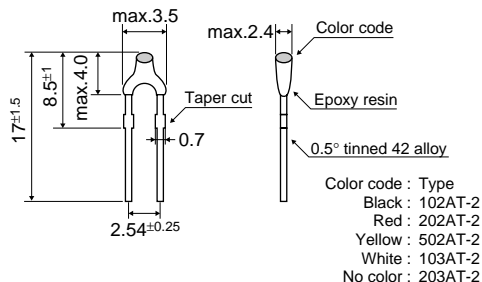
| Type | R25 | B constant | Thermal radiation constant (mW/°C) | Thermal constant (s) | Maximum power (mW) at 25°C | Temperature range (°C) |
|------------|-----------|------------|------------------------------------|----------------------|----------------------------|------------------------|
| 102AT-1 | 1 kΩ ±1% | 3100K ±1% | Approx. 3 | Approx. 75 | 15 | -50 to 90 |
| 202AT-1 | 2 kΩ ±1% | 3182K ±1% | Approx. 3 | Approx. 75 | 15 | -50 to 90 |
| 502AT-1 | 5 kΩ ±1% | 3324K ±1% | Approx. 3 | Approx. 75 | 15 | -50 to 105 |
| 103AT-1 | 10 kΩ ±1% | 3435K ±1% | Approx. 3 | Approx. 75 | 15 | -50 to 105 |
| 102AT-2 | 1 kΩ ±1% | 3100K ±1% | Approx. 2 | Approx. 15 | 10 | -50 to 90 |
| 202AT-2 | 2 kΩ ±1% | 3182K ±1% | Approx. 2 | Approx. 15 | 10 | -50 to 90 |
| 502AT-2 | 5 kΩ ±1% | 3324K ±1% | Approx. 2 | Approx. 15 | 10 | -50 to 110 |
| 103AT-2, 3 | 10 kΩ ±1% | 3435K ±1% | Approx. 2 | Approx. 15 | 10 | -50 to 110 |
| 203AT-2 | 20 kΩ ±1% | 4013K ±1% | Approx. 2 | Approx. 15 | 10 | -50 to 110 |
| 103AT-4 | 10 kΩ ±1% | 3435K ±1% | Approx. 2 | Approx. 10 | 10 | -30 to 90 |

External dimension (AT-3, 4 in omission)

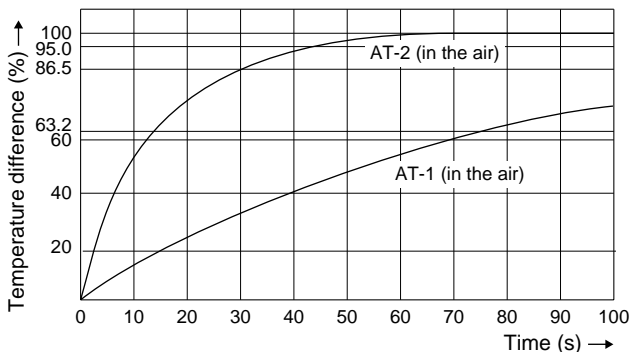
AT-1



AT-2

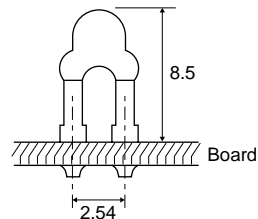


Thermal response



Board soldering method

Proper usage example



Proper soldering conditions:
260°C, 10 seconds or less

Resistance - Temperature characteristics

-50 to 29°C

30 to 110°C

| Temp (°C) | 103AT | | |
|-----------|-----------|----------|-----------|
| | Rmax (kΩ) | Rst (kΩ) | Rmin (kΩ) |
| -50 | 344.4 | 329.2 | 314.7 |
| -49 | 324.7 | 310.7 | 297.2 |
| -48 | 306.4 | 293.3 | 280.7 |
| -47 | 289.2 | 277.0 | 265.3 |
| -46 | 273.2 | 261.8 | 250.8 |
| -45 | 258.1 | 247.5 | 237.3 |
| -44 | 244.0 | 234.1 | 224.6 |
| -43 | 230.8 | 221.6 | 212.7 |
| -42 | 218.5 | 209.8 | 201.5 |
| -41 | 206.8 | 198.7 | 191.0 |
| -40 | 195.9 | 188.4 | 181.1 |
| -39 | 185.4 | 178.3 | 171.5 |
| -38 | 175.5 | 168.9 | 162.6 |
| -37 | 166.2 | 160.1 | 154.2 |
| -36 | 157.5 | 151.8 | 146.2 |
| -35 | 149.3 | 144.0 | 138.8 |
| -34 | 141.6 | 136.6 | 131.8 |
| -33 | 134.4 | 129.7 | 125.2 |
| -32 | 127.6 | 123.2 | 118.9 |
| -31 | 121.2 | 117.1 | 113.1 |
| -30 | 115.1 | 111.3 | 107.5 |
| -29 | 109.3 | 105.7 | 102.2 |
| -28 | 103.8 | 100.4 | 97.16 |
| -27 | 98.63 | 95.47 | 92.41 |
| -26 | 93.75 | 90.80 | 87.93 |
| -25 | 89.15 | 86.39 | 83.70 |
| -24 | 84.82 | 82.22 | 79.71 |
| -23 | 80.72 | 78.29 | 75.93 |
| -22 | 76.85 | 74.58 | 72.36 |
| -21 | 73.20 | 71.07 | 68.99 |
| -20 | 69.74 | 67.74 | 65.80 |
| -19 | 66.42 | 64.54 | 62.72 |
| -18 | 63.27 | 61.52 | 59.81 |
| -17 | 60.30 | 58.66 | 57.05 |
| -16 | 57.49 | 55.95 | 54.44 |
| -15 | 54.83 | 53.39 | 51.97 |
| -14 | 52.31 | 50.96 | 49.63 |
| -13 | 49.93 | 48.66 | 47.42 |
| -12 | 47.67 | 46.48 | 45.31 |
| -11 | 45.53 | 44.41 | 43.32 |
| -10 | 43.50 | 42.45 | 41.43 |
| -9 | 41.54 | 40.56 | 39.59 |
| -8 | 39.68 | 38.76 | 37.85 |
| -7 | 37.91 | 37.05 | 36.20 |
| -6 | 36.24 | 35.43 | 34.63 |
| -5 | 34.65 | 33.89 | 33.14 |
| -4 | 33.14 | 32.43 | 31.73 |
| -3 | 31.71 | 31.04 | 30.39 |
| -2 | 30.35 | 29.72 | 29.11 |
| -1 | 29.06 | 28.47 | 27.89 |
| 0 | 27.83 | 27.28 | 26.74 |
| 1 | 26.64 | 26.13 | 25.62 |
| 2 | 25.51 | 25.03 | 24.55 |
| 3 | 24.44 | 23.99 | 23.54 |
| 4 | 23.42 | 22.99 | 22.57 |
| 5 | 22.45 | 22.05 | 21.66 |
| 6 | 21.52 | 21.15 | 20.78 |
| 7 | 20.64 | 20.29 | 19.95 |
| 8 | 19.80 | 19.48 | 19.15 |
| 9 | 19.00 | 18.70 | 18.40 |
| 10 | 18.24 | 17.96 | 17.67 |
| 11 | 17.51 | 17.24 | 16.97 |
| 12 | 16.80 | 16.55 | 16.31 |
| 13 | 16.13 | 15.90 | 15.67 |
| 14 | 15.50 | 15.28 | 15.06 |
| 15 | 14.89 | 14.68 | 14.48 |
| 16 | 14.31 | 14.12 | 13.93 |
| 17 | 13.75 | 13.57 | 13.40 |
| 18 | 13.22 | 13.06 | 12.89 |
| 19 | 12.72 | 12.56 | 12.41 |
| 20 | 12.23 | 12.09 | 11.95 |
| 21 | 11.77 | 11.63 | 11.50 |
| 22 | 11.32 | 11.20 | 11.07 |
| 23 | 10.90 | 10.78 | 10.66 |
| 24 | 10.49 | 10.38 | 10.27 |
| 25 | 10.10 | 10.00 | 9.900 |
| 26 | 9.732 | 9.632 | 9.533 |
| 27 | 9.381 | 9.281 | 9.181 |
| 28 | 9.044 | 8.944 | 8.845 |
| 29 | 8.721 | 8.622 | 8.523 |

| Temp (°C) | 103AT | | |
|-----------|-----------|----------|-----------|
| | Rmax (kΩ) | Rst (kΩ) | Rmin (kΩ) |
| 30 | 8.412 | 8.313 | 8.215 |
| 31 | 8.113 | 8.015 | 7.917 |
| 32 | 7.826 | 7.729 | 7.632 |
| 33 | 7.551 | 7.455 | 7.359 |
| 34 | 7.288 | 7.192 | 7.097 |
| 35 | 7.036 | 6.941 | 6.846 |
| 36 | 6.793 | 6.699 | 6.606 |
| 37 | 6.561 | 6.468 | 6.375 |
| 38 | 6.338 | 6.246 | 6.154 |
| 39 | 6.124 | 6.033 | 5.942 |
| 40 | 5.918 | 5.828 | 5.739 |
| 41 | 5.719 | 5.630 | 5.541 |
| 42 | 5.527 | 5.439 | 5.352 |
| 43 | 5.343 | 5.256 | 5.170 |
| 44 | 5.166 | 5.080 | 4.996 |
| 45 | 4.996 | 4.912 | 4.828 |
| 46 | 4.833 | 4.749 | 4.667 |
| 47 | 4.676 | 4.594 | 4.512 |
| 48 | 4.525 | 4.444 | 4.364 |
| 49 | 4.380 | 4.300 | 4.221 |
| 50 | 4.240 | 4.161 | 4.084 |
| 51 | 4.104 | 4.026 | 3.950 |
| 52 | 3.973 | 3.897 | 3.822 |
| 53 | 3.847 | 3.772 | 3.698 |
| 54 | 3.726 | 3.652 | 3.579 |
| 55 | 3.609 | 3.537 | 3.465 |
| 56 | 3.497 | 3.426 | 3.355 |
| 57 | 3.389 | 3.319 | 3.249 |
| 58 | 3.285 | 3.216 | 3.148 |
| 59 | 3.184 | 3.116 | 3.049 |
| 60 | 3.088 | 3.021 | 2.955 |
| 61 | 2.994 | 2.928 | 2.863 |
| 62 | 2.903 | 2.838 | 2.775 |
| 63 | 2.816 | 2.752 | 2.690 |
| 64 | 2.732 | 2.669 | 2.608 |
| 65 | 2.650 | 2.589 | 2.529 |
| 66 | 2.572 | 2.512 | 2.452 |
| 67 | 2.496 | 2.437 | 2.379 |
| 68 | 2.423 | 2.365 | 2.308 |
| 69 | 2.353 | 2.296 | 2.240 |
| 70 | 2.285 | 2.229 | 2.174 |
| 71 | 2.219 | 2.163 | 2.109 |
| 72 | 2.155 | 2.101 | 2.047 |
| 73 | 2.093 | 2.040 | 1.987 |
| 74 | 2.034 | 1.981 | 1.930 |
| 75 | 1.976 | 1.924 | 1.874 |
| 76 | 1.920 | 1.870 | 1.820 |
| 77 | 1.866 | 1.817 | 1.768 |
| 78 | 1.814 | 1.766 | 1.718 |
| 79 | 1.764 | 1.716 | 1.669 |
| 80 | 1.716 | 1.669 | 1.622 |
| 81 | 1.668 | 1.622 | 1.577 |
| 82 | 1.623 | 1.577 | 1.533 |
| 83 | 1.578 | 1.534 | 1.490 |
| 84 | 1.536 | 1.492 | 1.449 |
| 85 | 1.494 | 1.451 | 1.409 |
| 86 | 1.454 | 1.412 | 1.371 |
| 87 | 1.415 | 1.374 | 1.333 |
| 88 | 1.378 | 1.337 | 1.297 |
| 89 | 1.341 | 1.301 | 1.262 |
| 90 | 1.306 | 1.266 | 1.228 |
| 91 | 1.271 | 1.233 | 1.195 |
| 92 | 1.238 | 1.200 | 1.163 |
| 93 | 1.206 | 1.169 | 1.132 |
| 94 | 1.175 | 1.138 | 1.102 |
| 95 | 1.144 | 1.108 | 1.073 |
| 96 | 1.115 | 1.080 | 1.045 |
| 97 | 1.087 | 1.052 | 1.018 |
| 98 | 1.059 | 1.025 | 0.9918 |
| 99 | 1.032 | 0.9988 | 0.9663 |
| 100 | 1.006 | 0.9735 | 0.9416 |
| 101 | 0.9812 | 0.9489 | 0.9175 |
| 102 | 0.9567 | 0.9250 | 0.8942 |
| 103 | 0.9330 | 0.9018 | 0.8716 |
| 104 | 0.9100 | 0.8793 | 0.8496 |
| 105 | 0.8877 | 0.8575 | 0.8284 |
| 106 | 0.8660 | 0.8364 | 0.8077 |
| 107 | 0.8456 | 0.8159 | 0.7877 |
| 108 | 0.8245 | 0.7960 | 0.7683 |
| 109 | 0.8047 | 0.7767 | 0.7495 |

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