32 kHz watch circuit with EEPROM

PCA16XX series

FEATURES

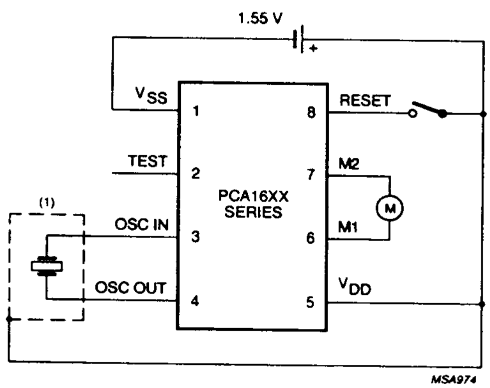
- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Time keeping adjustment electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption; typically 170 nA
- Detector for silver-oxide or lithium battery voltage levels
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

GENERAL DESCRIPTION

The PCA16XX series are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with bipolar stepping motors.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA16XXT	8	micro-flat-pack	plastic	SOT144A
PCA16XXU	–	chip in tray	–	–



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

Fig.1 Typical application circuit diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	positive supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

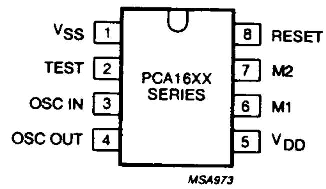


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

Motor pulse

The motor pulse width (t_W) and the cycle times (t_T) are given in Table 2.

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{LIT} and V_{EOL} every minute. The first voltage level detection is carried out 30 ms after a RESET.

Lithium mode

If a lithium voltage is detected ($V_{DD} \geq V_{LIT}$), the circuit will operate in the lithium mode. The motor pulse will be produced with a 75% duty factor.

Silver-oxide mode

If the voltage level detected is between V_{LIT} and V_{EOL}, the circuit will operate in silver-oxide mode.

Battery end-of-life

(1)

If the battery end-of-life is detected ($V_{DD} \leq V_{EOL}$), the motor pulse will be produced without chopping. To indicate this condition, bursts of 4 pulses are produced every 4 s.

Power-on reset

For correct operation of the power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms. All resetable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of time keeping adjustment, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a HIGH impedance 3-state condition and a 32 Hz signal without jitter is produced at the TEST pin. A debounce circuit protects accidental stoppages due to mechanical shock to the watch (t_{DEB} = 14.7 to 123.2 ms).

Connecting RESET to V_{SS} activates Tests 1 and 2 and disables the time keeping adjustment.

Test 1 ($V_{DD} > V_{EOL}$): normal function takes place except the voltage detection cycle (t_V) is 125 ms and the cycle time is 31.25 ms. At pin TEST a minute signal is available at 8192 times its normal frequency.

Test 2(2) ($V_{DD} < V_{EOL}$): the voltage detection cycle (t_V) is 31.25 ms and the motor pulse period (t_{T2}) = 31.25 ms.

Test and reset mode are terminated by disconnecting the RESET pin.

(1) Only available for types with a 1 s motor pulse.
(2) Only applicable for types with the battery end-of-life detector.

Test 3: when V_{DD} voltage level is greater than 5 V, motor pulses with a time period of t_{T3} = 31.25 ms and n x 122 µs are produced to check the contents of the EEPROM. At pin TEST the motor pulse period signal (t_T) is available at 1024 times its normal frequency. The circuit returns to normal operation when V_{DD} < 2.5 V between two motor pulses.

Time keeping adjustment

(1)

To compensate for the tolerance in the quartz crystal frequency, a number (n) of 8192 Hz pulses are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, which is achieved by the following steps (see Fig.4):

1. The quartz frequency deviation (Δf/f) and n are found (see Table 1).
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3}.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to write the EEPROM and reset the circuit.
8. V_{DD} is decreased to the operating voltage level to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage between two motor pulses to return to operating mode.

Table 1 Quartz crystal frequency deviation and n.

$\frac{\Delta f}{f} \times 10^{-6}$ (ppm)	n	t_{T3} step 2 or 9 (ms)
0	0	31.250 (note 1)
+2.03	1	31.372
+4.06	2	31.494
.	.	.
.	.	.
.	.	.
+127.89	63	38.936

Note

1. 122 µs per step.

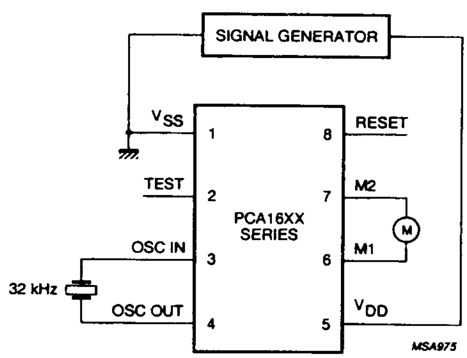
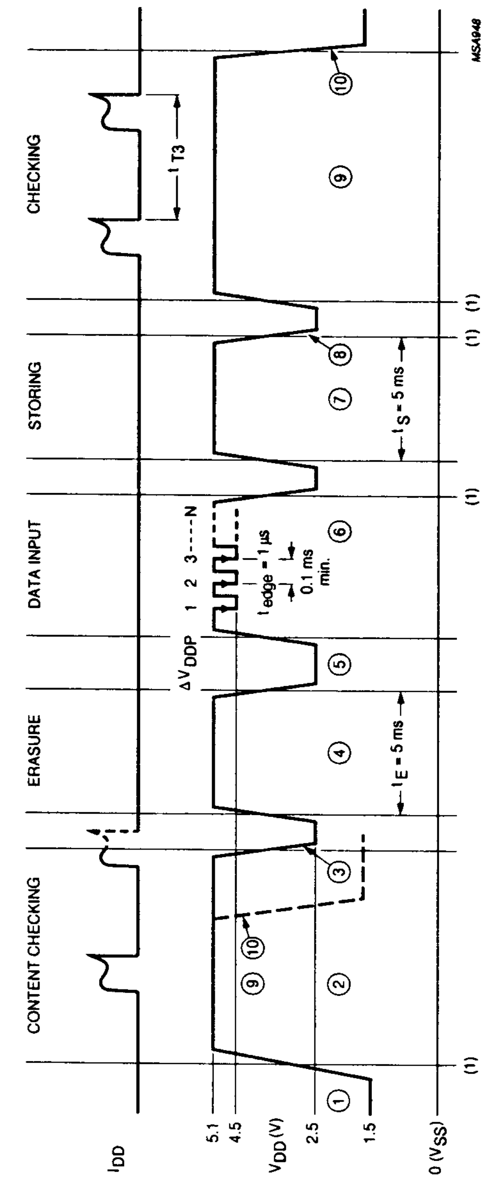


Fig.3 Programming circuit diagram.

(1) Programming can be performed 100 times.



(1) Rise and fall time should be greater than 1 ms for immediately correct checking.

Fig.4 V_{DD} for programming.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages	note 2	V_{SS}	V_{DD}	V
	output short-circuit duration			indefinite	
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C
V_{es}	electrostatic handling	note 3	−800	+800	V

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').
3. Equivalent to three discharges of a 100 pF capacitor at 800 V, through a resistor of 1.5 kΩ (with positive and negative polarity).

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.
Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.5	2.5	V
ΔV_{DD}	supply voltage	transient; V_{DD} = 1.2 to 2.5 V	−	−	0.25	V
V_{DDP}	supply voltage	programming	5.0	5.1	5.2	V
ΔV_{DDP}	supply voltage pulse	programming	0.55	0.6	0.65	V
I_{DD1}	supply current	between motor pulses	−	170	260	nA
I_{DD2}	supply current	between motor pulses; V_{DD} = 2.1 V	−	190	300	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	−	180	280	nA
I_{DD4}	supply current	stop mode; pin 8 connected to V_{DD}; V_{DD} = 2.1 V	−	220	360	nA
I_{DD5}	supply current	V_{DD} = 2.1 V; T_{amb} = −10 to +60 °C	−	−	600	nA
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_L = 2 kΩ; T_{amb} = −10 to +60 °C	−	150	200	mV
R_{sc}	short-circuit resistance Σ (P + N)	$I_{transistor}$ < 1 mA	−	200	300	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_T	cycle time		note 1			
t_P	pulse width		note 2			
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	–	–	V
g_m	transconductance	$V_{i(p-p)} \leq 50$ mV	6	15	–	µA/V
t_{osc}	start-up time		–	1	–	s
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		8	10	12	pF
C_o	output capacitance		12	15	18	pF
Voltage level detector						
V_{LIT}	threshold voltage	lithium mode	1.65	1.80	1.95	V
V_{EOL}	threshold voltage	battery end-of-life	1.27	1.38	1.46	V
ΔV_{VLD}	hysteresis of threshold		–	10	–	mV
$\frac{\Delta V_{VLD}}{°C}$	temperature coefficient		–	−1	–	mV/K
t_V	voltage detection cycle		–	60	–	s
Reset input						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	–	–	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	–	1	–	µs
I_{im}	peak input current	note 3	–	320	–	nA
$I_{i(av)}$	average input current		–	10	–	nA
Test mode						
	cycle time:					
t_{T1}	test 1		–	31.25	–	ms
t_{T2}	test 2		–	31.25	–	ms
t_{T3}	test 3		see Table 1			
t_{DEB}	debounce time	RESET = V_{DD}	14.7	–	123.2	ms
Battery end-of-life						
t_{EOL}	end-of-life sequence		–	4	–	s
t_{E1}	motor pulse width	see Table 2	–	t_P	–	ms
t_{E2}	time between pulses		–	31.25	–	ms

Notes

1. Cycle time can be changed to one of the following values: 1, 5, 10, 12 or 20 s (see Table 2).
2. Pulse width can be varied from 2 ms to 15.7 ms in steps of 1 ms (see Table 2).
3. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

Table 2 Available types and timing information (see Fig.5).

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS				
			PULSE WIDTH t_p (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS
1602	T	1	7.8	75	yes	no	
1603	U/7	20	7.8	100	yes	no	
1604	U; T	5	7.8	75	yes	no	
1605	U/7	5	4.8	75	yes	no	
1606	U/10	10	6.8	100	yes	no	
1607	U	5	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1608	U	5	7.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1611	U	1	6.8	75	yes	no	
1624	U	12	3.9	75 56	yes	no	1.5 V and 2.1 V Lithium
1625	U/7	5	5.8	75	yes	no	
1626	U	20	5.8	100	yes	no	
1627	U/7	20	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1628	U	20	5.8	75	yes	no	
1629	U/7	5	6.8	75	yes	no	

Where:

U = Chip in trays.

U/7 = Chip with bumps on tape.

U/10 = Chip on foil.

T = SOT144.

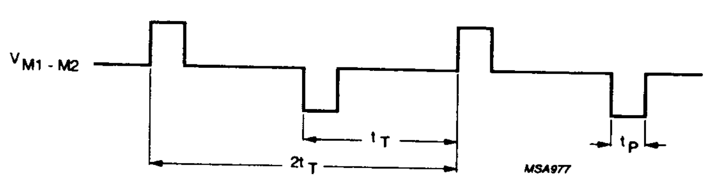
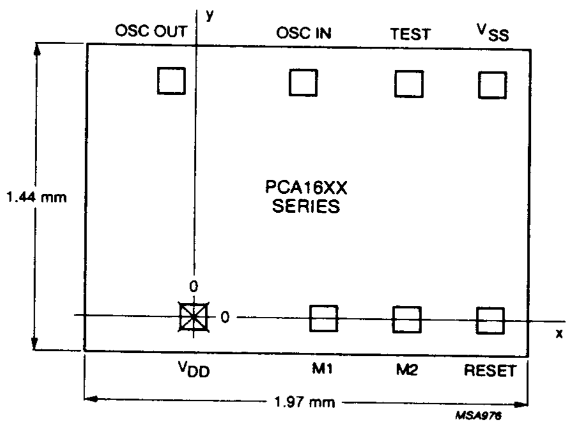


Fig.5 Motor output waveform (normal operation).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 2.84 mm².

Bonding pad dimensions: 110 μm x 110 μm.

Chip thickness: 200 ±25 μm, with bumps: 270 ±25 μm.

Fig.6 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to the center of pad (V_{DD}), see Fig.6.

PAD	X	Y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
RESET	1290	0
chip corner (max. value)	−495	−170