TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

4,194,304-WORDS × 4 BANKS × 16-BITS SYNCHRONOUS DYNAMIC RAM
8,388,608-WORDS × 4 BANKS × 8-BITS SYNCHRONOUS DYNAMIC RAM
16,777,216-WORDS × 4 BANKS × 4-BITS SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

TC59SM816CMB/CMBL is a CMOS synchronous dynamic random access memory organized as 4,194,304-words × 4 banks × 16 bits and TC59SM808CMB/CMBL is organized as 8,388,608 words × 4 banks × 8 bits and The TC59SM804CMB/CMBL is organized as 16,777,216 words × 4 banks × 4 bits. Fully synchronous operations are referenced to the positive edges of clock input and can transfer data up to 143M words per second. These devices are controlled by commands setting. Each bank are kept active so that DRAM core sense amplifiers can be used as a cache. The refresh functions, either Auto Refresh or Self Refresh are easy to use. By having a programmable Mode Register, the system can choose the most suitable modes which will maximize its performance. These devices are ideal for main memory in applications such as work-stations.

FEATURES

PARAMETER		TC59SM816/M808/M804		
		-70	-75	-80
t_{CK}	Clock Cycle Time (min)	7 ns	7.5 ns	8 ns
t_{RAS}	Active to Precharge Command Period (min)	40 ns	45 ns	48 ns
t_{AC}	Access Time from CLK (max)	5.4 ns	5.4 ns	6 ns
t_{RC}	Ref/Active to Ref/Active Command Period (min)	56 ns	65 ns	68 ns
I_{CC1}	Operation Current (max) (Single bank)	80 mA	75 mA	70 mA
I_{CC4}	Burst Operation Current (max)	100 mA	95 mA	90 mA
I_{CC6}	Self-Refresh Current (max)	3 mA	3 mA	3 mA

- Single power supply of 3.3 V ± 0.3 V
- Up to 143 MHz clock frequency
- Synchronous operations: All signals referenced to the positive edges of clock
- Architecture: Pipeline
- Organization
  TC59SM816CMB/CMBL: 4,194,304 words × 4 banks × 16 bits
  TC59SM808CMB/CMBL: 8,388,608 words × 4 banks × 8 bits
  TC59SM804CMB/CMBL: 16,777,216 words × 4 banks × 4 bits
- Programmable Mode register
- Auto Refresh and Self Refresh
- Burst Length: 1, 2, 4, 8, Full page
- CAS Latency: 2, 3
- Single Write Mode
- Burst Stop Function
- Byte Data Controlled by LDQM, UDQM (TC59SM816)
- 8K Refresh cycles/64 ms
- Interface: LVTTL
- Package
  TC59SM816CMB/CMBL: P-TFBGA60-0816-0.80AZ
  TC59SM808CMB/CMBL: P-TFBGA60-0816-0.80AZ
  TC59SM804CMB/CMBL: P-TFBGA60-0816-0.80AZ

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PIN NAMES

A0~A12	Address Input
BS0, BS1	Bank Select
DQ0~DQ3 (TC59SM804)	Data Input/Output
DQ0~DQ7 (TC59SM808)	
DQ0~DQ15 (TC59SM816)	
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM (TC59SM808/M804)	Output Disable/Write Mask
UDQM/LDQM (TC59SM816)	
CLK	Clock input
CKE	Clock enable
V_{CC}	Power (+3.3 V)
V_{SS}	Ground
V_{CCQ}	Power (+3.3 V) (for DQ buffer)
V_{SSQ}	Ground (for DQ buffer)
NC	No Connection

BALL ASSIGNMENT (TOP VIEW)

TC59SM816CMB/CMBL

TC59SM808CMB/CMBL

TC59SM804CMB/CMBL

1	2	1	2	1	2		5	6	5	6	5	6
V	DQ15	V	DQ7	V	NC	A	NC	V	DQ0	V	DQ0	V
DQ14	V Q	NC	V Q	NC	V Q	B	V Q	NC	V Q	NC	V Q	DQ1
DQ13	V Q	DQ6	V Q	DQ3	V Q	C	V Q	DQ0	V Q	DQ1	V Q	DQ2
DQ12	DQ11	NC	DQ5	NC	NC	D	NC	NC	DQ2	NC	DQ4	DQ3
DQ10	V Q	NC	V Q	NC	V Q	E	V Q	NC	V Q	NC	V Q	DQ5
DQ9	V Q	DQ4	V Q	DQ2	V Q	F	V Q	DQ1	V Q	DQ3	V Q	DQ6
DQ8	NC	NC	NC	NC	NC	G	NC	NC	NC	NC	NC	DQ7
NC	V	NC	V	NC	V	H	V	NC	V	NC	V	NC
NC	UDQM	NC	DQM	NC	DQM	J	NC	$\overline{WE}$	NC	$\overline{WE}$	LDQM	$\overline{WE}$
NC	CLK	NC	CLK	NC	CLK	K	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$
CKE	A12	CKE	A12	CKE	A12	L	NC	$\overline{CS}$	NC	$\overline{CS}$	NC	$\overline{CS}$
A11	A9	A11	A9	A11	A9	M	BA1	BA0	BA1	BA0	BA1	BA0
A8	A7	A8	A7	A8	A7	N	A0	A10/AP	A0	A10/AP	A0	A10/AP
A6	A5	A6	A5	A6	A5	P	A2	A1	A2	A1	A2	A1
V	A4	V	A4	V	A4	Q	A3	V	A3	V	A3	V

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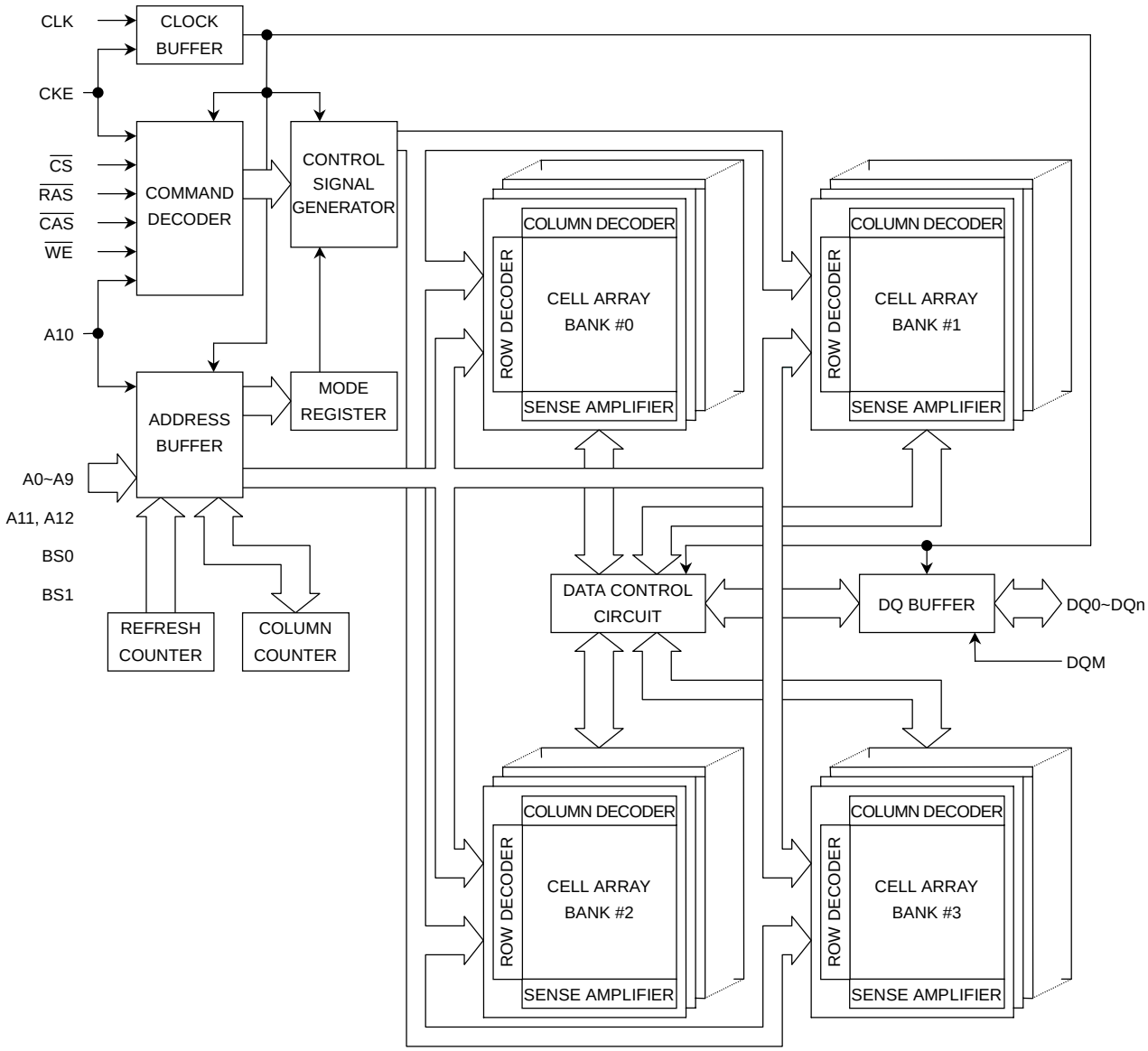
BLOCK DIAGRAM



NOTE: The TC59SM804CMB/CMBL configuration is 8192 × 2048 × 4 of cell array with the DQ pins numbered DQ0~DQ3.
The TC59SM808CMB/CMBL configuration is 8192 × 1024 × 8 of cell array with the DQ pins numbered DQ0~DQ7.
The TC59SM816CMB/CMBL configuration is 8192 × 512 × 16 of cell array with the DQ pins numbered DQ0~DQ15.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS	NOTES
V_{IN}, V_{OUT}	Input, Output Voltage	–0.3~V_{CC} + 0.3	V	1
V_{CC}, V_{CCQ}	Power Supply Voltage	–0.3~4.6	V	1
T_{opr}	Operating Temperature	0~70	°C	1
T_{stg}	Storage Temperature	–55~150	°C	1
T_{solder}	Soldering Temperature (10s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short-Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0°~70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	3	3.3	3.6	V	2
V_{CCQ}	Power Supply Voltage (for DQ Buffer)	3	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2	—	V_{CC} + 0.3	V	2
V_{IL}	LVTTL Input Low Voltage	–0.3	—	0.8	V	2

Note: V_{IH} (max) = V_{CC}/V_{CCQ} + 1.2 V for pulse width ≤ 5 ns
V_{IL} (min) = V_{SS}/V_{SSQ} – 1.2 V for pulse width ≤ 5 ns
V_{CCQ} must be less than or equal to V_{CC}.

CAPACITANCE (V_{CC} = 3.3 V, f = 1 MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_I	Input Capacitance (A0~A12, BS0, BS1, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM*, CKE)	—	4	pF
	Input Capacitance (CLK)	—	5	pF
C_O	Input/Output Capacitance	—	6.5	pF

Note: These parameters are periodically sampled and not 100% tested.
* LDQM, UDQM (TC59SM816)

DC CHARACTERISTICS (V_{CC} = 3.3 V ± 0.3 V, Ta = 0°~70°C)

PARAMETER		SYMBOL	-70		-75		-80		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
OPERATING CURRENT t_{CK} = min, t_{RC} = min Active Precharge command cycling without burst operation	1 bank operation	I_{CC1}	—	80	—	75	—	70	mA	3
STANDBY CURRENT t_{CK} = min, $\overline{CS}$ = V_{IH}, $V_{IH/L}$ = V_{IH}(min) / V_{IL}(max), Bank: Inactive state	CKE = V_{IH}	I_{CC2}	—	40	—	35	—	30		3
	CKE = V_{IL} (Power Down mode)	I_{CC2P}	—	1	—	1	—	1		3
STANDBY CURRENT CLK = V_{IL}, $\overline{CS}$ = V_{IH}, $V_{IH/L}$ = V_{IH}(min) / V_{IL}(max), Bank: Inactive state	CKE = V_{IH}	I_{CC2S}	—	10	—	10	—	10		
	CKE = V_{IL} (Power Down mode)	I_{CC2PS}	—	1	—	1	—	1		
NO OPERATING CURRENT t_{CK} = min, $\overline{CS}$ = V_{IH}(min), Bank: Active state (4 banks)	CKE = V_{IH}	I_{CC3}	—	60	—	55	—	50		
	CKE = V_{IL} (Power Down mode)	I_{CC3P}	—	10	—	10	—	10		
BURST OPERATING CURRENT t_{CK} = min Read/Write command cycling		I_{CC4}	—	100	—	95	—	90		3, 4
AUTO REFRESH CURRENT t_{CK} = min, t_{RC} = min Auto Refresh command cycling		I_{CC5}	—	170	—	160	—	150		3
SELF REFRESH CURRENT Self Refresh mode CKE = 0.2 V	Standard Products (CMB)	I_{CC6}	—	3	—	3	—	3		
	Low Power Version (CMBL)		—	1.6	—	1.6	—	1.6		

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (0 V ≤ V_{IN} ≤ V_{CC}, all other pins not under test = 0 V)	I_I(L)	–5	5	μA	
OUTPUT LEAKAGE CURRENT (Output disable, 0 V ≤ V_{OUT} ≤ V_{CCQ})	I_O(L)	–5	5	μA	
LVTTL OUTPUT H LEVEL VOLTAGE (I_{OUT} = –2 mA)	V_{OH}	2.4	—	V	
LVTTL OUTPUT L LEVEL VOLTAGE (I_{OUT} = 2 mA)	V_{OL}	—	0.4	V	

AC CHARACTERISTICS AND OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0°~70°C) (Notes: 5, 6, 7)

SYMBOL	PARAMETER		-70		-75		-80		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Ref/Active to Ref/Active Command Period		56	—	65	—	68	—	ns	8
t_{RAS}	Active to Precharge Command Period		40	100000	45	100000	48	100000		
t_{RCD}	Active to Read/Write Command Delay Time		15	—	20	—	20	—		
t_{CCD}	Read/Write(a) to Read/Write(b) Command Period		1	—	1	—	1	—	Cycle	
t_{RP}	Precharge to Active Command Period		15	—	20	—	20	—	ns	
t_{RRD}	Active(a) to Active(b) Command Period		15	—	15	—	20	—		
t_{WR}	Write-Recovery Time	CL* = 2	7.5	—	10	—	10	—		
		CL* = 3	7	—	7.5	—	8	—		
t_{CK}	CLK Cycle Time	CL* = 2	7.5	1000	10	1000	10	1000		
		CL* = 3	7	1000	7.5	1000	8	1000		
t_{CH}	CLK High-Level Width		2.5	—	2.5	—	3	—		
t_{CL}	CLK Low-Level Width		2.5	—	2.5	—	3	—		
t_{AC}	Access Time from CLK	CL* = 2	—	5.4	—	6	—	6		
		CL* = 3	—	5.4	—	5.4	—	6		
t_{OH}	Output Data Hold Time		3	—	3	—	3	—		
t_{HZ}	Output Data High-Impedance Time		3	7	3	7.5	3	8		7
t_{LZ}	Output Data Low-Impedance Time		0	—	0	—	0	—		
t_{SB}	Power-Down Mode Entry Time		0	7	0	7.5	0	8		
t_t	Transition Time of CLK (rise and fall)		0.5	10	0.5	10	0.5	10		
t_{DS}	Data-In Set-up Time		1.5	—	1.5	—	2	—		
t_{DH}	Data-In Hold Time		0.8	—	0.8	—	1	—		
t_{AS}	Address Set-up Time		1.5	—	1.5	—	2	—		
t_{AH}	Address Hold Time		0.8	—	0.8	—	1	—		
t_{CKS}	CKE Set-up Time		1.5	—	1.5	—	2	—		
t_{CKH}	CKE Hold Time		0.8	—	0.8	—	1	—		
t_{CMS}	Command Set-up Time		1.5	—	1.5	—	2	—		
t_{CMH}	Command Hold Time		0.8	—	0.8	—	1	—		
t_{REF}	Refresh Time		—	64	—	64	—	64	ms	
t_{RSC}	Mode Register Set Cycle Time		14	—	15	—	16	—	ns	8

* CL means $\overline{CAS}$ latency.

NOTES:

(1) Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.

(2) All voltages are referenced to V_{SS}.

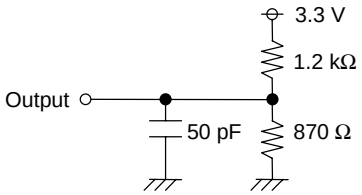
(3) These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.

(4) These parameters depend on the output loading. Specified values are obtained with the output open.

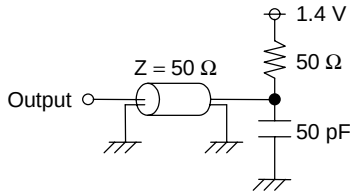
(5) Power-up sequence is described in Note 9.

(6) AC TEST CONDITIONS

Output Reference Level	1.4 V, 1.4 V
Output Load	See diagram B below
Input Signal Levels	2.4 V, 0.4 V
Transition Time (rise and fall) of Input Signals	2 ns
Input Reference Level	1.4 V



AC test load (A)



AC test load (B)

(7) t_{HZ} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

(8) These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows:
the number of clock cycles = specified value of timing / clock period
(count fractions as a whole number)

(9) Power-up Sequence
Power-up must be performed in the following sequence.

1) Power must be applied to V_{CC} and V_{CCQ} (simultaneously) while all input signals are held in the "NOP" state. The CLK signals must be started at the same time.

2) After power-up a pause of at least 200 μs is required. It is required that DQM and CKE signals must be held "High" (V_{CC} levels) to ensure that the DQ output is in High-impedance state.

3) All banks must be precharged.

4) The Mode Register Set command must be asserted to initialize the Mode Register.

5) A minimum of eight Auto Refresh dummy cycles is required to stabilize the internal circuitry of the device.

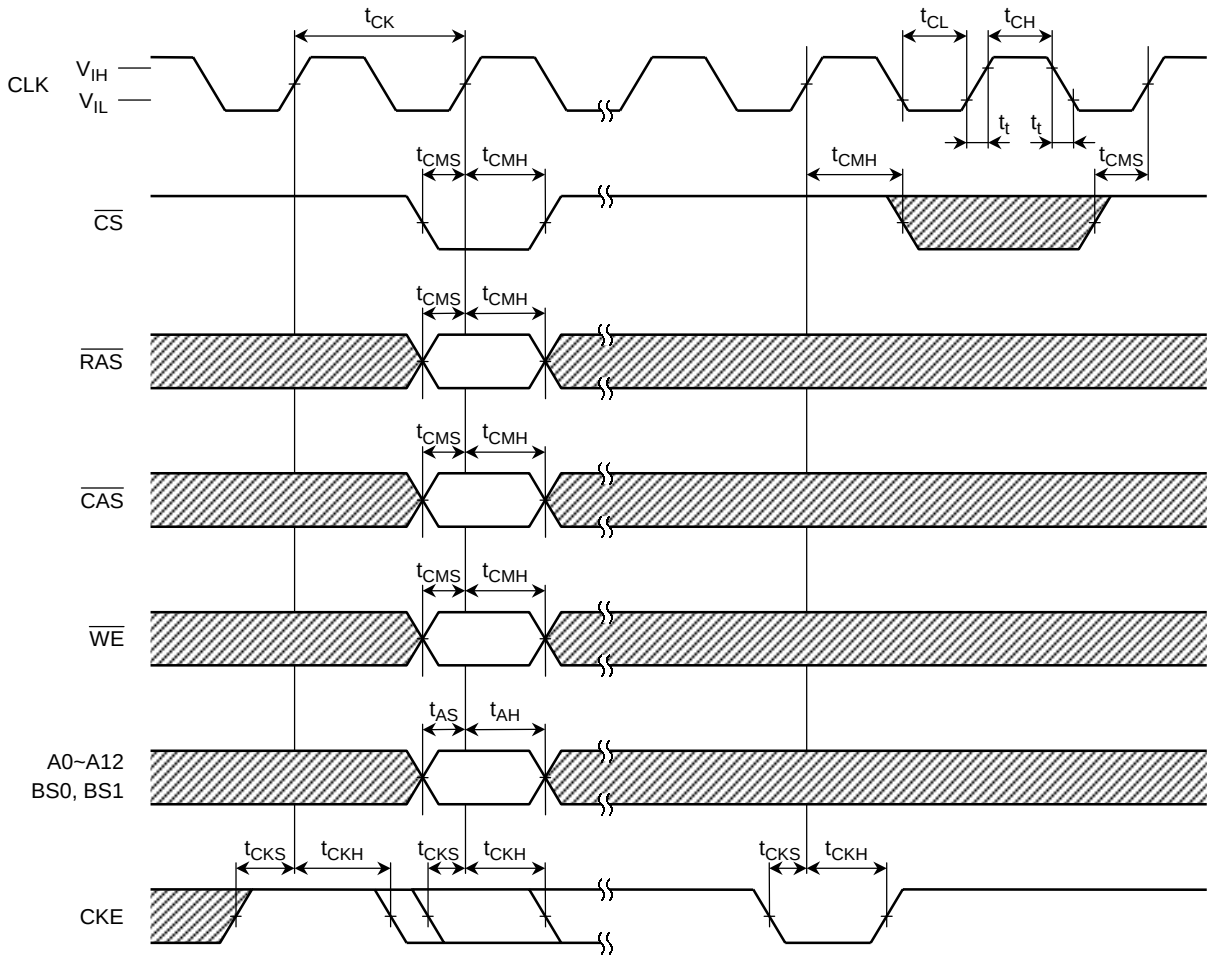
The Mode Register Set command can be invoked either before or after the Auto Refresh dummy cycles.

(10) AC Latency Characteristics

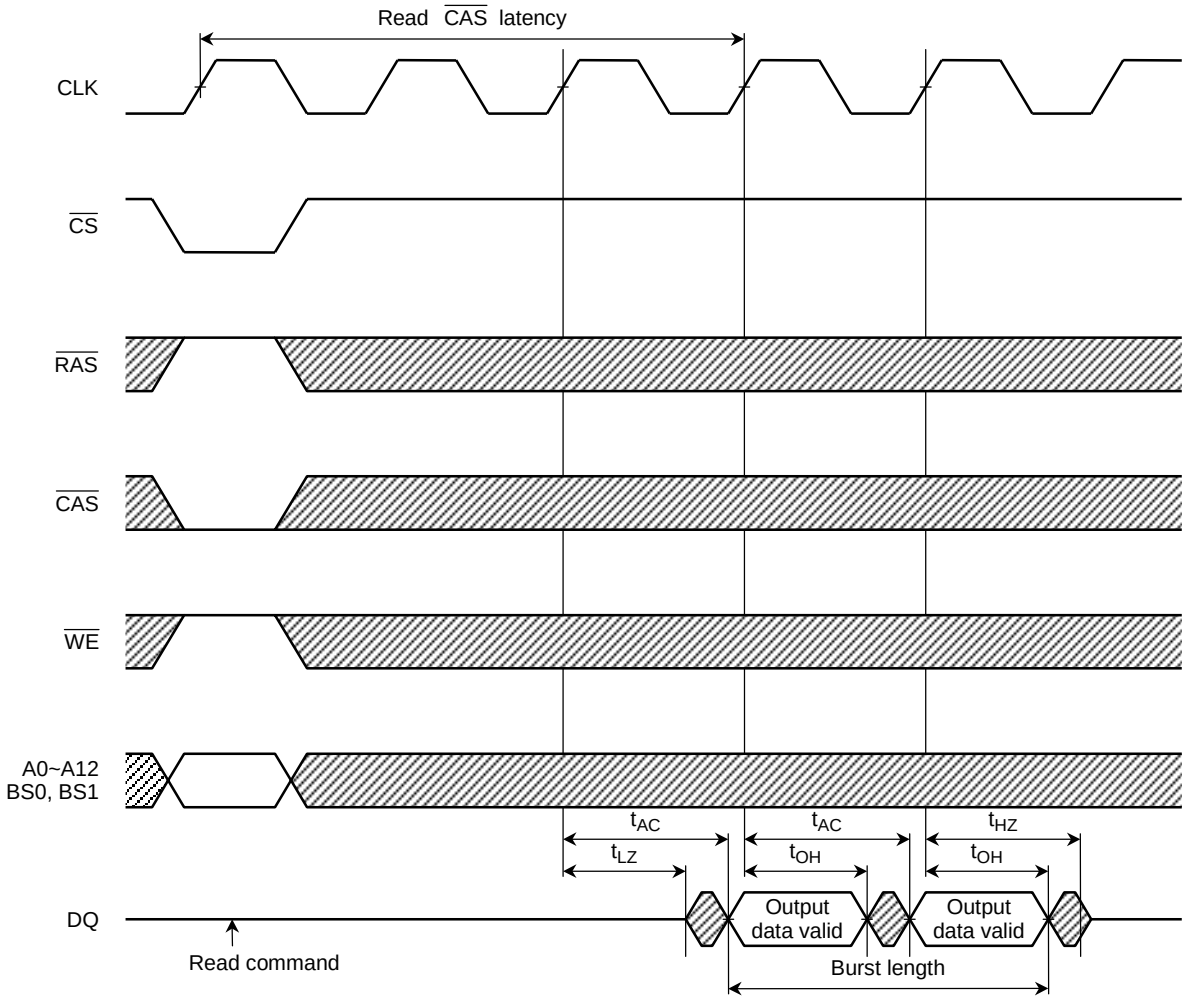
CKE to clock disable (CKE Latency)		1	Cycle
DQM to output in High-Z (Read DQM Latency)		2	
DQM to input data delay (Write DQM Latency)		0	
Write command to input data (Write Data Latency)		0	
$\overline{CS}$ to Command input ($\overline{CS}$ Latency)		0	
Precharge to DQ Hi-Z Lead time	CL = 2	2	
	CL = 3	3	
Precharge to Last Valid data out	CL = 2	1	
	CL = 3	2	
Burst Stop Command to DQ Hi-Z Lead time	CL = 2	2	
	CL = 3	3	
Burst Stop Command to Last Valid data out	CL = 2	1	
	CL = 3	2	
Read with Autoprecharge Command to Active/Ref Command	CL = 2	BL + t_{RP}	Cycle + ns
	CL = 3	BL + t_{RP}	
Write with Autoprecharge Command to Active/Ref Command	CL = 2	BL + t_{RP}	
	CL = 3	BL + t_{RP}	

TIMING DIAGRAMS

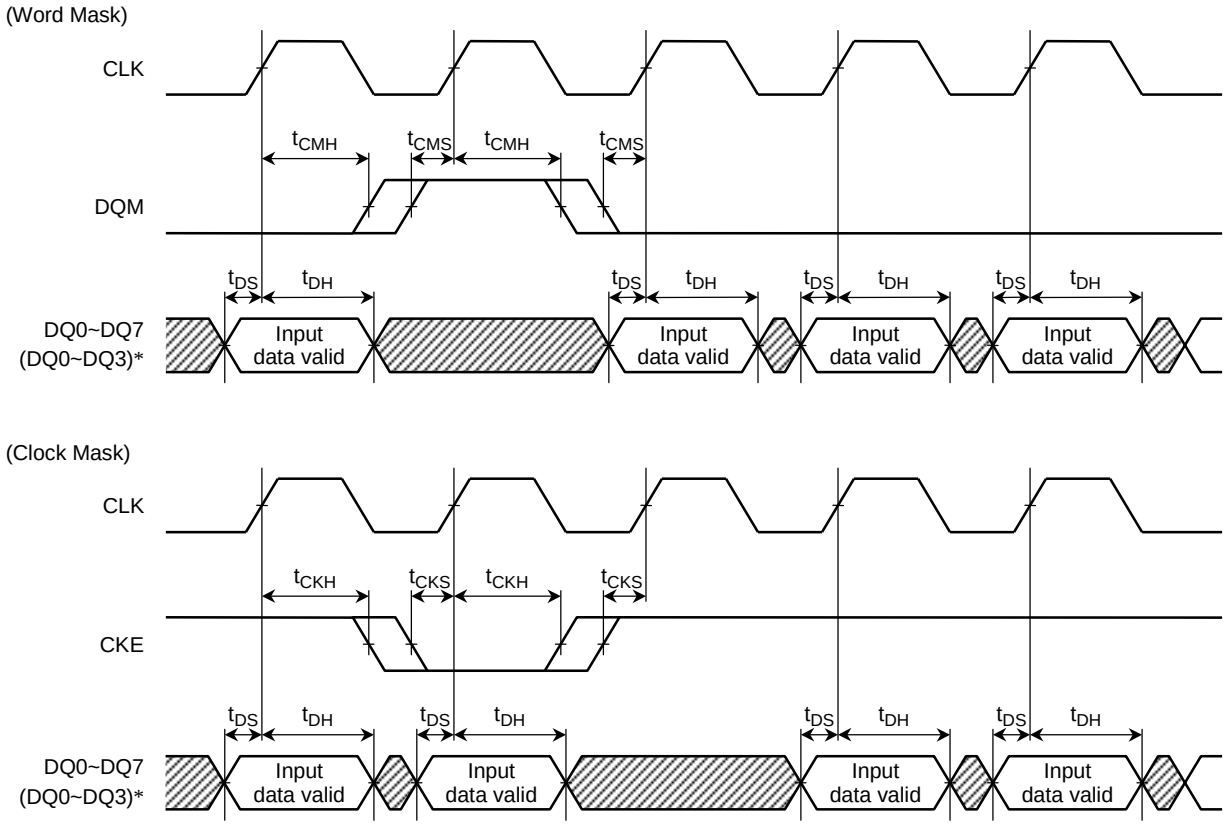
Command Input Timing



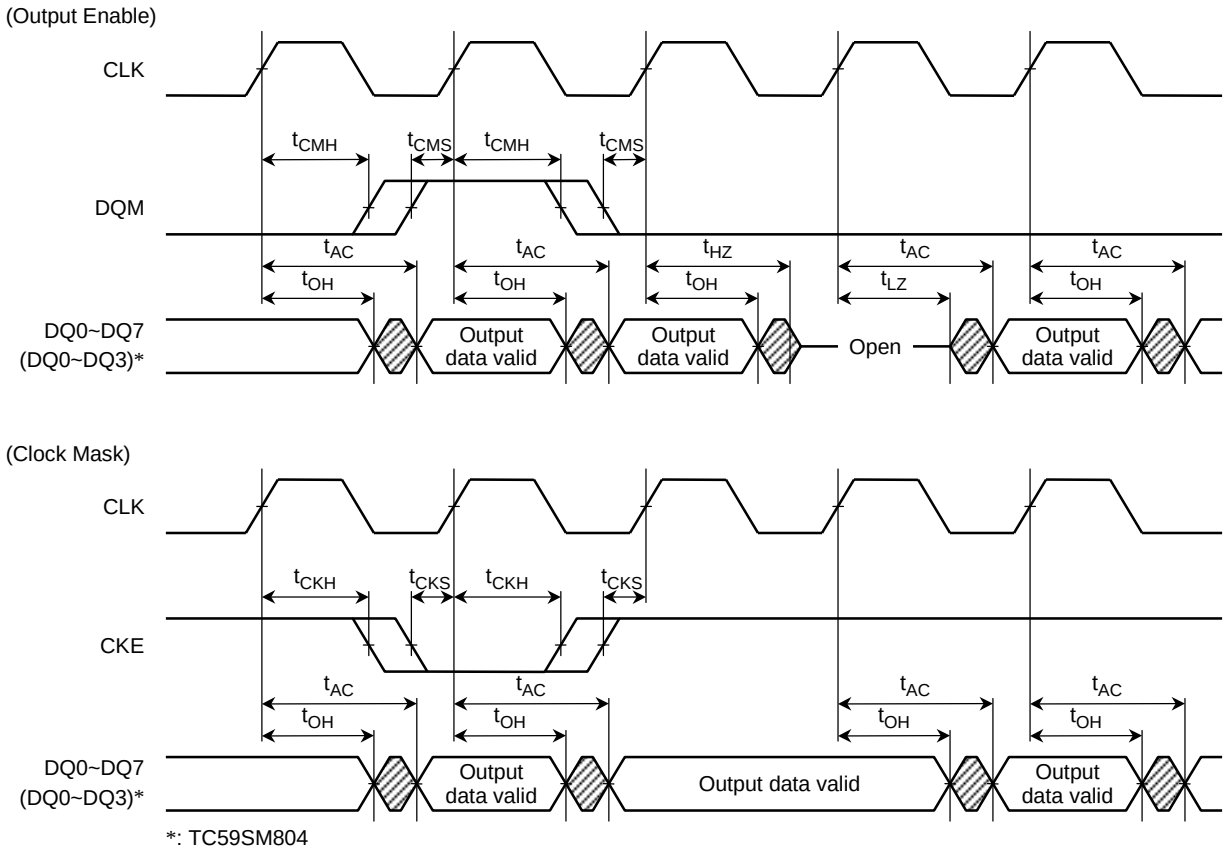
Read Timing


Read CAS latency
CLK
CS
RAS
CAS
WE
A0~A12
BS0, BS1
tAC
tLZ
tAC
tOH
tHZ
tOH
DQ
Output data valid
Output data valid
Read command
Burst length

Control Timing of Input Data (TC59SM808/M804)

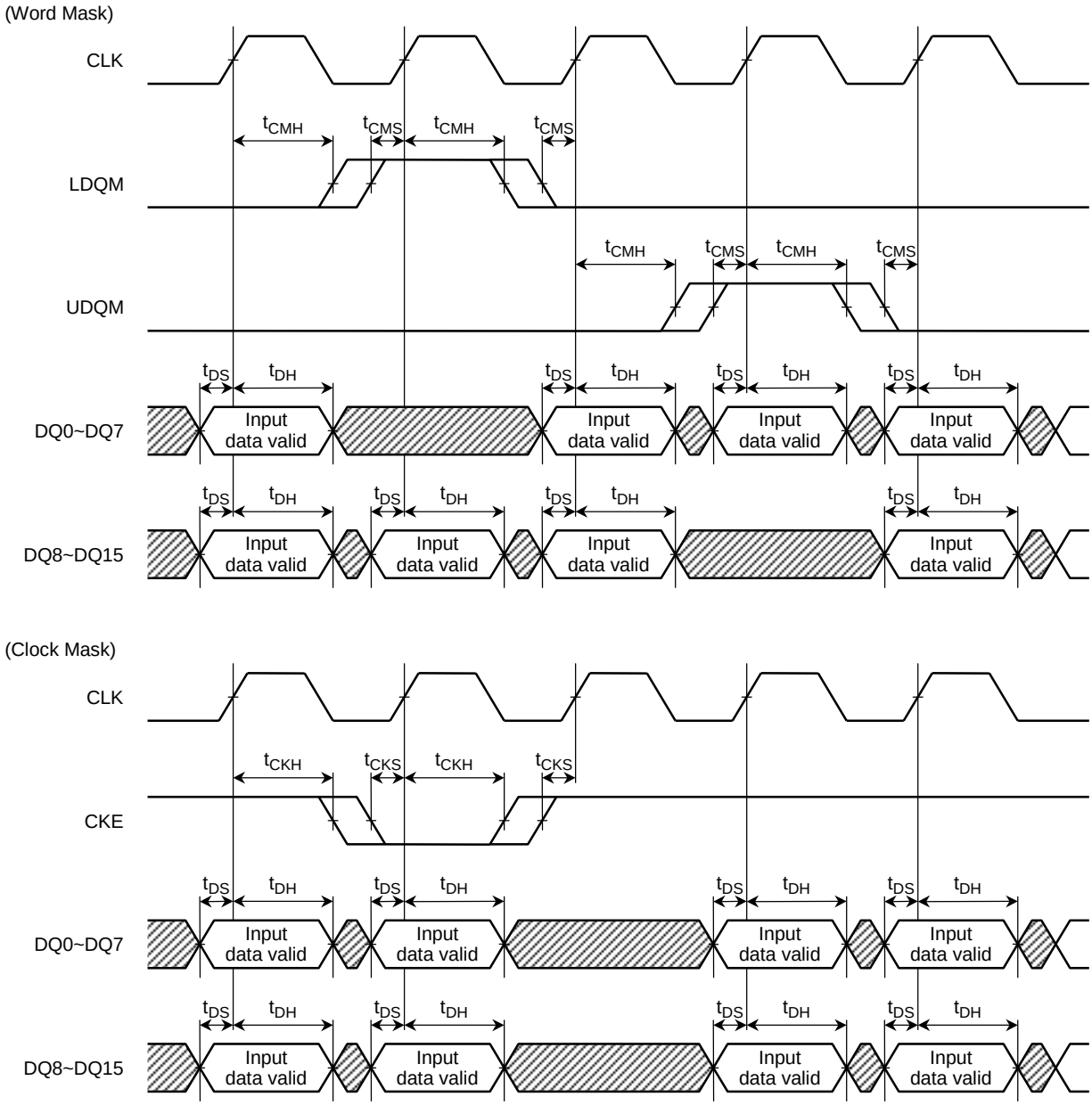


Control Timing of Output Data (TC59SM808/M804)

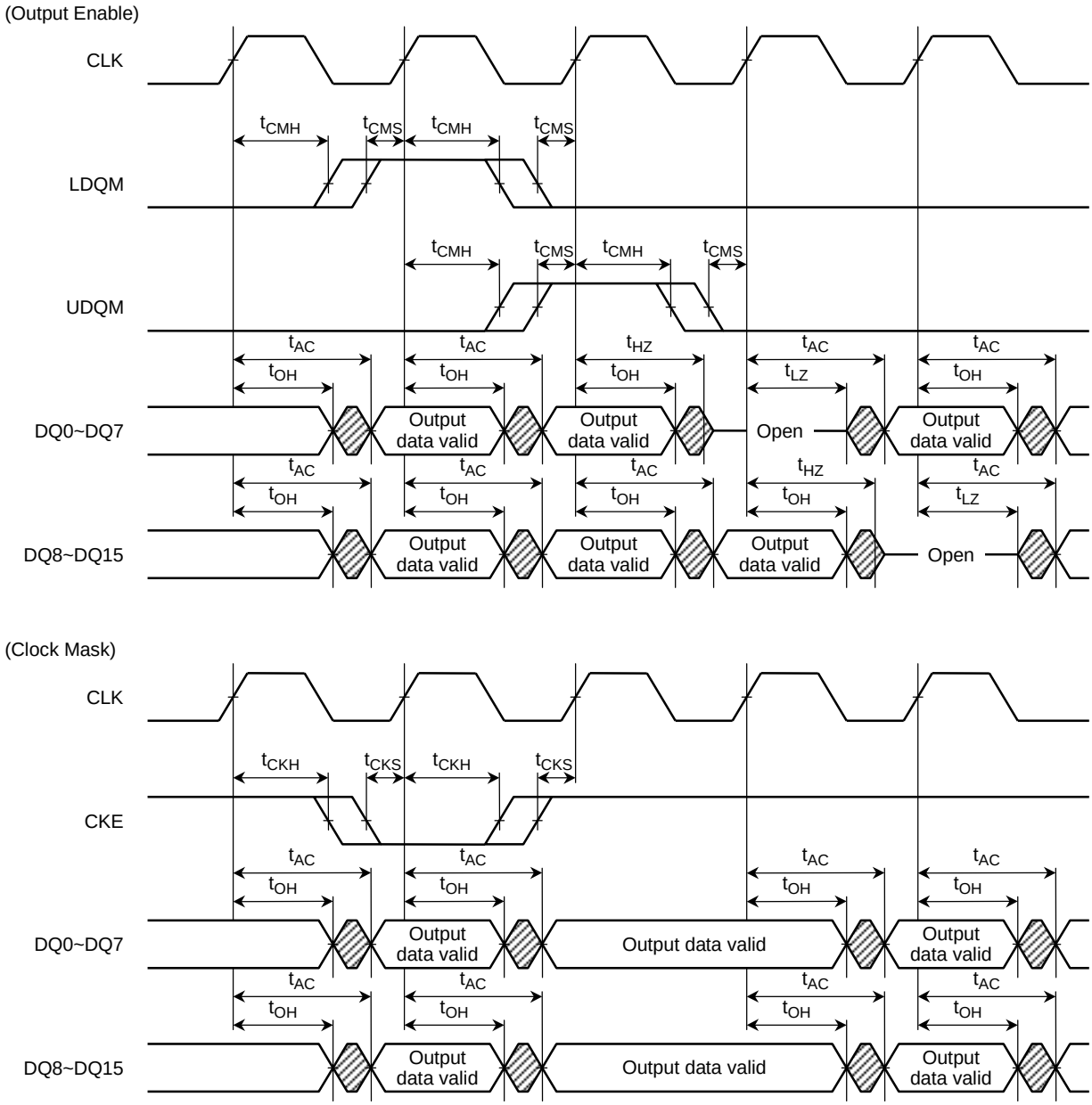


*: TC59SM804

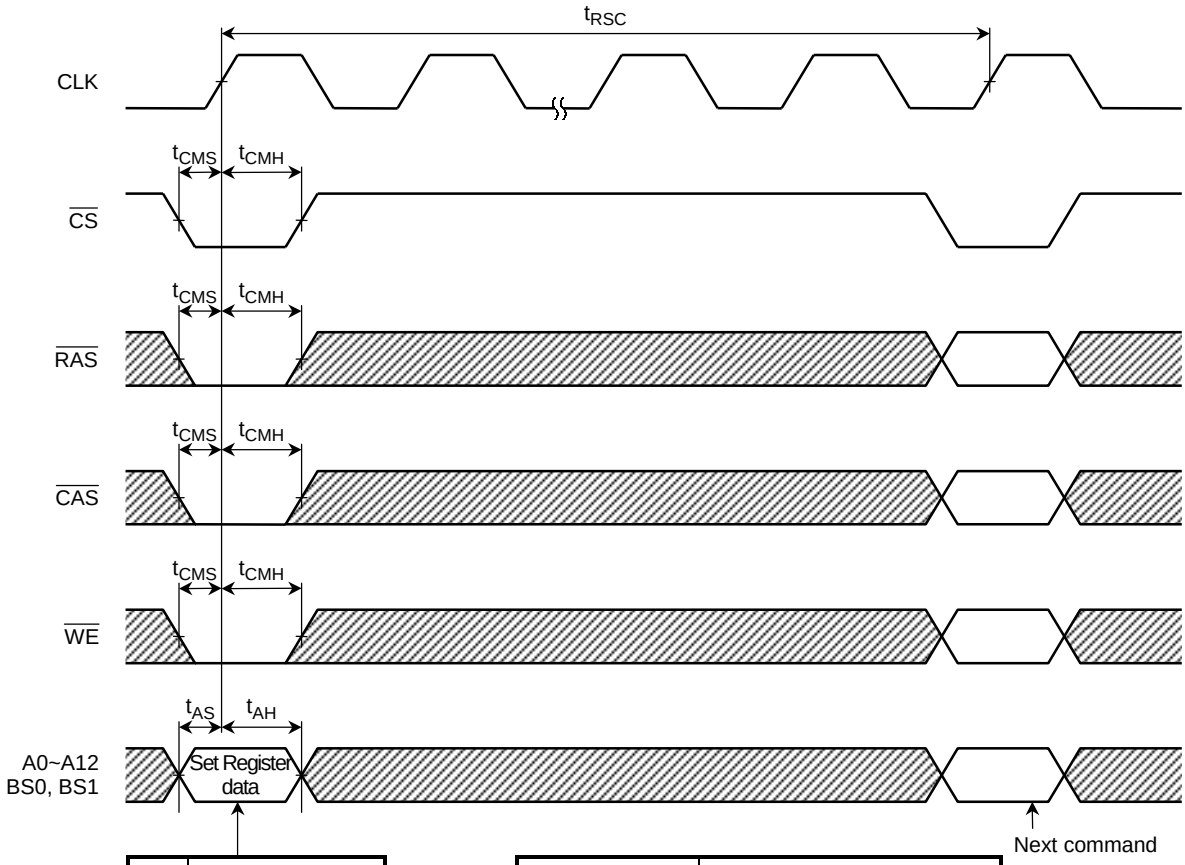
Control Timing of Input Data (TC59SM816)



Control Timing of Output Data (TC59SM816)



Mode Register Set Cycle



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	0	(Test Mode)
A8	0	Reserved
A9	Write Mode	
A10	0	Reserved
A11	0	
A12	0	
BS0	0	
BS1	0	

			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleaved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and Single write

OPERATING TIMING EXAMPLE

Figure 1. Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)

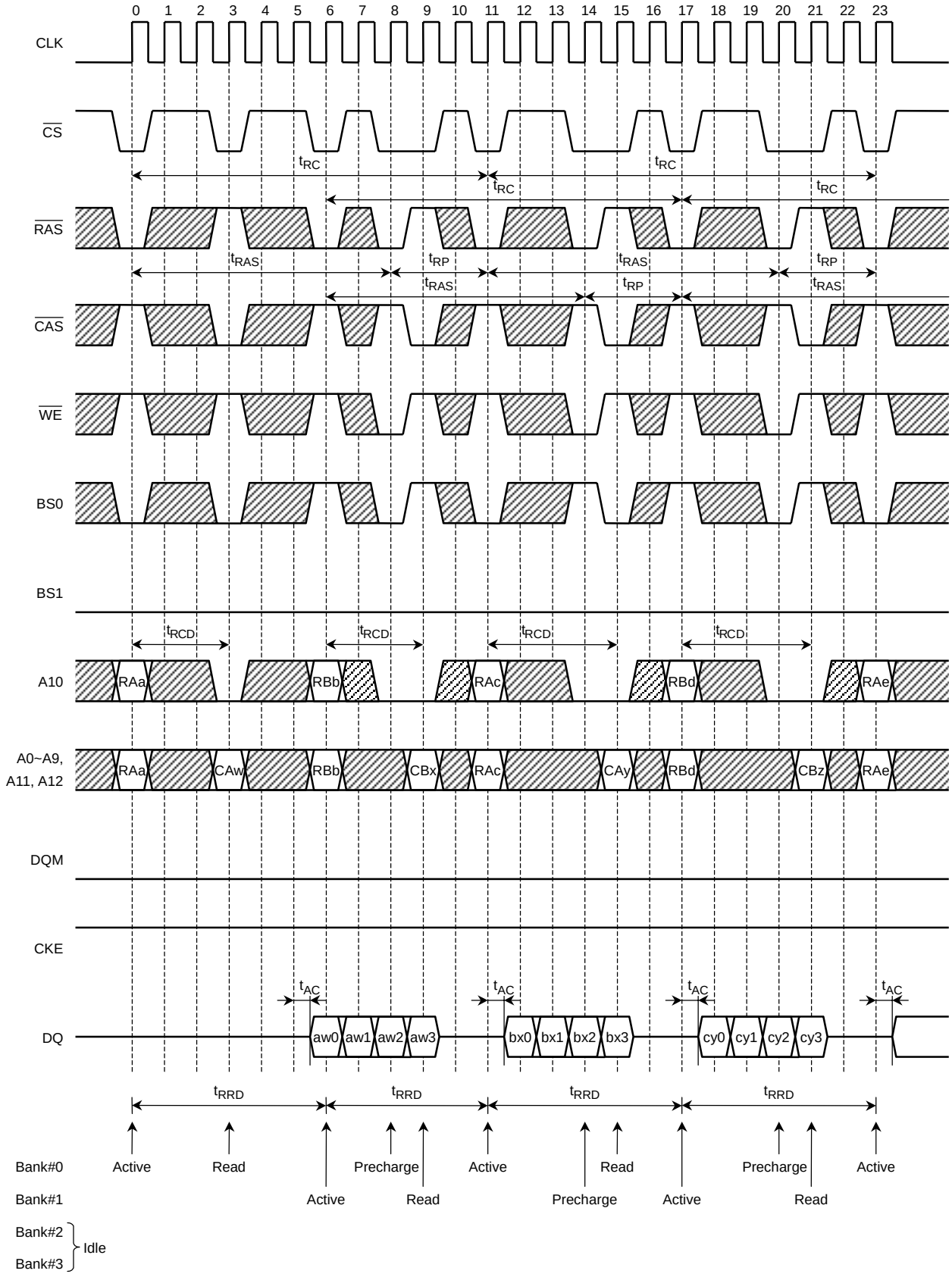
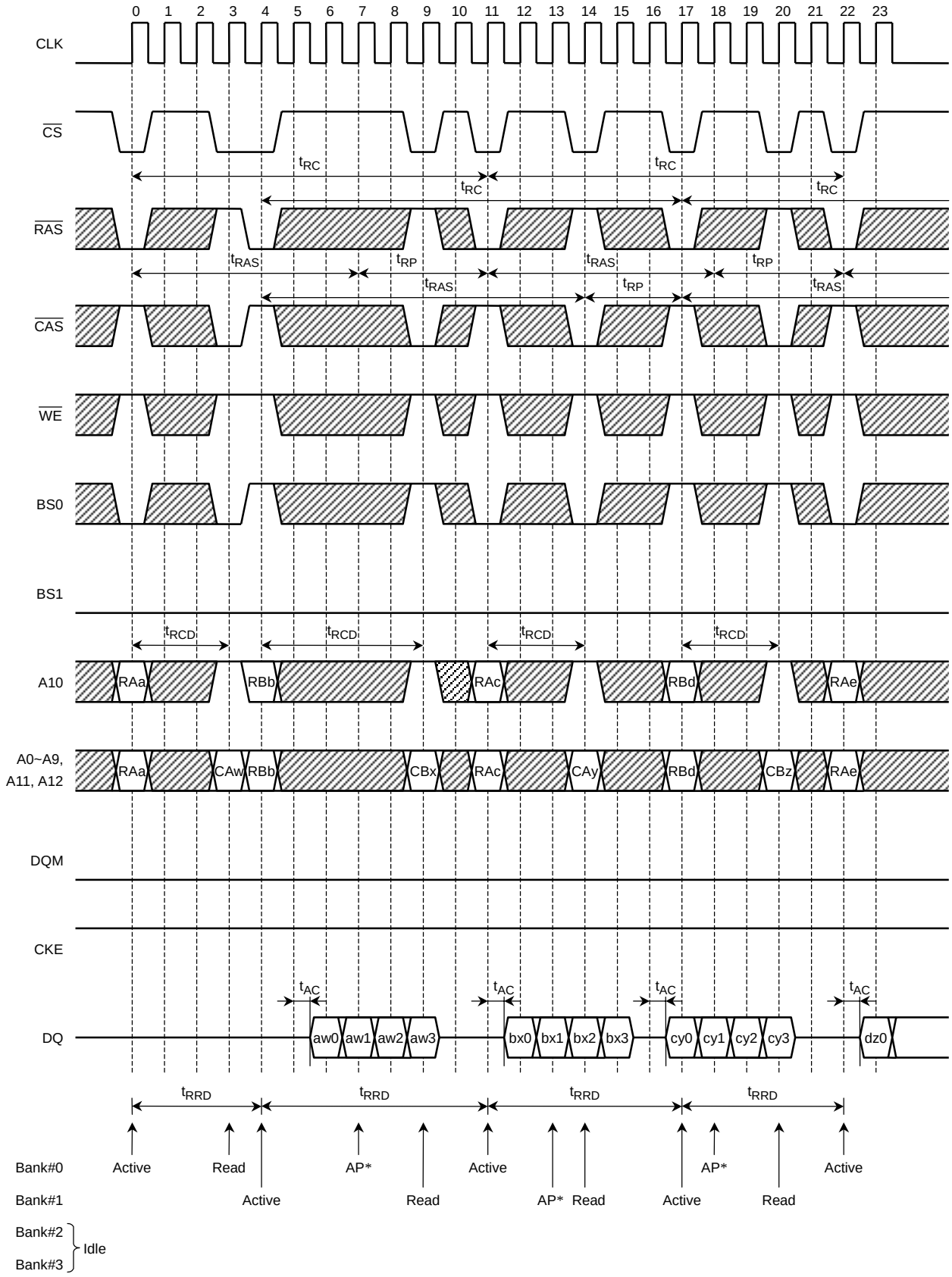


Figure 2. Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3, Auto Precharge)



*: AP shows internal precharge start timing.

Figure 3. Interleaved Bank Read (Burst Length = 8, $\overline{CAS}$ Latency = 3)

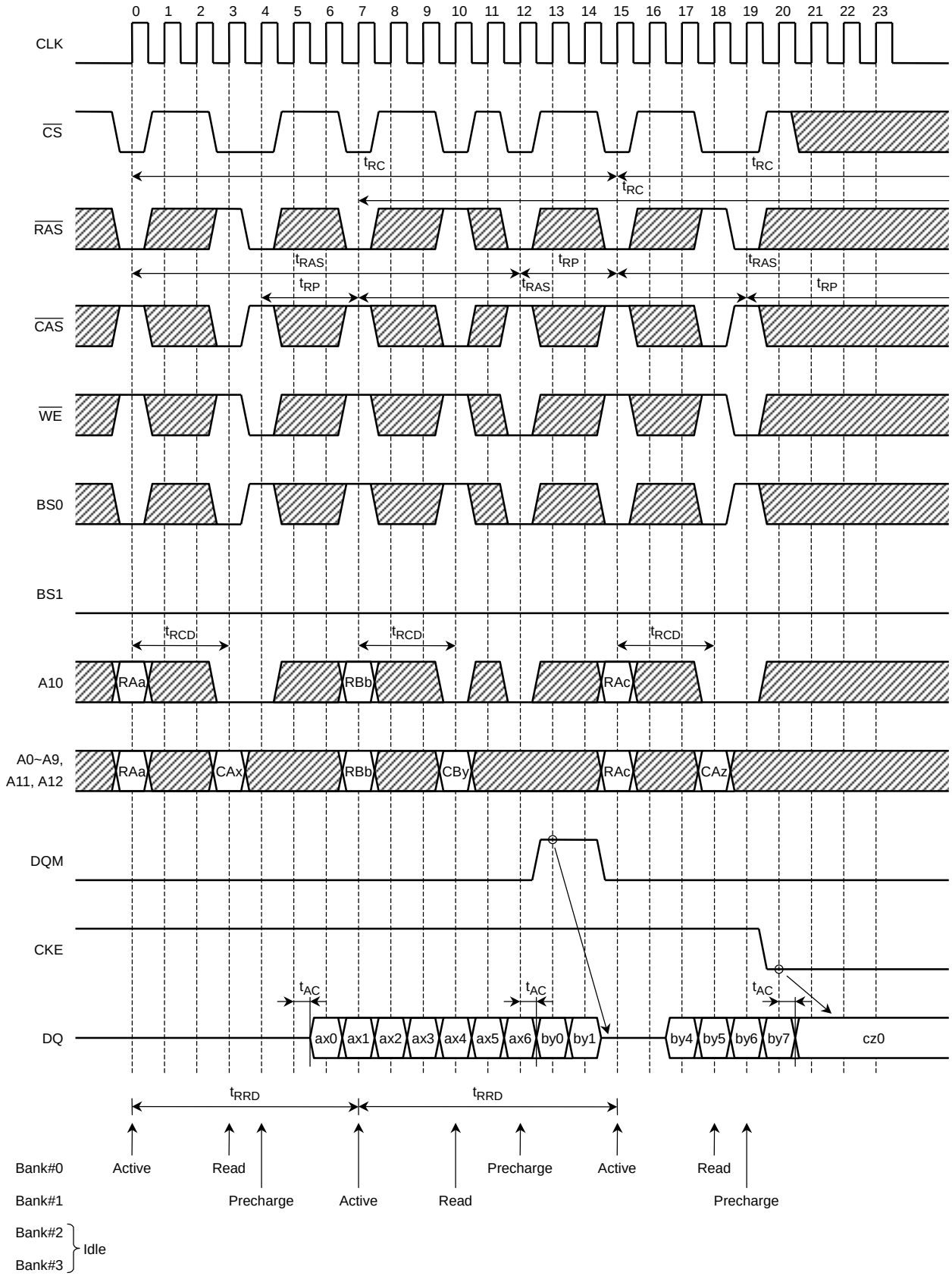
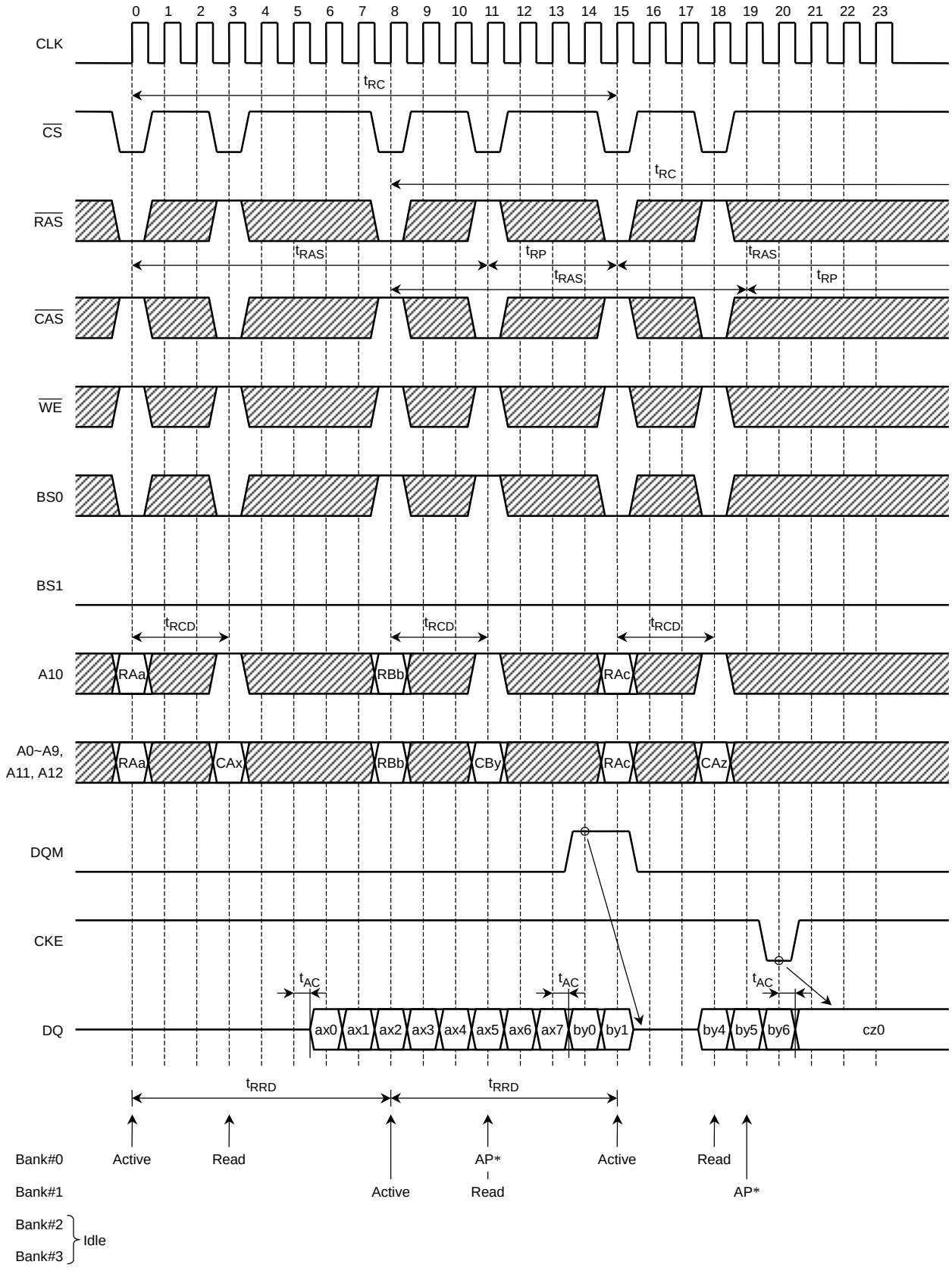


Figure 4. Interleaved Bank Read (Burst Length = 8, $\overline{CAS}$ Latency = 3, Auto Precharge)



*: AP shows the internal precharge start timing.

Figure 5. Interleaved Bank Write (Burst Length = 8)

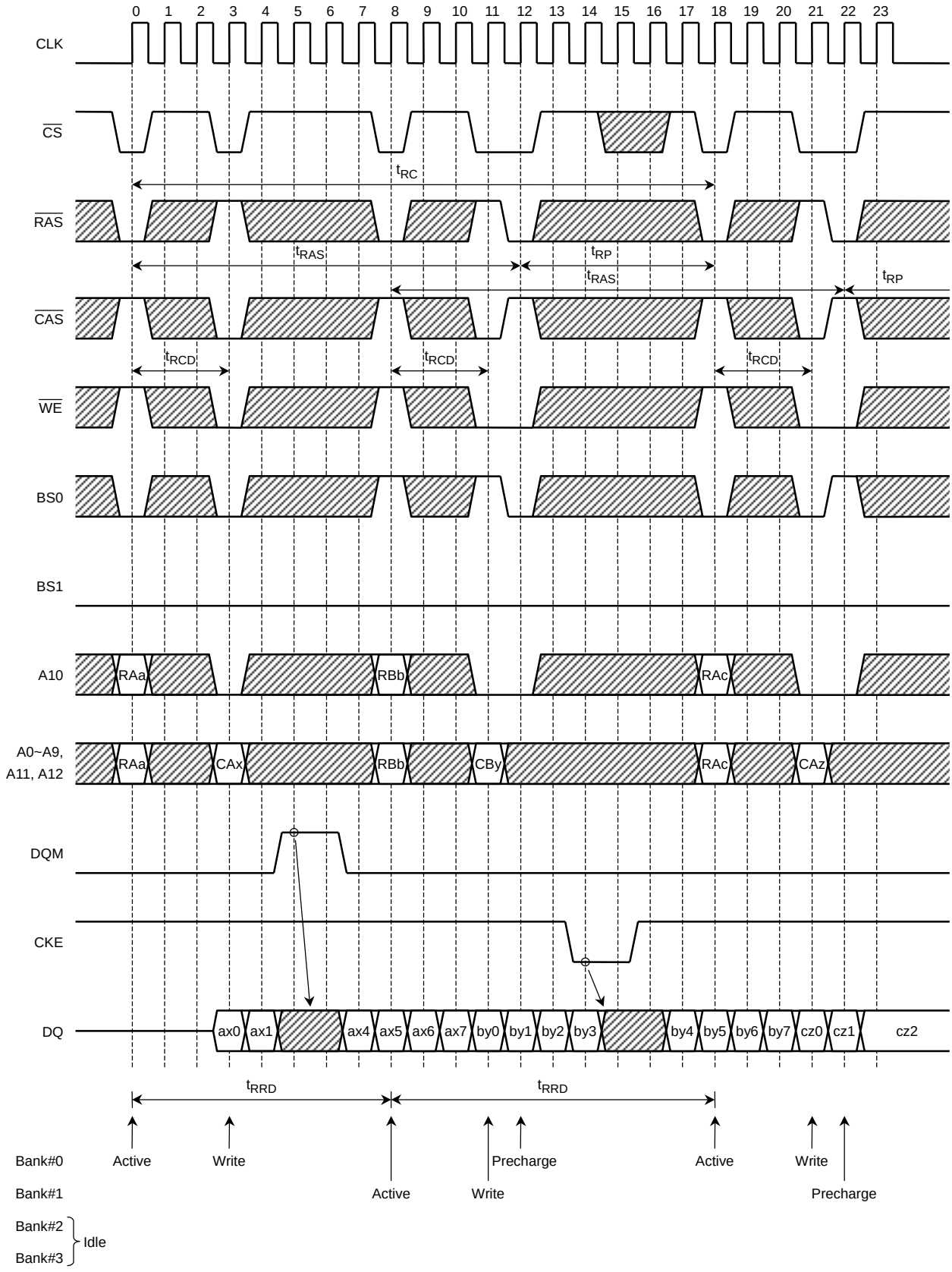
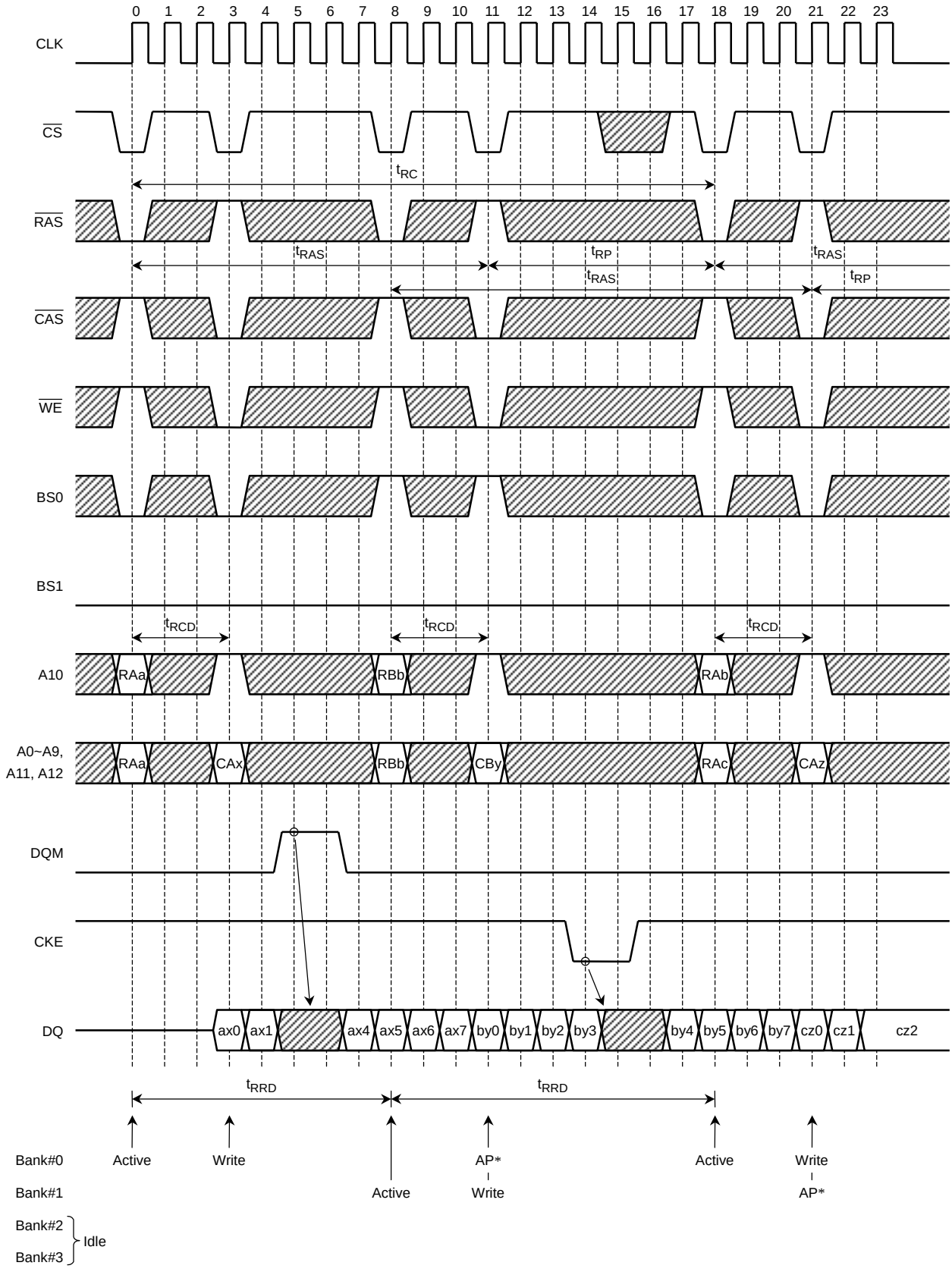
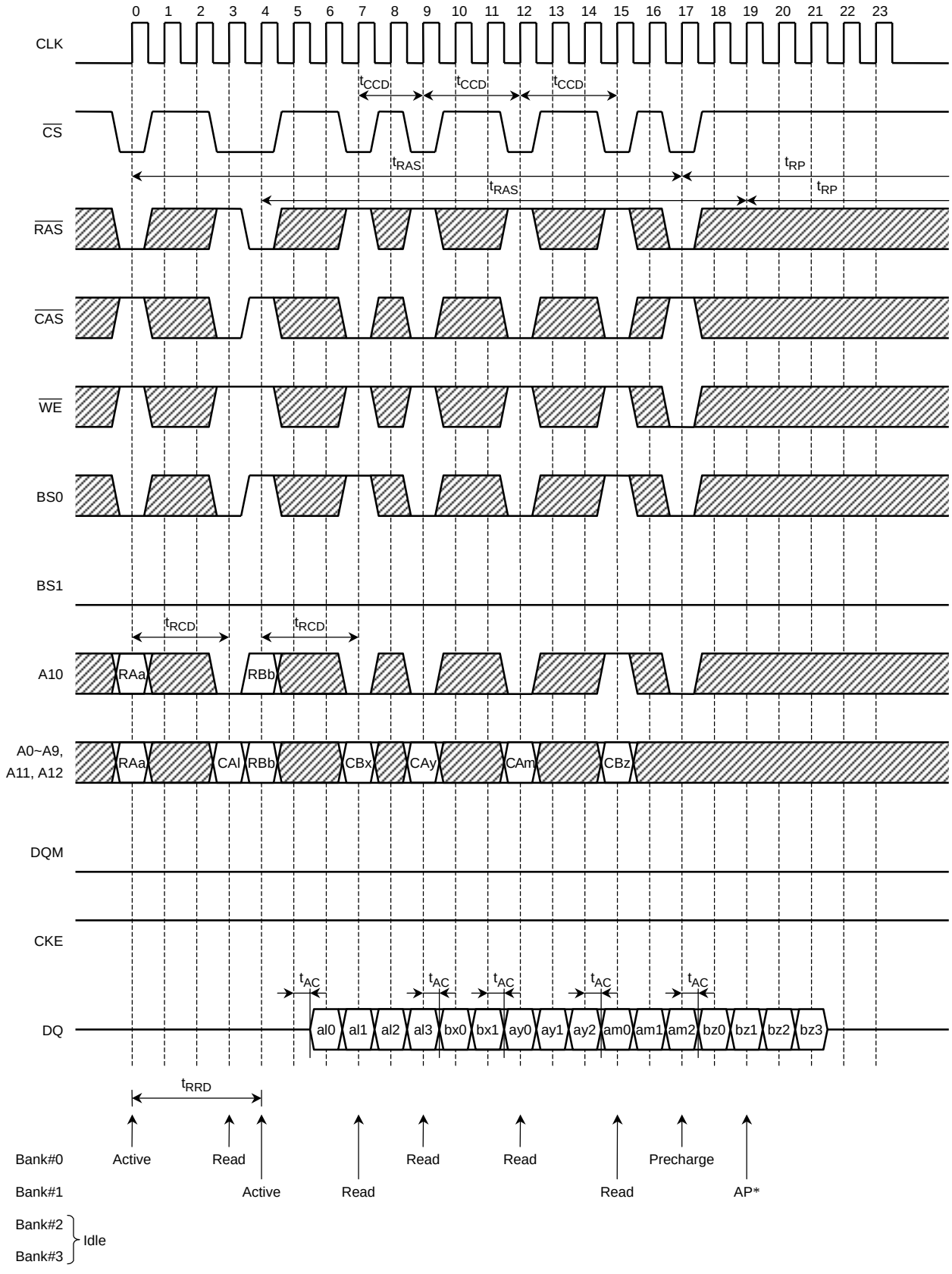


Figure 6. Interleaved Bank Write (Burst Length = 8, Auto Precharge)



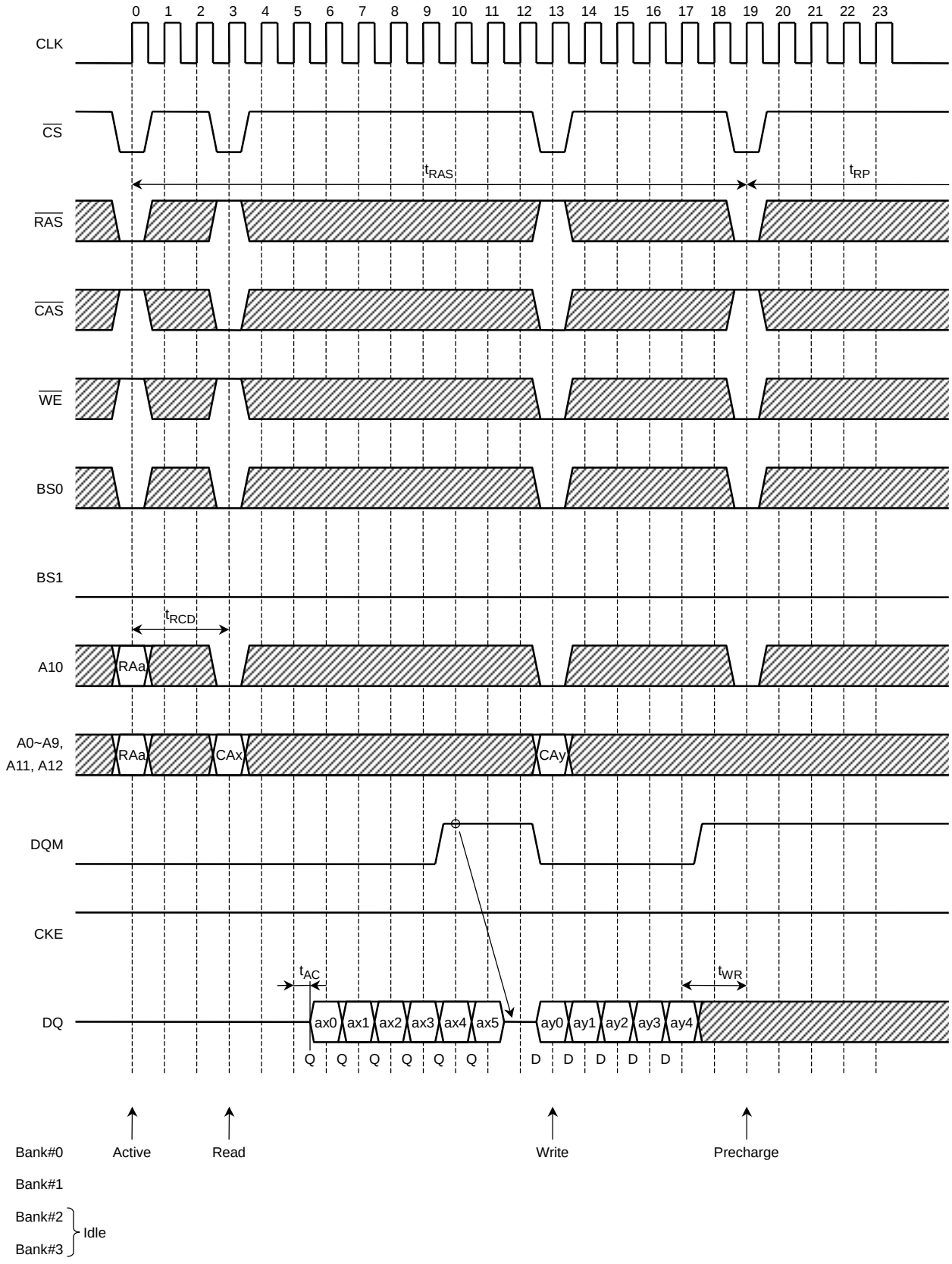
*: AP shows the internal precharge start timing.

Figure 7. Page Mode Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



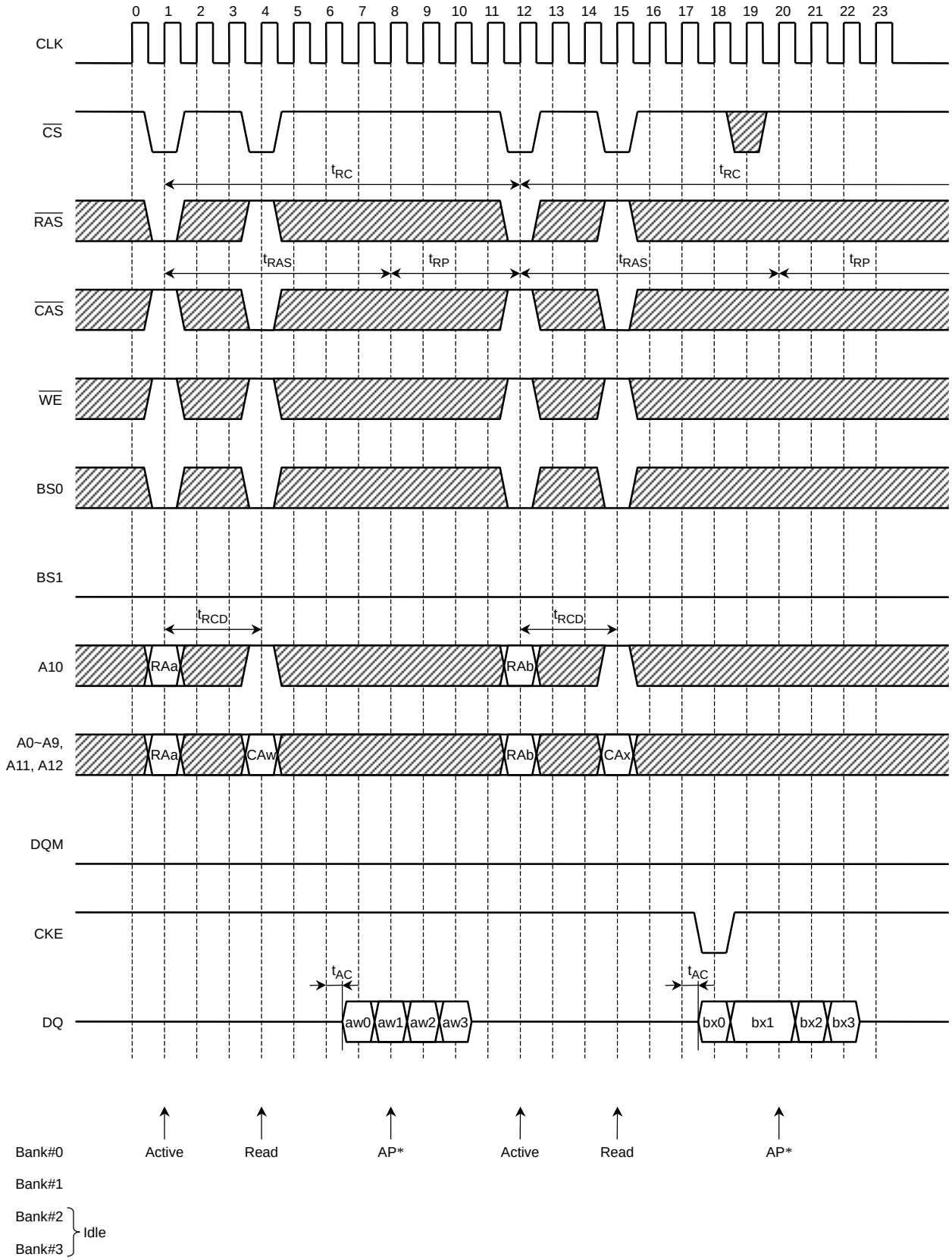
*: AP shows the internal precharge start timing.

Figure 8. Page Mode Read/Write (Burst Length = 8, $\overline{CAS}$ Latency = 3)



Note): See Figure 17, 20

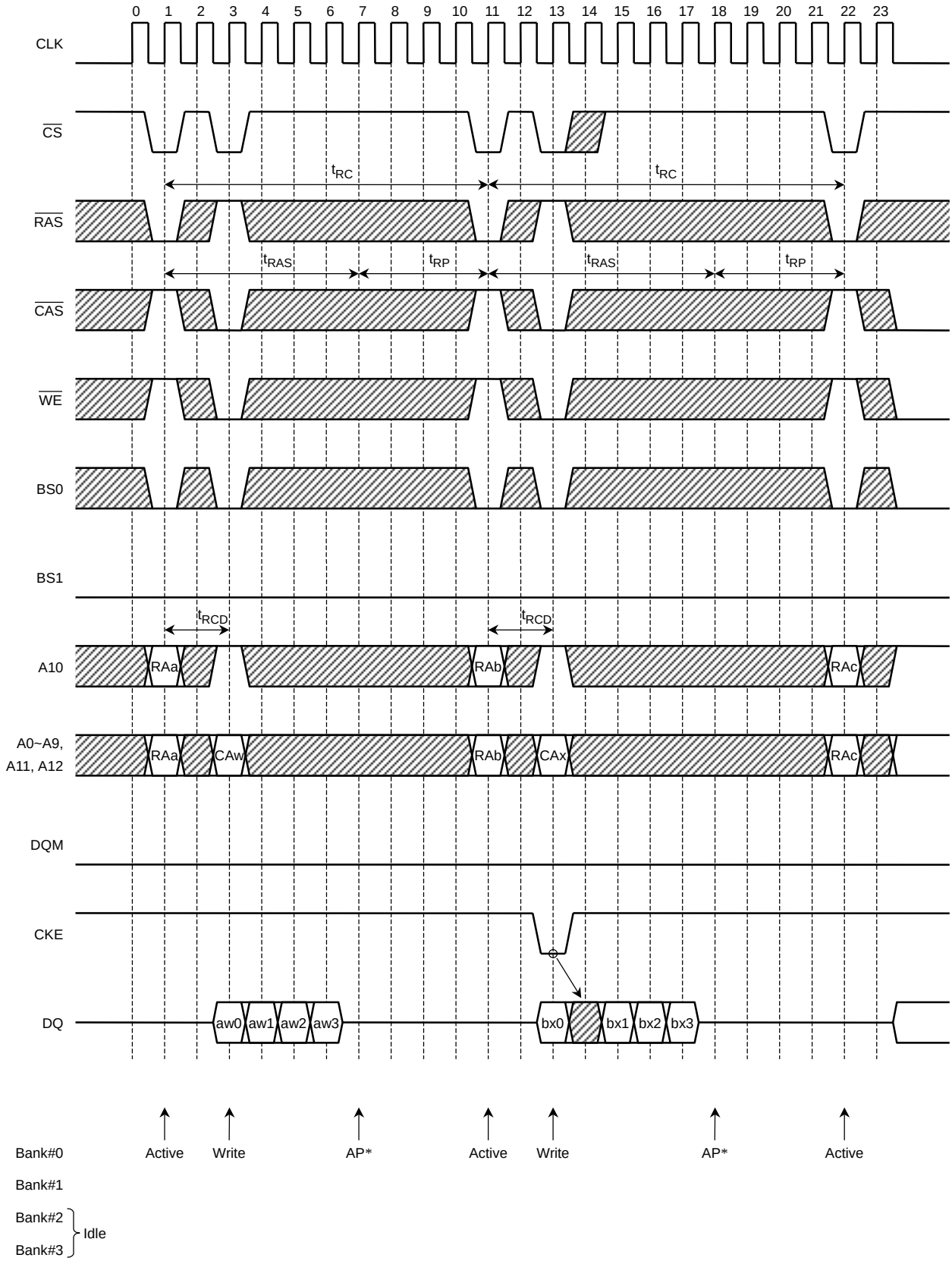
Figure 9. Auto Precharge Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



*: AP shows the internal precharge start timing.

Note): See Figure 15

Figure 10. Auto Precharge Write (Burst Length = 4)



*: AP shows the internal precharge start timing.

Note): See Figure 16

Figure 11. Auto Refresh Cycle

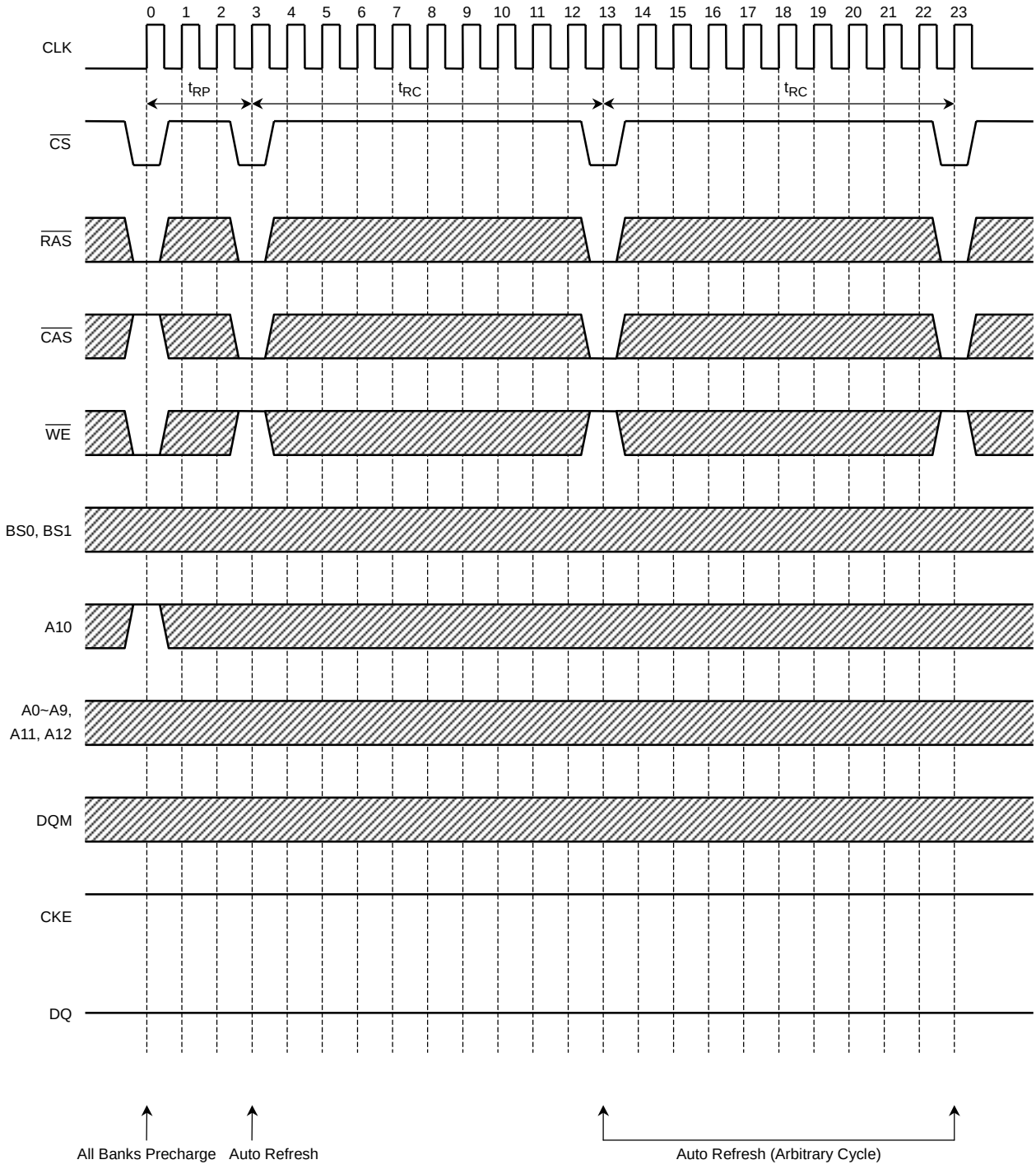


Figure 12. Self Refresh Cycle

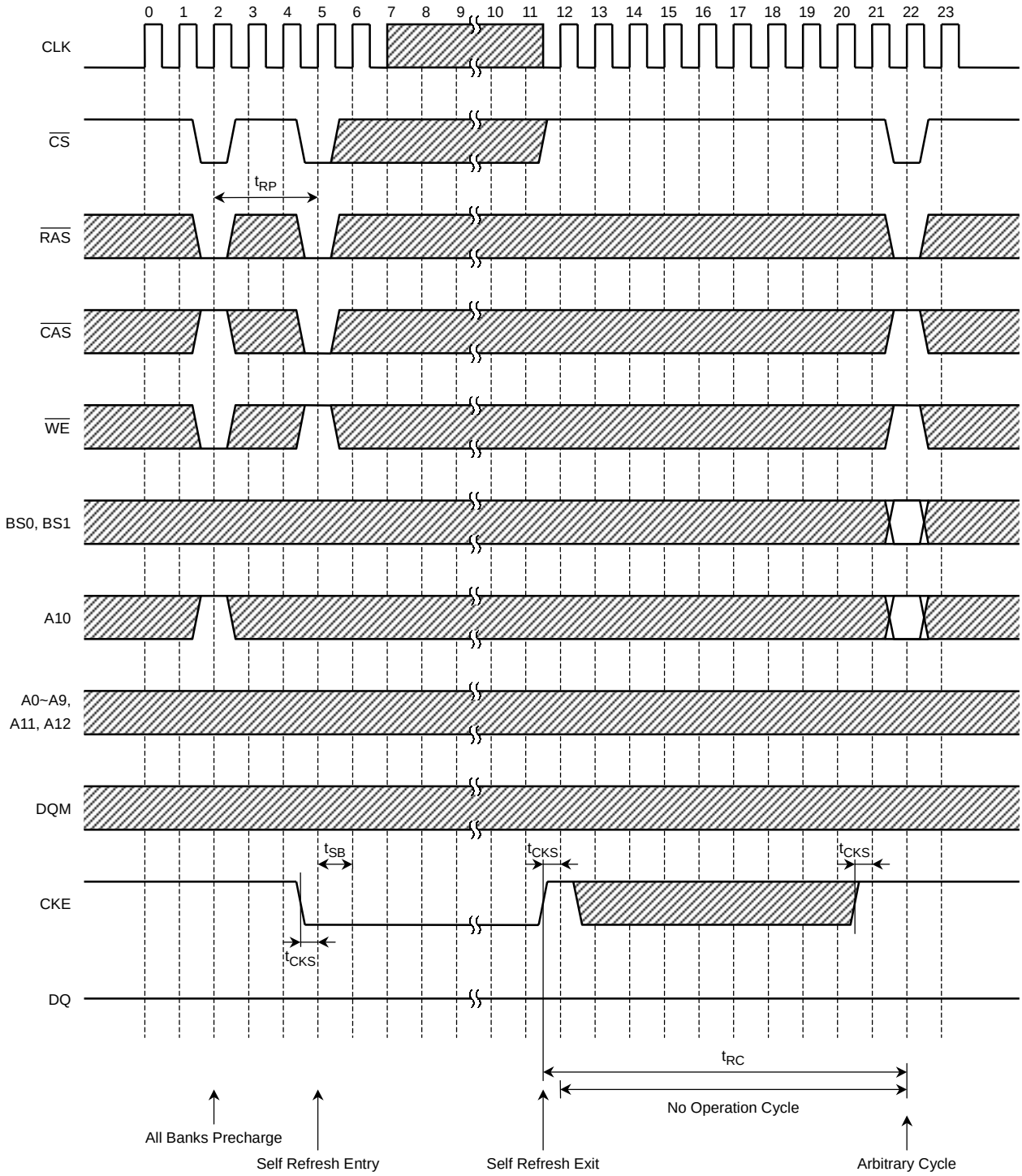
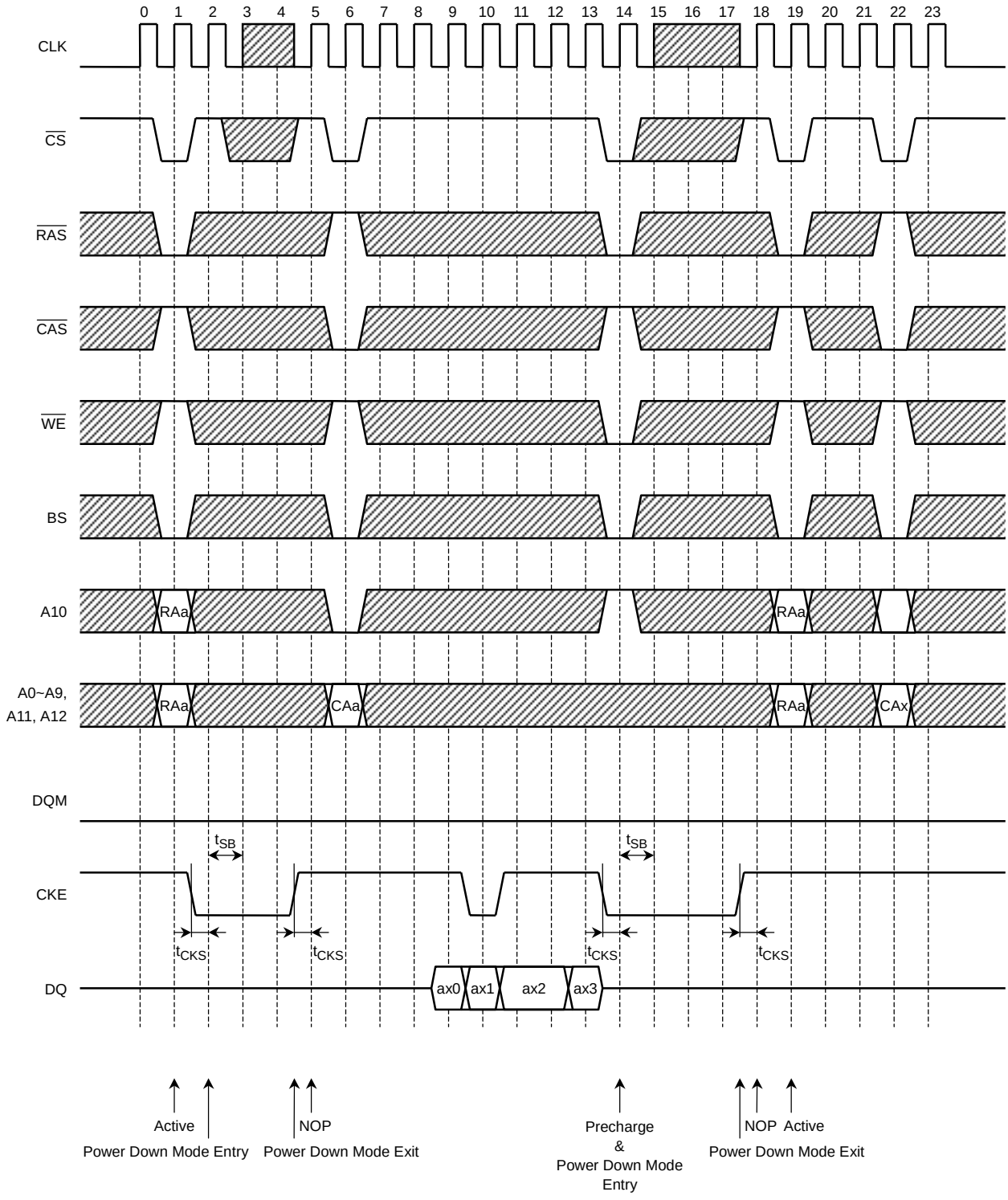


Figure 13. Power Down Mode

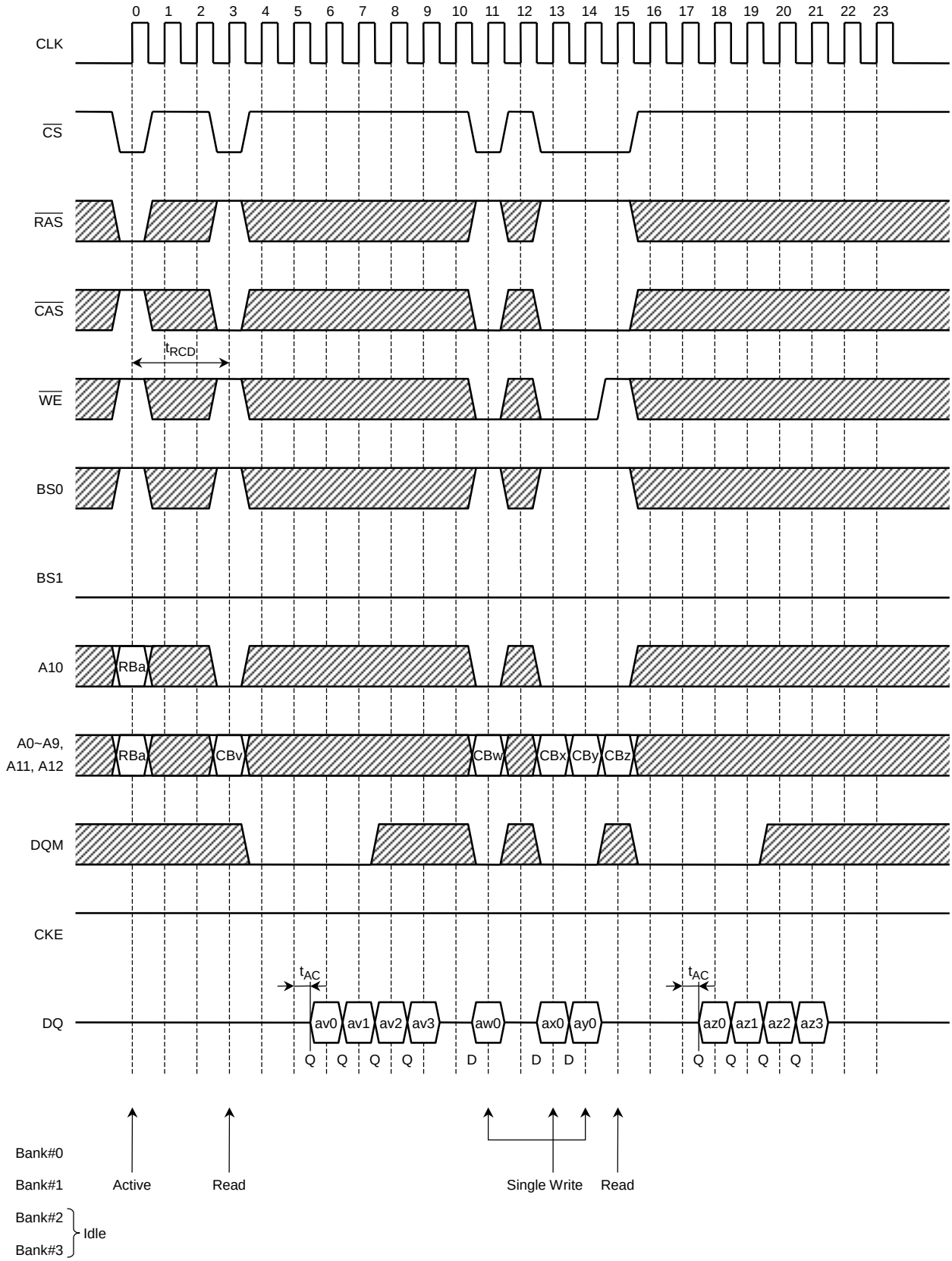


Note): The Power Down mode is invoked by asserting CKE "low".

All Input/Output buffers (except the CKE buffer) are turned off in Power Down mode.

When CKE goes high, the No-operation command input must be at next CLK rising edge and CKE should be set high at least 1CLK + t_{CKS} at Power Down Mode Exit.

Figure 14. Burst Read and Single Write (Burst Length = 4, $\overline{CAS}$ Latency = 3)



PIN FUNCTIONS

CLOCK INPUT: CLK

The CLK input is used as the reference for SDRAM operations. Operations are synchronized to the positive edges of CLK.

CLOCK ENABLE: CKE

The CKE input is used to suspend the internal CLK. When the CKE signal is asserted "low", the internal CLK is suspended and output data is held intact while CKE is asserted "low". When the device is not running a Burst cycle, the CKE input controls the entry to the Power Down and Self Refresh modes. When the Self Refresh command is issued, the device must be in the idle state.

BANK SELECT: BS0, BS1

The TC59SM816CMB/CMBL, TC59SM808CMB/CMBL and the TC59SM804CMB/CMBL are organized as four-bank memory cell arrays. The BS0, BS1 inputs are latched at the time of assertion of the operation commands and selects the bank to be used for the operation.

BS0	BS1	
0	0	Bank#0
1	0	Bank#1
0	1	Bank#2
1	1	Bank#3

ADDRESS INPUTS: A0~A12

The A0~A12 inputs are address to access the memory cell array, as following table.

	Row Address	Column Address
TC59SM816CMB/CMBL	A0~A12	A0~A8
TC59SM808CMB/CMBL	A0~A12	A0~A9
TC59SM804CMB/CMBL	A0~A12	A0~A9, A11

The row address bits are latched at the Bank Activate command and column address bits are latched on the Read or Write command. Also, the A0~A12 inputs are used to set the data in the Mode register in a Mode Register Set cycle.

CHIP SELECT: $\overline{CS}$

The $\overline{CS}$ input controls the latching of the commands on the positive edges of CLK when $\overline{CS}$ is asserted "low". No commands are latched as long as $\overline{CS}$ is held "high".

ROW ADDRESS STROBE: $\overline{RAS}$

The $\overline{RAS}$ input defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ inputs, and is latched at the positive edges of CLK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "low" and $\overline{CAS}$ is asserted "high", either the Bank Activate command or the Precharge command is selected by the $\overline{WE}$ signal. When $\overline{WE}$ is asserted "high", the Bank Activate command is selected and the bank designated by BS0, BS1 are turned on so that it is in the active state. When $\overline{WE}$ is asserted "low", the Precharge command is selected and the bank designated by BS0, BS1 are switched to the idle state after Precharge operation.

COLUMN ADDRESS STROBE: $\overline{CAS}$

The $\overline{CAS}$ input defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ inputs, and is latched at the positive edges of CLK. When $\overline{RAS}$ is held "high" and $\overline{CS}$ is asserted "low", column access is started by asserting $\overline{CAS}$ "low". Then, the Read or Write command is selected by asserting $\overline{WE}$ "low" or "high".

WRITE ENABLE: $\overline{WE}$

The $\overline{WE}$ input defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ inputs, and is latched at the positive edges of CLK. The $\overline{WE}$ input is used to select the Bank Activate or Precharge command and Read or Write command.

DATA INPUT/OUTPUT MASK: DQM or LDQM and UDQM

The DQM input enables output in a Read cycle and functions as the input data mask in a Write cycle. When DQM is asserted "high" at the positive edges of CLK, output data is disabled after two clock cycles during a Read cycle, and input data is masked at the same clock cycle during a Write cycle.

In the case of the TC59SM816CMB/CMBL, the LDQM and UDQM inputs function as byte data control. The LDQM input can control DQ0~DQ7 in a Read or Write cycle and the UDQM can control DQ8~DQ15 in a Read or Write cycle.

DATA INPUT/OUTPUT: DQ0~DQ15

The DQ0~DQ15 input and output data are synchronized with the positive edges of CLK. In the case of TC59SM808CMB/CMBL and TC59SM804CMB/CMBL, these pins are DQ0~DQ7 and DQ0~DQ3 respectively.

Operation Mode

Table 1 shows the truth table for the operation commands.

Table 1. Truth Table (Note (1) and (2))

Command	Device State	CKE_{n-1}	CKE_n	DQM (5)	BS0, BS1	A10	A12, A11, A9~A0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Activate	Idle (3)	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active (3)	H	X	X	V	L	V	L	H	L	L
Write with Auto Precharge	Active (3)	H	X	X	V	H	V	L	H	L	L
Read	Active (3)	H	X	X	V	L	V	L	H	L	H
Read with Auto Precharge	Active (3)	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst stop	Active (4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto-Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self-Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self-Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Idle/Active (6)	H	L	X	X	X	X	H	X	X	X
								L	H	H	X
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Note 1. V = Valid, X = Don't Care, L = Low level, H = High level
2. CKE_n signal is input level when commands are issued.
CKE_{n-1} signal is input level one clock cycle before the commands are issued.
3. These are state designated by the BS0, BS1 signals.
4. Device state is Full Page Burst operation.
5. LDQM, UDQM (TC59SM816CMB/CMBL)
6. Power Down Mode can not entry in the burst cycle.
When this command assert in the burst cycle, device state is clock suspend mode.

1. Command Function

1-1 Bank Activate command
($\overline{RAS}$ = L, $\overline{CAS}$ = H, $\overline{WE}$ = H, BS0, BS1 = Bank, A0~A12 = Row Address)

The Bank Activate command activates the bank designated by the BS (Bank Select) signal.
Row addresses are latched on A0~A12 when this command is issued and the cell data is read out to the sense amplifiers. The maximum time that each bank can be held in the active state is specified as t_{RAS} (max).

1-2 Bank Precharge command
($\overline{RAS}$ = L, $\overline{CAS}$ = H, $\overline{WE}$ = L, BS0, BS1 = Bank, A10 = L, A0~A9, A11, A12 = Don't care)

The Bank Precharge command precharges the bank designated by BS. The precharged bank is switched from the active state to the idle state.

1-3 Precharge All command
($\overline{RAS}$ = L, $\overline{CAS}$ = H, $\overline{WE}$ = L, BS0, BS1 = Don't care, A10 = H, A0~A9, A11, A12 = Don't care)

The Precharge All command precharges all banks simultaneously. All banks are then switched to the idle state.

1-4 Write command
($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = L, BS0, BS1 = Bank, A10 = L, A0~A9, A11 = Column Address, A12 = Don't care)

The Write command performs a Write operation to the bank designated by BS0 and BS1. The write data is latched at the positive edges of CLK. The length of the write data (Burst Length) and column access sequence (Addressing Mode) must be programmed in the Mode Resister at power-up prior to the Write operation.
The A11 input is "Don't care" on the TC59SM808CMB/CMBL and the A9 and A11 inputs are "Don't care" on the TC59SM816CMB/CMBL.

1-5 Write with Auto Precharge command
($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = L, BS0, BS1 = Bank, A10 = H, A0~A9, A11 = Column Address, A12 = Don't care)

The Write with Auto Precharge command performs the Precharge operation automatically after the Write operation. The internal precharge starts in the cycles immediately following the cycle in which the last data is written independent of $\overline{CAS}$ Latency (Figure 16). This command must not be interrupted by any other commands.
The A11 input is "Don't care" at the TC59SM808CMB/CMBL and the A9 and A11 inputs are "Don't care" on the TC59SM816CMB/CMBL.

1-6 Read command
($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = H, BS0, BS1 = Bank, A10 = L, A0~A9, A11 = Column Address, A12 = Don't care)

The Read command performs a Read operation to the bank designated by BS. The read data is issued sequentially synchronized to the positive edges of CLK. The length of read data (Burst Length), Addressing Mode and $\overline{CAS}$ Latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode Register at power-up prior to the Write operation.
The A11 input is "Don't care" on the TC59SM808CMB/CMBL and the A9 and A11 inputs are "Don't care" on the TC59SM816CMB/CMBL.

1-7 Read with Auto Precharge command
($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = H, BS0, BS1 = Bank, A10 = H, A0~A9, A11 = Column Address, A12 = Don't care)

The Read with Auto Precharge command automatically performs the Precharge operation after the Read operation. When the $\overline{CAS}$ Latency = 3, the internal precharge starts two cycles before the last data is output. When the $\overline{CAS}$ Latency = 2, the internal precharge starts one cycle before the last data is output (Figure 15). This command must not be interrupted by any other command.

The A11 input is "Don't care" on the TC59SM808CMB/CMBL and the A9 and A11 inputs are "Don't care" on the TC59SM816CMB/CMBL.

1-8 Mode Register Set command
($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = L, BS0, BS1, A0~A12 = Register Data)

The Mode Register Set command programs the values of $\overline{CAS}$ latency, Addressing Mode and Burst Length in the Mode Register. The default values in the Mode Register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while all banks are in the idle state.

1-9 No-Operation command
($\overline{RAS}$ = H, $\overline{CAS}$ = H, $\overline{WE}$ = H)

The No-Operation command simply performs no operation.

1-10 Burst stop command
($\overline{RAS}$ = H, $\overline{CAS}$ = H, $\overline{WE}$ = L)

The Burst stop command is used to stop the burst operation. This command is valid during a Full Page Burst operation. During other types of Burst operation, the command is illegal.

1-11 Device Deselect command
($\overline{CS}$ = H)

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

1-12 Auto Refresh command
($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = H, CKE = H, BS0, BS1, A0~A12 = Don't care)

The Auto Refresh command is used to refresh the row address provided by the internal refresh counter. The Refresh operation must be performed 8192 times within 64 ms. The next command can be issued after t_{RC} from the end of the Auto Refresh command. When the Auto Refresh command is issued, All banks must be in the idle state. The Auto Refresh operation is equivalent to the $\overline{CAS}$-before-$\overline{RAS}$ operation in a conventional DRAM.

1-13 Self Refresh Entry command
($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = H, CKE = L, BS0, BS1, A0~A12 = Don't care)

The Self Refresh Entry command is used to enter Self Refresh mode. While the device is in Self Refresh mode, all input and output buffers (except the CKE buffer) are disabled and the Refresh operation is automatically performed. Self Refresh mode is exited by taking CKE "high" (the Self Refresh Exit command).

1-14 Self Refresh Exit command
(CKE = H, $\overline{CS}$ = H or CKE = H, $\overline{RAS}$ = H, $\overline{CAS}$ = H)

This command is used to exit from Self Refresh mode. Any subsequent commands can be issued after t_{RC} from the end of this command.

1-15 Clock Suspend Mode Entry/Power Down Mode Entry command
(CKE = L)

The internal CLK is suspended for one cycle when this command is issued (when CKE is asserted "low"). The device state is held intact while the CLK is suspended. On the other hand, when the device is not operating the Burst cycle, this command performs entry into Power Down mode. All input and output buffers (except the CKE buffer) are turned off in Power Down mode.

1-16 Clock Suspend Mode Exit/Power Down Mode Exit command
(CKE = H)

When the internal CLK has been suspended, operation of the internal CLK is resumed by providing this command (asserting CKE "high"). When the device is in Power Down mode, the device exits this mode and all disabled buffers are turned on to the active state. Any subsequent commands can be issued after one clock cycle from the end of this command.

1-17 Data Write/Output Enable, Data Mask/Output Disable command
(DQM = L/H or LDQM, UDQM = L/H)

During a Write cycle, the DQM or LDQM, UDQM signal functions as Data Mask and can control every word of the input data. During a Read cycle, the DQM or LDQM, UDQM signal functions as the control of output buffers.

The LDQM signal controls DQ0~DQ7 and the UDQM signal controls DQ8~DQ15.

2. Read Operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued after t_{RCD} from the Bank Activate command, the data is read out sequentially, synchronized to the positive edges of CLK (a Burst Read operation). The initial read data becomes available after $\overline{CAS}$ Latency from the issuing of the Read command. The $\overline{CAS}$ latency must be set in the Mode Register at power-up. In addition, the burst length of read data and Addressing Mode must be set. Each bank is held in the active state unless the Precharge command is issued, so that the sense amplifiers can be used as secondary cache.

When the Read with Auto Precharge command is issued, the Precharge operation is performed automatically after the Read cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Also, when the Burst Length is 1 and t_{RCD} (min), the timing from the $\overline{RAS}$ command to the start of the Auto Precharge operation is shorter than t_{RAS} (min). In this case, t_{RAS} (min) must be satisfied by extending t_{RCD} (Figure 9, 15).

When the Precharge operation is performed on a bank during a Burst Read operation, the Burst operation is terminated (Figure 20).

When the Burst Length is full-page, column data is repeatedly read out until the Burst Stop command or Precharge command is issued.

3. Write Operation

Issuing the Write command after t_{RCD} from the Bank Activate command, the input data is latched sequentially, synchronizing with the positive edges of CLK after the Write command (Burst Write operation). The burst length of the Write data (Burst Length) and Addressing Mode must be set in the Mode Register at power-up.

When the Write with Auto Precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other command for the entire burst data duration. Also, when the Burst Length is 1 and t_{RCD} (min), the timing from the $\overline{RAS}$ command to the start of the Auto Precharge operation is shorter than t_{RAS} (min). In this case, t_{RAS} (min) must be satisfied by extending t_{RCD} (Figure 10, 16).

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated (Figure 20).

When the Burst Length is full-page, the input data is repeatedly latched until the Burst Stop command or the Precharge command is issued.

When the Burst Read and Single Write mode is selected, the write burst length is 1 regardless of the read burst length.

4. Precharge

There are two commands which perform the Precharge operation: Bank Precharge and Precharge All. When the Bank Precharge command is issued to the active bank, the bank is precharged and then switched to the idle state. The Bank Precharge command can precharge one bank independently of the other bank and hold the unprecharged bank in the active state. The maximum time each bank can be held in the active state is specified as t_{RAS} (max). Therefore, each bank must be precharged within t_{RAS} (max) from the Bank Activate command.

The Precharge All command can be used to precharge all banks simultaneously. Even if banks are not in the active state, the Precharge All command can still be issued. In this case, the Precharge operation is performed only for the active bank and the precharged bank is then switched to the idle state.

5. Page Mode

The Read or Write command can be issued on any clock cycle.

Whenever a Read operation is to be interrupted by a Write command, the output data must be masked by DQM to avoid I/O conflict. Also, when a Write operation is to be interrupted by a Read command, only the input data before the Read command is enable and the input data after the Read command is disabled.

6. Burst Termination

When the Precharge command is issued for a bank in a Burst cycle, the Burst operation is terminated. When the Burst Read cycle is interrupted by the Precharge command, read operation is disabled after clock cycle of ($\overline{CAS}$ latency-1) from the Precharge command (Figure 20). When the Burst Write cycle is interrupted by the Precharge command, the input circuit is reset at the same clock cycle at which the Precharge command is issued. In this case, the DQM signal must be asserted “High” to prevent writing the invalid data to the cell array (Figure 20).

When the Burst Stop command is issued for the bank in a Full-page Burst cycle, the Burst operation is terminated. When the Burst Stop command is issued during Full-page Burst Read cycle, read operation is disabled after clock cycle of ($\overline{CAS}$ latency-1) from the Burst Stop command. When the Burst Stop command is issued during a Full-page Burst Write cycle, write operation is disabled at the same clock cycle at which the Burst Stop command is issued. (Figure 19)

7. Mode Register Operation

The Mode register designates the operation mode for the Read or Write cycle. This register is divided into three fields; A Burst Length field to set the length of burst data, an Addressing Mode selected bits to designate the column access sequence in a Burst cycle, and a $\overline{CAS}$ latency field to set the access time in clock cycle.

The Mode Register is programmed by the Mode Register Set command when all banks are in the idle state. The data to be set in the Mode Register is transferred using the A0~A12, BS0, BS1 address inputs. The initial value of the Mode Register after power-up is undefined; therefore the Mode Register Set command must be issued before proper operation.

- Burst Length field (A2~A0)

  This field specifies the data length for column access using the A2~A0 pins and sets the Burst Length to be 1, 2, 4, 8, words, or full-page.

A2	A1	A0	Burst Length
0	0	0	1 word
0	0	1	2 words
0	1	0	4 words
0	1	1	8 words
1	1	1	Full-Page

- Addressing Mode Select (A3)

  The Addressing Mode can be one of two modes; Interleave mode or Sequential mode. When the A3 bit is 0, Sequential mode is selected. When the A3 bit is 1, Interleave mode is selected.
  Both Addressing modes support burst length of 1, 2, 4 and 8 words. Additionally, Sequential mode supports the full-page burst.

A3	Addressing Mode
0	Sequential
1	Interleave

- Addressing sequence of Sequential mode

  A column access is performed by incrementing the column address input to the device. The address is varied by the Burst Length as shown in Table 2.

Table 2. Addressing sequence for Sequential mode

DATA	Access Address	Burst Length
Data0	n	2 words (Address bits is A0) not carried from A0 to A1
Data1	n + 1	
Data2	n + 2	4 words (Address bits is A1, A0) not carried from A1 to A2
Data3	n + 3	
Data4	n + 4	8 words (Address bits is A2, A1, A0) not carried from A2 to A3
Data5	n + 5	
Data6	n + 6	
Data7	n + 7	

- Addressing sequence of Interleave mode

  A column access is started from the input column address and is performed by inverting the address bits in the sequence shown in Table 3.

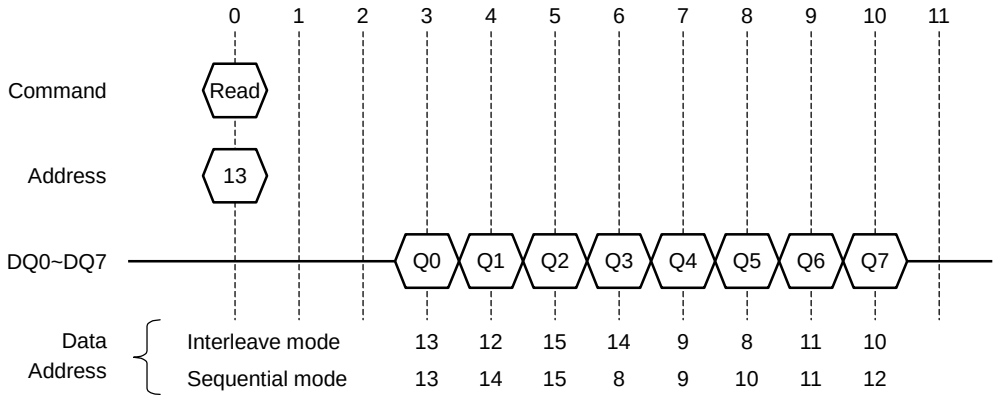
Table 3. Addressing sequence for Interleave mode

DATA	Access Address									Burst Length
Data0	A8	A7	A6	A5	A4	A3	A2	A1	A0	2 words
Data1	A8	A7	A6	A5	A4	A3	A2	A1	$\overline{A0}$	
Data2	A8	A7	A6	A5	A4	A3	A2	$\overline{A1}$	A0	4 words
Data3	A8	A7	A6	A5	A4	A3	A2	$\overline{A1}$	$\overline{A0}$	
Data4	A8	A7	A6	A5	A4	A3	$\overline{A2}$	A1	A0	8 words
Data5	A8	A7	A6	A5	A4	A3	$\overline{A2}$	A1	$\overline{A0}$	
Data6	A8	A7	A6	A5	A4	A3	$\overline{A2}$	$\overline{A1}$	A0	
Data7	A8	A7	A6	A5	A4	A3	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	

Addressing sequence example (Burst Length = 8 and input address is 13.)

DATA	Interleave Mode										Sequential Mode		
	A8	A7	A6	A5	A4	A3	A2	A1	A0	ADD		ADD	
Data0	0	0	0	0	0	1	1	0	1	13	13	13	
Data1	0	0	0	0	0	1	1	0	0	12	13 + 1	14	
Data2	0	0	0	0	0	1	1	1	1	15	13 + 2	15	calculated using A2, A1 and A0 bits
Data3	0	0	0	0	0	1	1	1	0	14	13 + 3	8	not carry from A2 to A3 bit.
Data4	0	0	0	0	0	1	0	0	1	9	13 + 4	9	
Data5	0	0	0	0	0	1	0	0	0	8	13 + 5	10	
Data6	0	0	0	0	0	1	0	1	1	11	13 + 6	11	
Data7	0	0	0	0	0	1	0	1	0	10	13 + 7	12	

Read Cycle $\overline{CAS}$ Latency = 3



- $\overline{CAS}$ Latency field (A6~A4)

  This field specifies the number of clock cycles from the assertion of the Read command to the first data read. The minimum values of $\overline{CAS}$ Latency depends on the frequency of CLK. The minimum value which satisfies the following formula must be set in this field.

A6	A5	A4	$\overline{CAS}$ Latency
0	1	0	2 clock
0	1	1	3 clock

- Test mode entry bit (A7)

  This bit is used to enter Test mode and must be set to 0 for normal operation.

- Reserved bits (A8, A10, A11, A12, BS0, BS1)

  These bits are reserved for future operations. They must be set to 0 for normal operation.

- Single Write mode (A9)

  This bit is used to select the write mode. When the A9 bit is 0, Burst Read and Burst Write mode are selected. When the A9 bit is 1, Burst Read and Single Write mode are selected.

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

8. Refresh Operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before- $\overline{RAS}$ refresh of conventional DRAMs and is performed by issuing the Auto Refresh command while all banks are in the idle state. By repeating the Auto Refresh cycle, all banks refreshed automatically. The Refresh operation must be performed 8192 times (rows) within 64 ms (Figure 11). The period between the Auto Refresh command and the next command is specified by t_{RC}.

Self Refresh mode is entered by issuing the Self Refresh command (CKE asserted "low") while all banks are in the idle state. The device is in Self Refresh mode for as long as CKE is held "low". In Self Refresh mode, all input/output buffers (except the CKE buffer) are disabled to lower power dissipation (Figure 12).

In the case of 8192 burst Auto Refresh commands, 8192 burst Auto Refresh commands must be performed within 7.8 μs before entering and after exiting the Self Refresh mode.

In the case of distributed Auto Refresh commands, distributed Auto Refresh commands must be issued every 7.8 μs or faster and the last distributed Auto Refresh command must be performed within 7.8 μs before entering the Self Refresh mode. After exiting from the Self Refresh mode, the refresh operation must be performed within 7.8 μs.

9. Power Down Mode

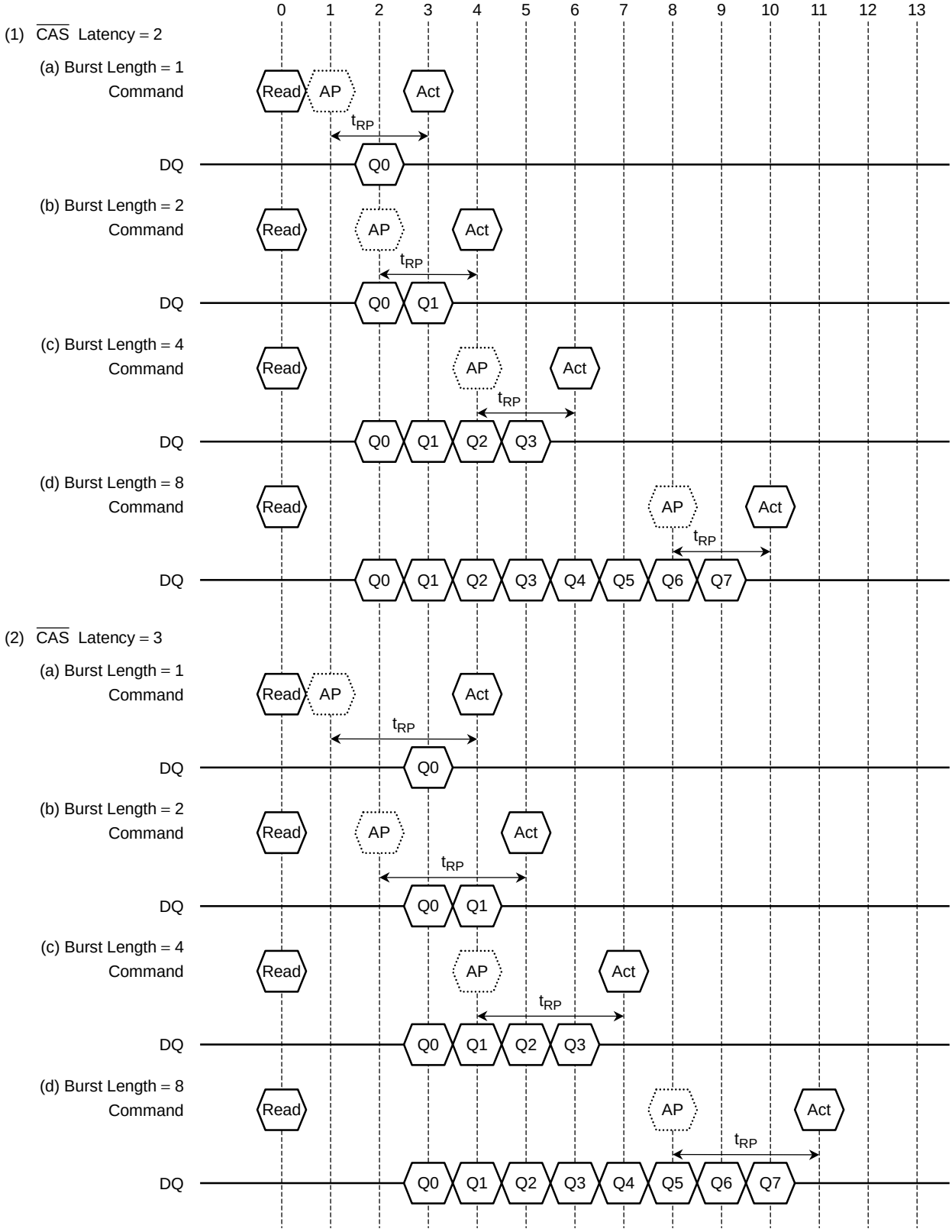
When the device enters the Power Down mode, all input/output buffers (except CKE buffer) are disabled to lower power dissipation in the idle state. Power Down mode is entered by asserting CKE "low" while the device is not running a Burst cycle. Taking CKE "high" exit this mode. When CKE goes high, a No-operation command must be input at next CLK rising edge of CLK (Figure 13) and CKE should be set high at least 1CLK + t_{CKS} at Power Down Mode Exit.

10. CLK suspension and Input/Output Mask

When the device is running a Burst cycle, the internal CLK is suspended by asserting CKE "low" the burst operation is frozen from the next cycle. A Read/Write operation is held intact until the CKE signal is taken "high".

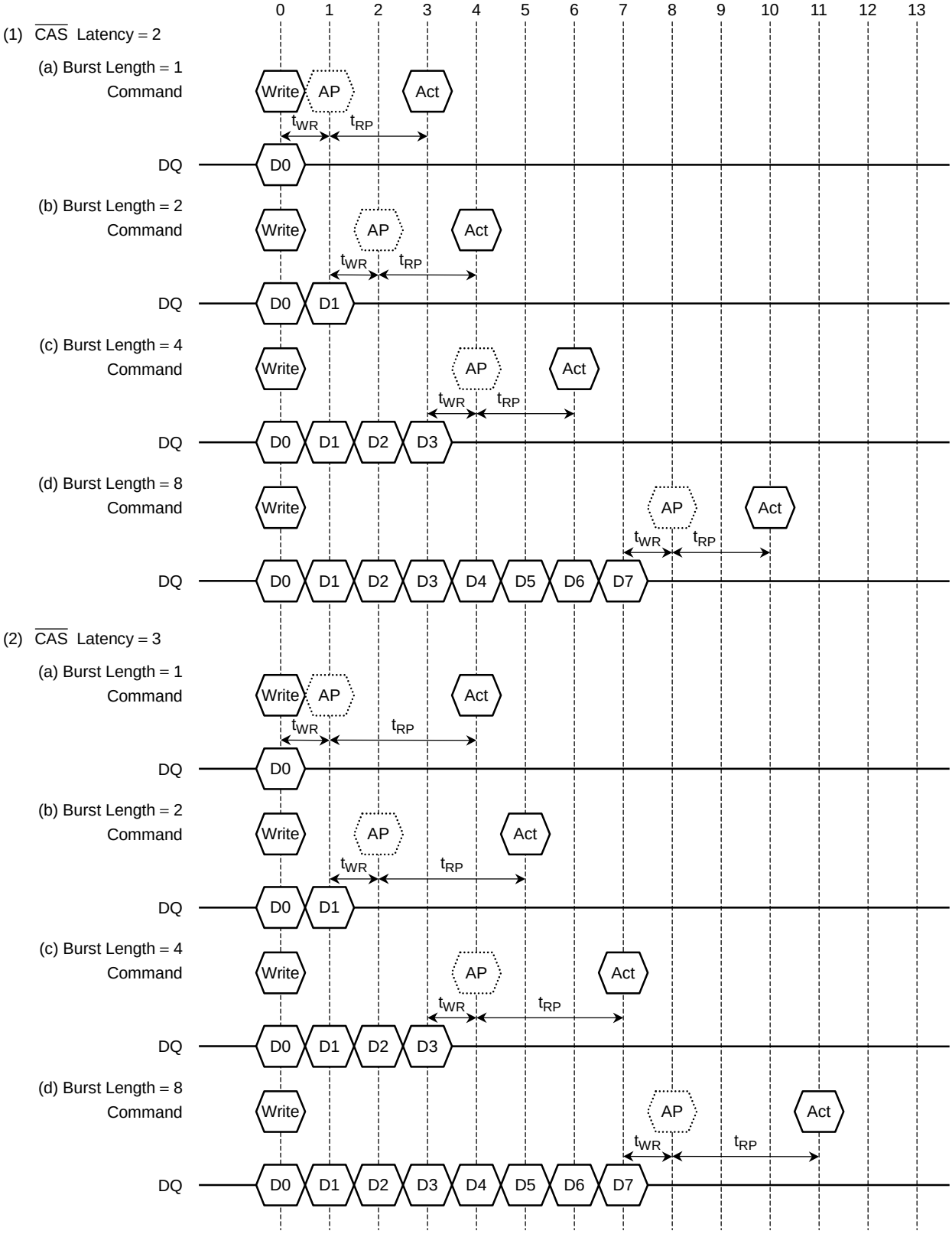
The Output Disable/Write Mask signal (DQM) has two functions, controlling the output data in a Read cycle and performing word mask in a Write cycle. When the DQM is asserted "high" at the positive edge of CLK, the output data is disabled after two clock cycles in the case of a Read operation and the write data is masked at the same clock cycle in the case of a Write operation. The timing relations between the CKE timing and DQM are described in Figure 21 (a) and 21 (b).

Figure 15. Auto Precharge timing (Read cycle)



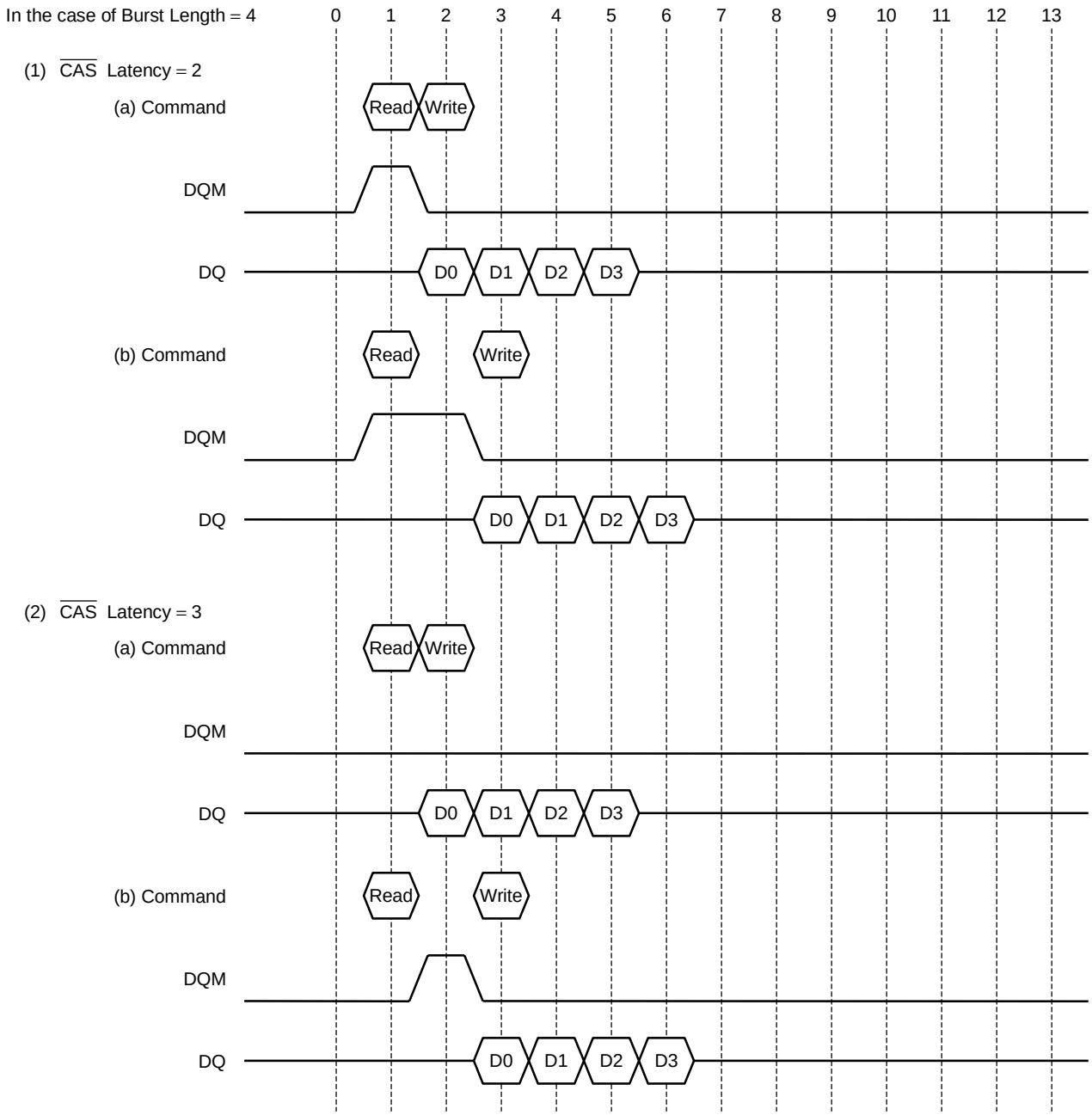
Note)
- Read represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from the Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure 16. Auto Precharge timing (Write cycle)



Note)
- Write represents the Write with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from the Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure 17. Timing chart for Read-to-Write cycle



Note) • The output data must be masked by DQM to avoid I/O conflict.

Figure 18. Timing chart for Write-to-Read cycle

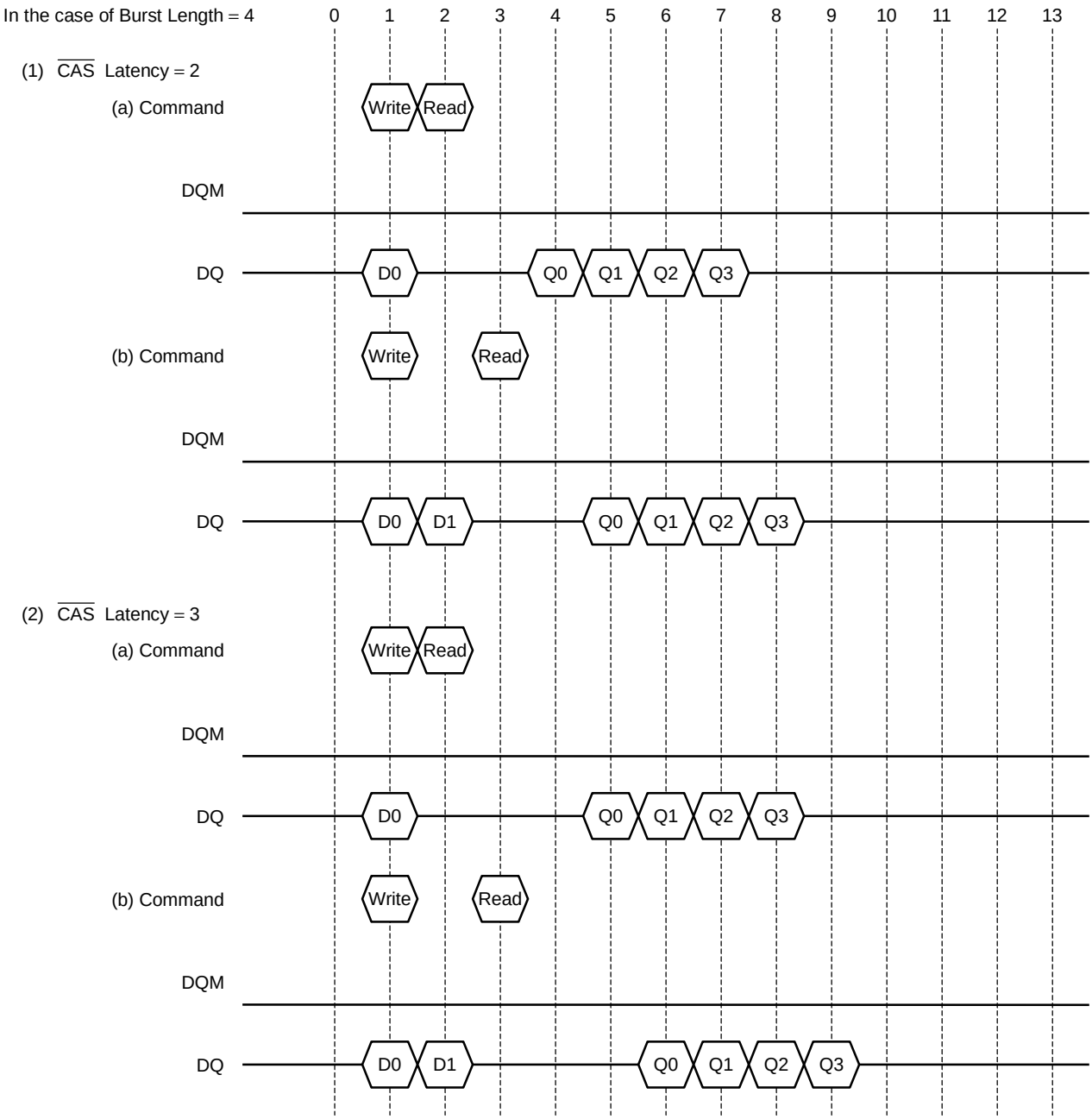
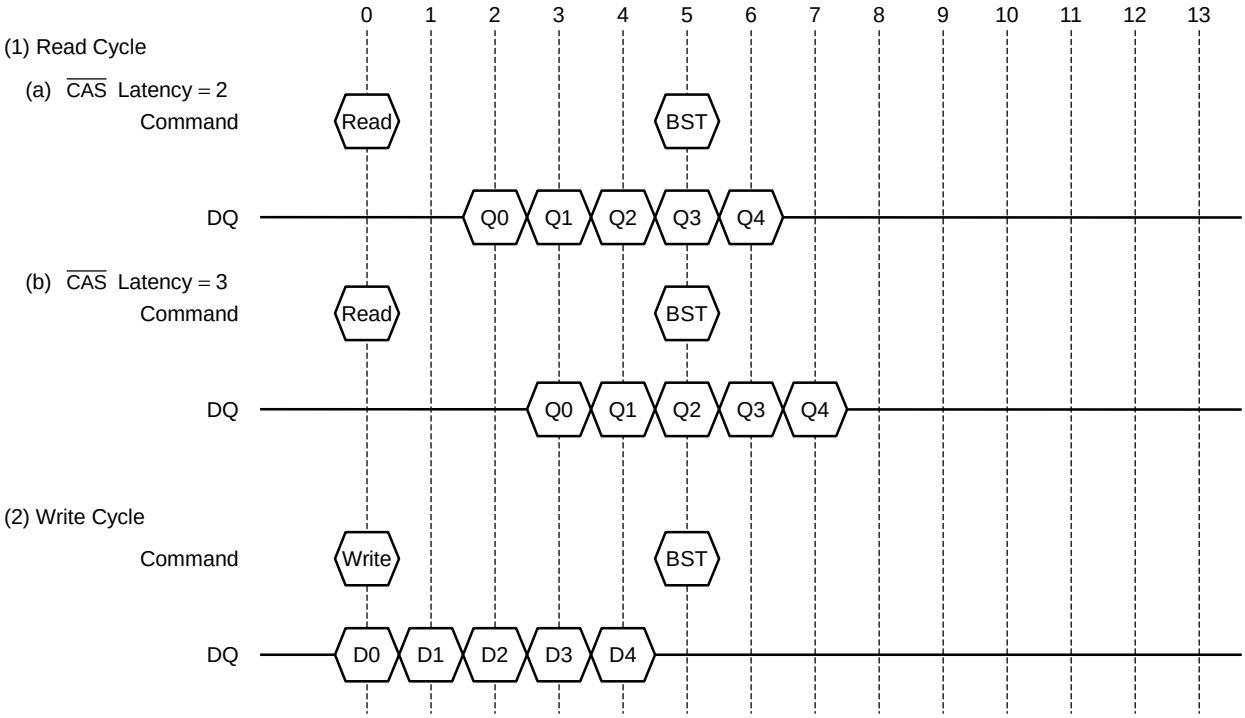
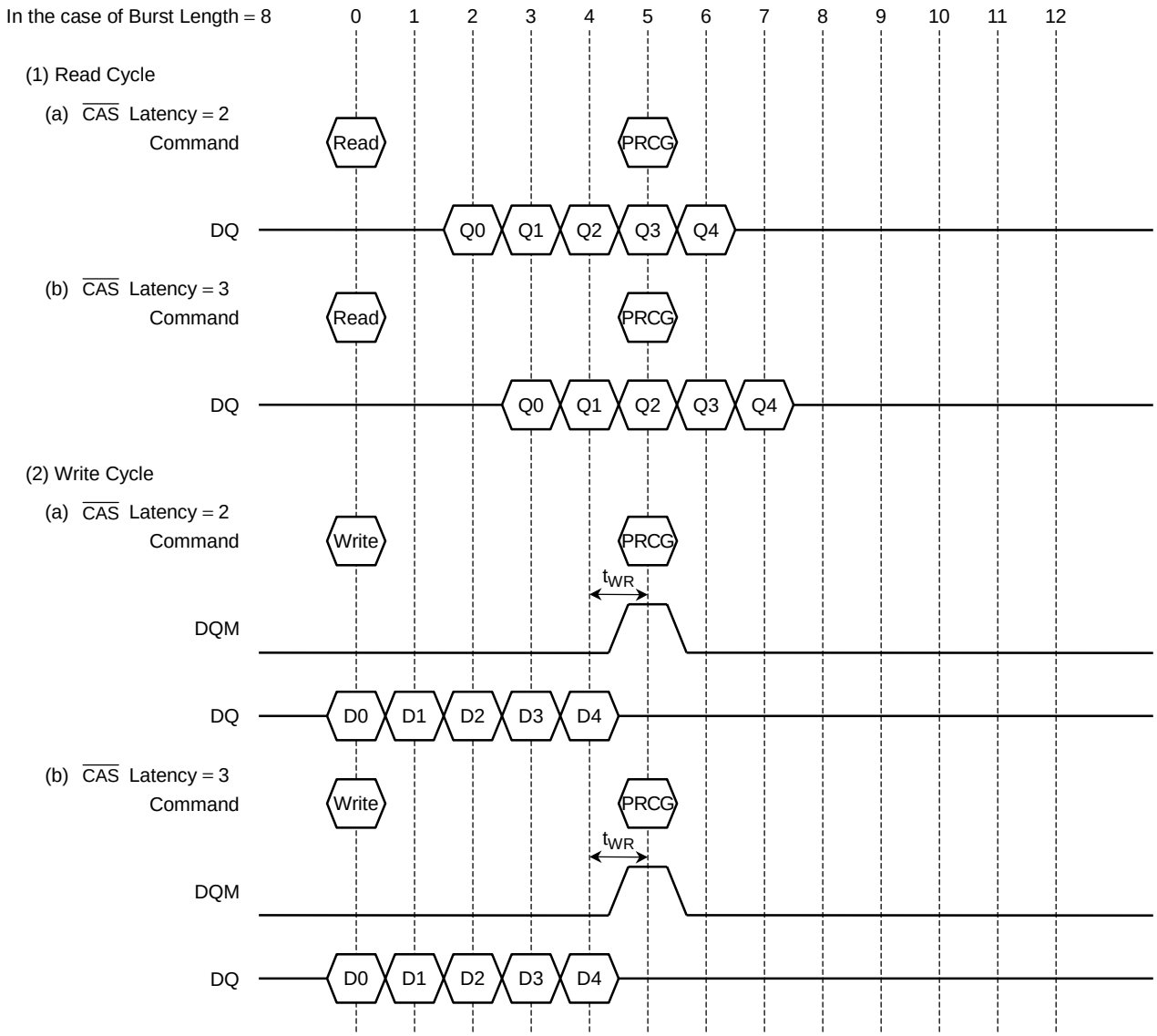


Figure 19. Timing chart for Burst Stop cycle (Burst stop command)



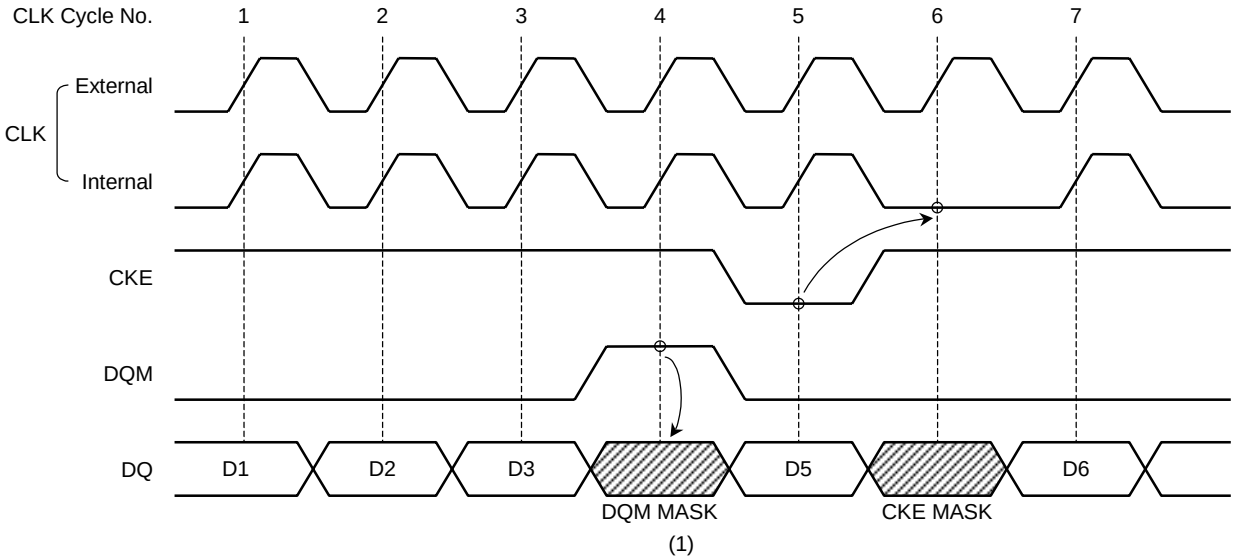
Note) • BST represents the Burst stop command.

Figure 20. Timing chart for Burst Stop cycle (Precharge command)

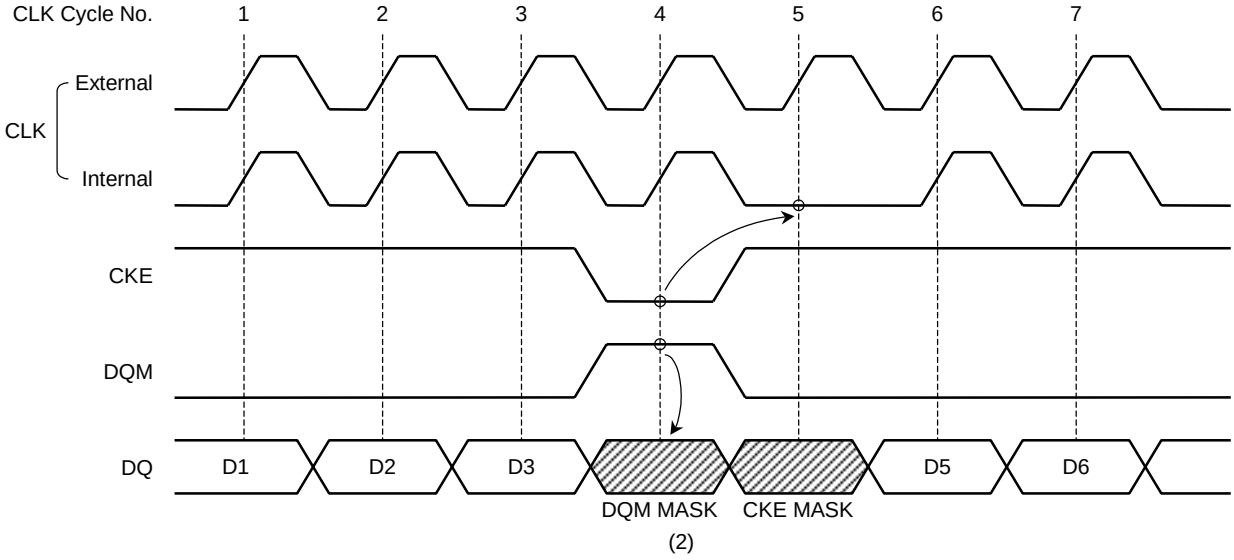


Note) • PRCG represents the Precharge command.

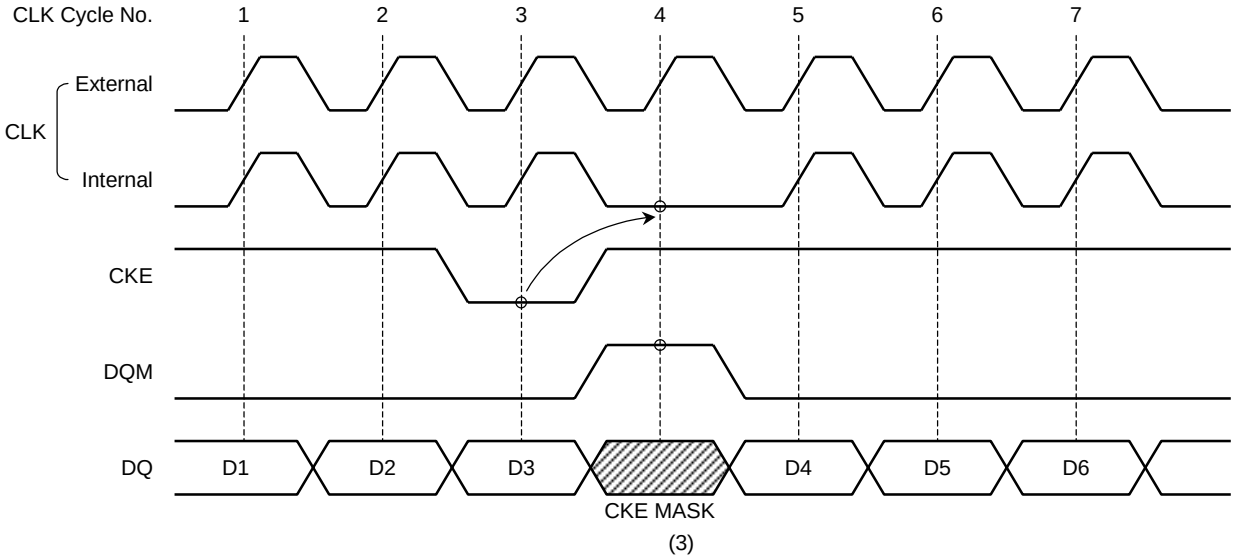
Figure 21 (a). CKE/DQM Input timing (Write cycle)



(1)

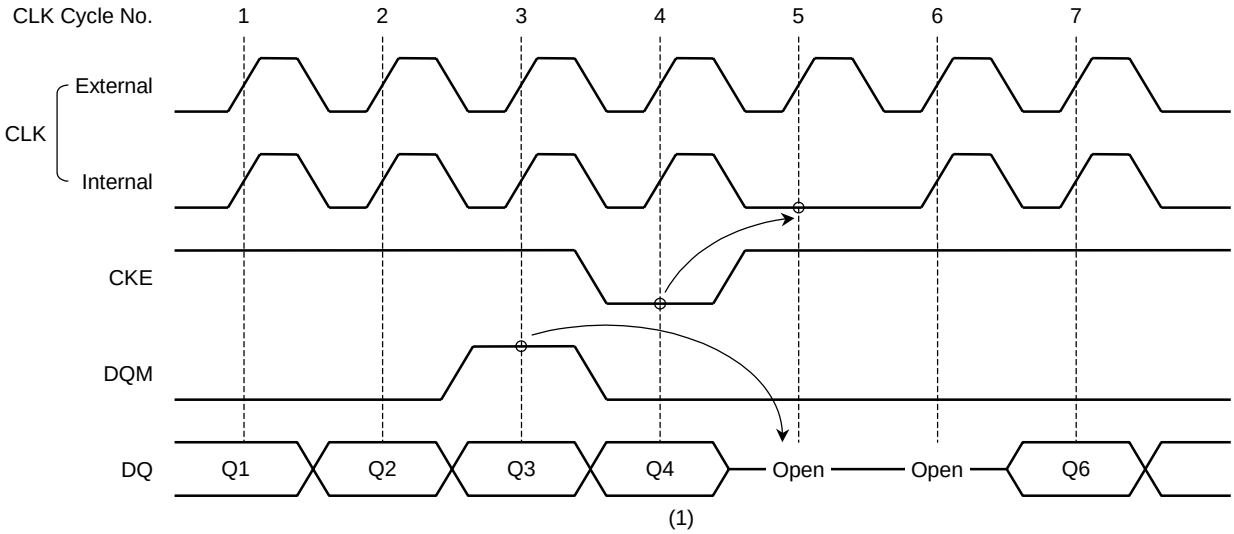


(2)

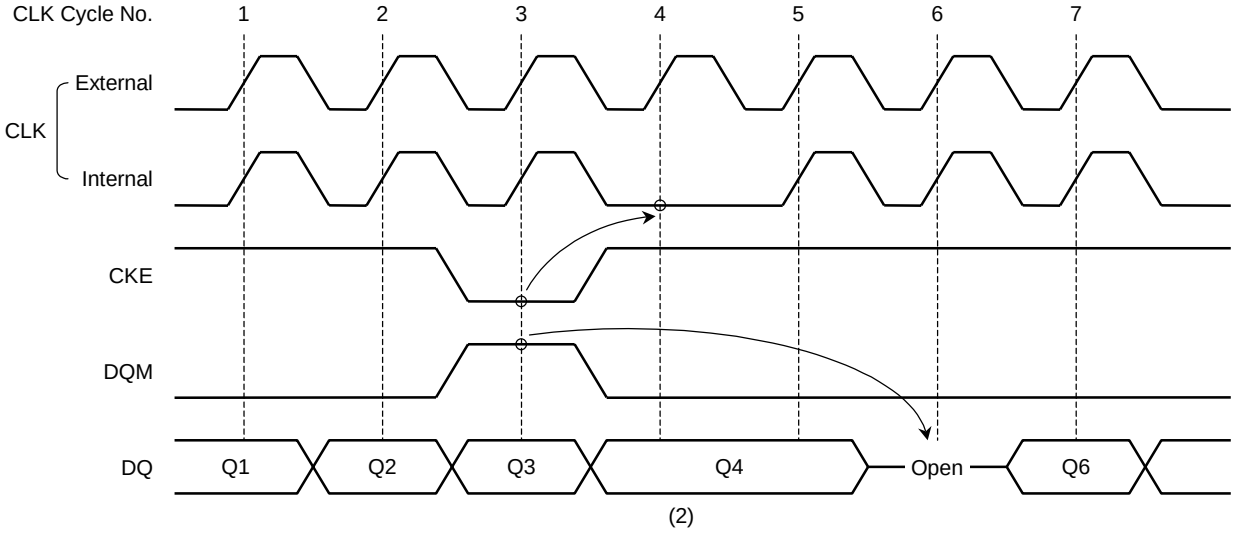


(3)

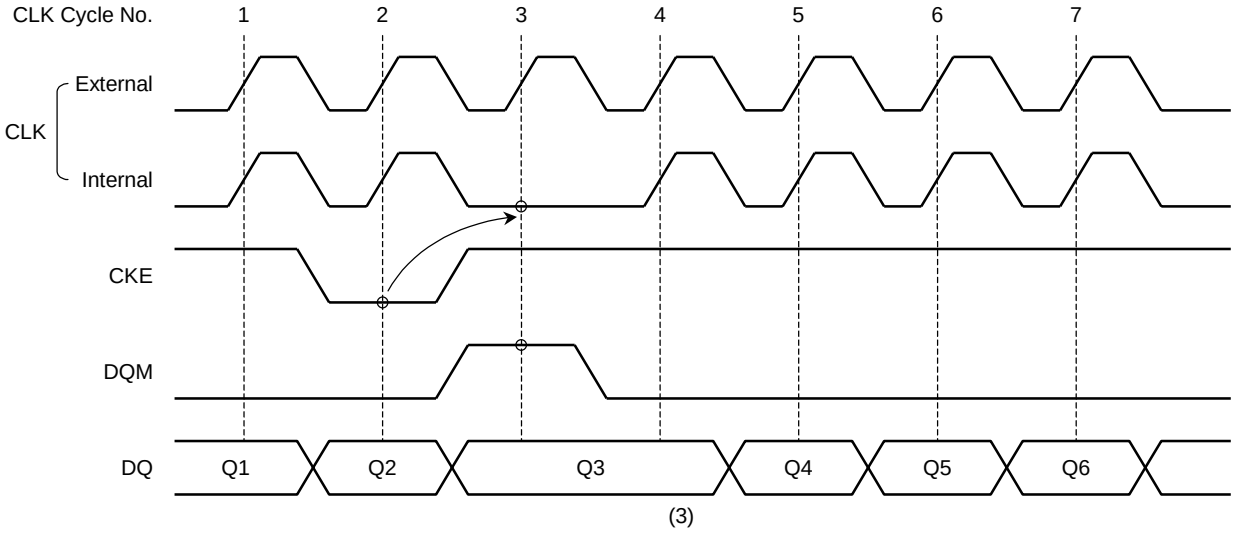
Figure 21 (b). CKE/DQM Input timing (Read cycle)



(1)



(2)



(3)

PACKAGE DIMENSIONS

Unit: mm

P-TFBGA60-0816-0.80AZ