NCP4681, NCP4684

150 mA, Ultra Low Quiescent Current, Low Dropout Regulator

The NCP4681 and NCP4684 are CMOS Linear voltage regulators with 150 mA output current capability and ultra low supply currents (1 μA typ.) The devices are easy to use and include output current protection and a fully integrated soft−start circuit to minimize inrush current and to ensure no output voltage overshoot. The NCP4681 includes an Enable function to reduce supply current by using a Standby mode, while the NCP4684 excludes the Enable pin to avoid any pull down current, thereby offering the lowest possible current consumption for battery powered applications in Active mode. For portable products the devices are available in the exceptionally small 0.8 x 0.8 mm XDFN, along with the SC−70 and SOT23 packages

Features

- Operating Input Voltage Range: 1.40 V to 5.25 V
- Output Voltage Range: 0.8 V to 3.6 V (available in 0.1 V steps)
- Output Voltage Accuracy: ±1.0%
- Supply Current: 1 μA (excluding the CE pull down current)
- Dropout Voltage: 0.28 V (I_{OUT} = 150 mA, V_{OUT} = 2.8 V)
- Line Regulation: 0.02%/V Typ.
- Stable with Ceramic Capacitors: 0.1 μF or more
- Current Fold Back Protection
- Build−in Constant Slope Circuit for soft−start function
- Available in XDFN4 0.8 x 0.8 mm, SC−70, SOT23 Packages
- These are Pb−Free Devices

Typical Applications

- Battery−powered Equipment
- Networking and Communication Equipment
- Cameras, DVRs, STB and Camcorders
- Home Appliances

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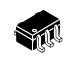
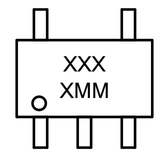
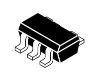
MARKING DIAGRAMS

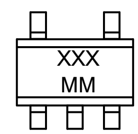


SC−70
CASE 419A

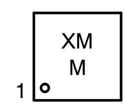




SOT−23−5
CASE 1212



1
XDFN4
CASE 711AB



X, XXXX = Specific Device Code
MM = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

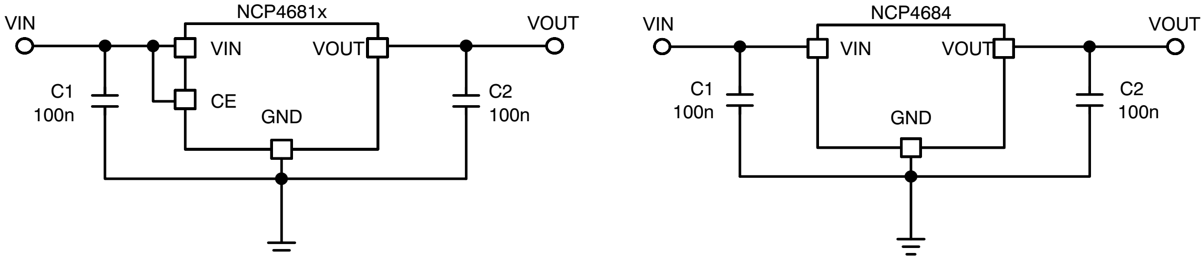


Figure 1. Typical Application Schematics

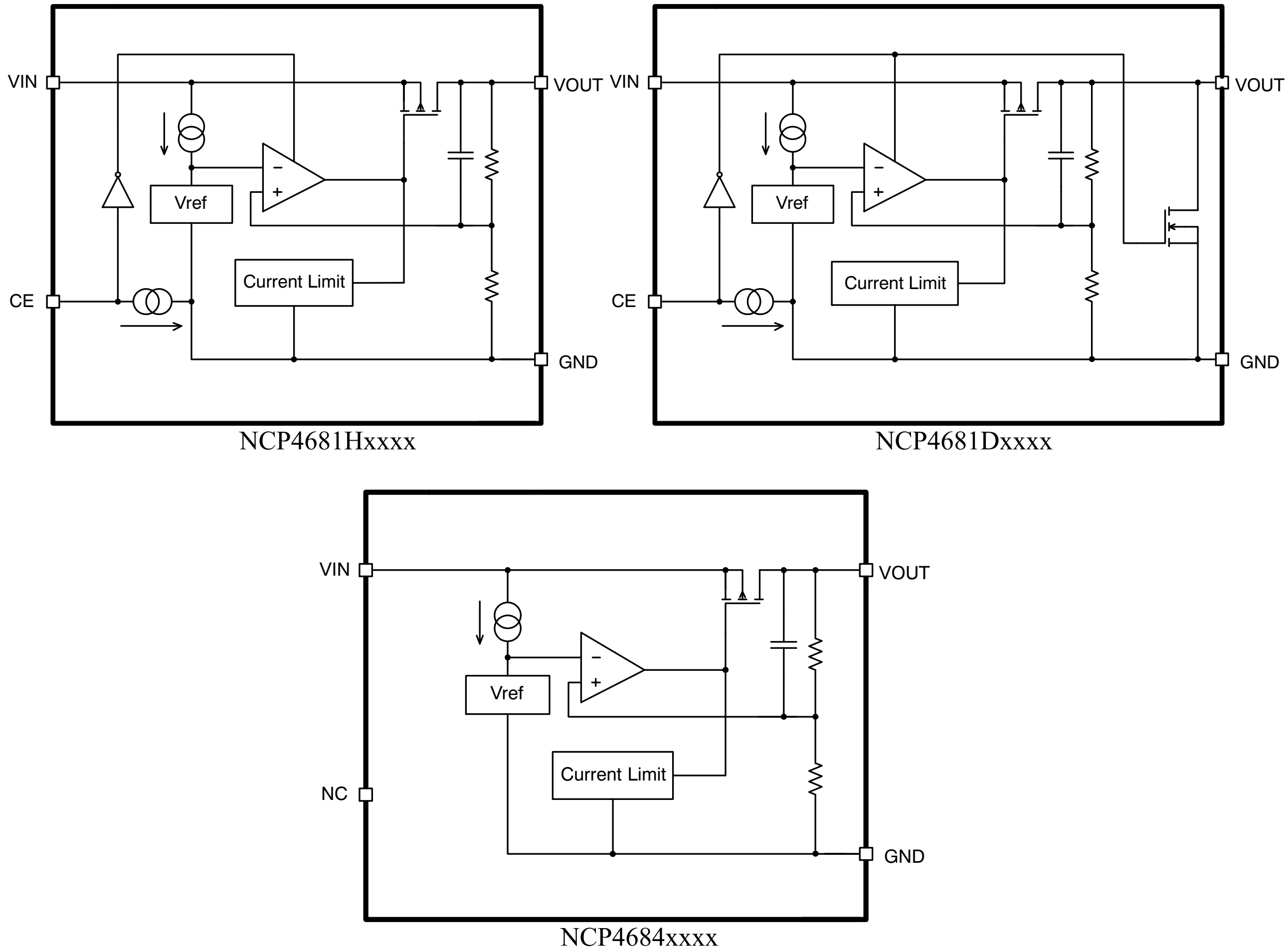


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. XDFN0808*	Pin No. SC−70	Pin No. SOT23	Pin Name	Description
1	4	5	V_{OUT}	Output pin
2	3	2	GND	Ground
3	1	3	CE/NC	Chip enable pin (Active “H”) / No connection (NCP4684)
4	5	1	V_{IN}	Input pin
–	2	4	NC	No connection

*Tab is GND level. (They are connected to the reverse side of this IC.
The tab is better to be connected to the GND, but leaving it open is also acceptable.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	6.0	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	6.0	V
Output Current	I_{OUT}	180	mA
Power Dissipation XDFN0808	P_D	286	mW
Power Dissipation SC−70		380	
Power Dissipation SOT23		420	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latch−up Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN 0.8 x 0.8 mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	350	°C/W
Thermal Characteristics, SOT23 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, SC−70 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	263	°C/W

ELECTRICAL CHARACTERISTICS

−40°C ≤ T_A ≤ 85°C; V_{IN} = $V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0.1 μF, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage	(Note 3)		V_{IN}	1.40		5.25	V
Output Voltage	T_A = +25°C	V_{OUT} ≥ 2.0 V	V_{OUT}	x0.99		x1.01	V
		V_{OUT} < 2.0 V		−20		20	mV
	−40°C ≤ T_A ≤ 85°C	V_{OUT} ≥ 2.0 V		x0.970		x1.025	V
		V_{OUT} < 2.0 V		−60		60	mV
Output Voltage Temp. Coefficient	−40°C ≤ T_A ≤ 85°C		$\Delta V_{OUT}/\Delta T_A$		±100		ppm/°C
Line Regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.0 V		$Line_{Reg}$		0.02	0.10	%/V
Load Regulation	IOUT = 1 mA to 150 mA		$Load_{Reg}$	−20	0	20	mV
Dropout Voltage	I_{OUT} = 150 mA	0.8 V ≤ V_{OUT} < 0.9 V	V_{DO}		0.96	1.40	V
		0.9 V ≤ V_{OUT} < 1.0 V			0.87	1.25	
		1.0 V ≤ V_{OUT} < 1.2 V			0.78	1.15	
		1.2 V ≤ V_{OUT} < 1.4 V			0.64	1.00	
		1.4 V ≤ V_{OUT} < 1.7 V			0.52	0.80	
		1.7 V ≤ V_{OUT} < 2.0 V			0.40	0.60	
		2.0 V ≤ V_{OUT} < 2.5 V			0.32	0.48	
		2.5 V ≤ V_{OUT} < 3.0 V			0.28	0.40	
		3.0 V ≤ V_{OUT} < 3.6 V			0.25	0.35	
Output Current			I_{OUT}	150			mA
Short Current Limit	V_{OUT} = 0 V		I_{SC}		50		mA
Quiescent Current			I_Q		1	2	μA
Standby Current	V_{CE} = 0 V, T_A = 25°C, NCP4681 only		I_{STB}		0.1	1.0	μA
CE Pin Threshold Voltage (NCP4681 only)	CE Input Voltage "H"		V_{CEH}	1.0			V
	CE Input Voltage "L"		V_{CEL}			0.4	
CE Pull Down Current	NCP4681 only		I_{CEPD}		0.3		μA
Power Supply Rejection Ratio	V_{OUT} = 1.5 V, V_{IN} = 2.5 V, ΔV_{IN} = 0.2 V_{pk-pk}, I_{OUT} = 30 mA, f = 1 kHz		PSRR		25		dB
Output Noise Voltage	f = 10 Hz to 100 kHz, V_{OUT} = 1.5 V, V_{IN} = 2.5 V, I_{OUT} = 30 mA		V_N		100		μV_{rms}
Low Output Nch Tr. On Resistance	V_{IN} = 4 V, V_{CE} = 0 V, NCP4681D only		R_{LOW}		60		Ω

3. The maximum Input Voltage of the Electrical Characteristics is 5.25 V. In case of exceeding this specification, the IC must be operated n condition that the Input Voltage is up to 5.50 V and total operation time is within 500 hours.

TYPICAL CHARACTERISTICS

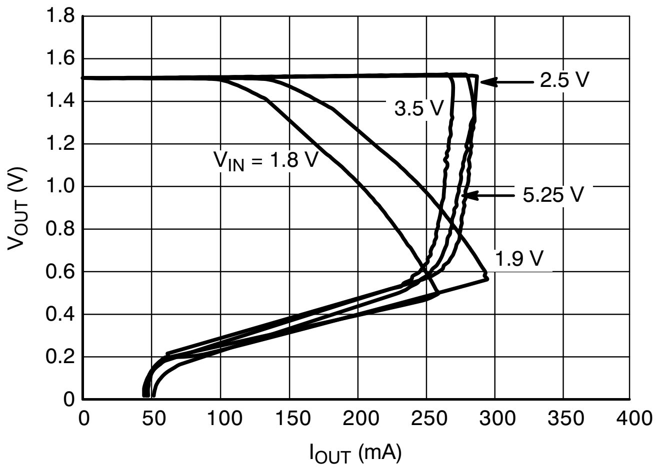


Figure 3. Output Voltage vs. Output Current 1.5 V Version (T_J = 25°C)

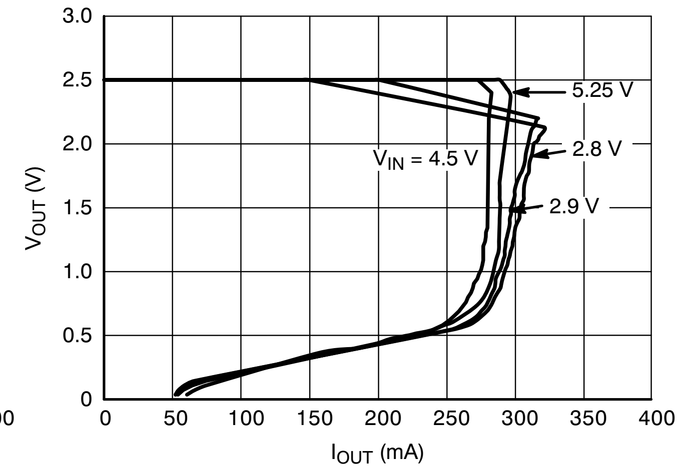


Figure 4. Output Voltage vs. Output Current 2.5 V Version (T_J = 25°C)

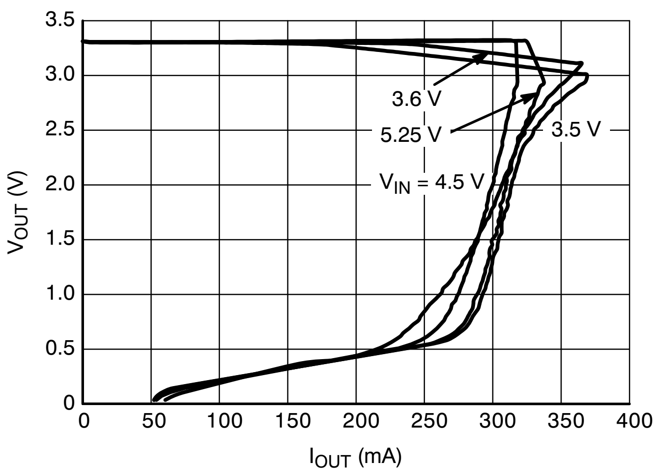


Figure 5. Output Voltage vs. Output Current 3.3 V Version (T_J = 25°C)

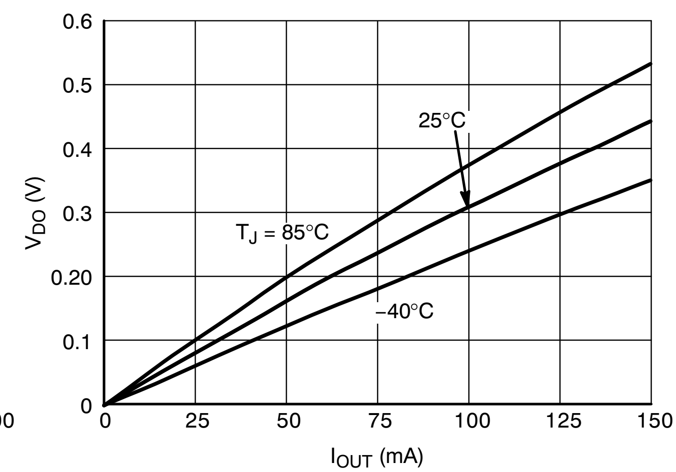


Figure 6. Dropout Voltage vs. Output Current 1.5 V Version

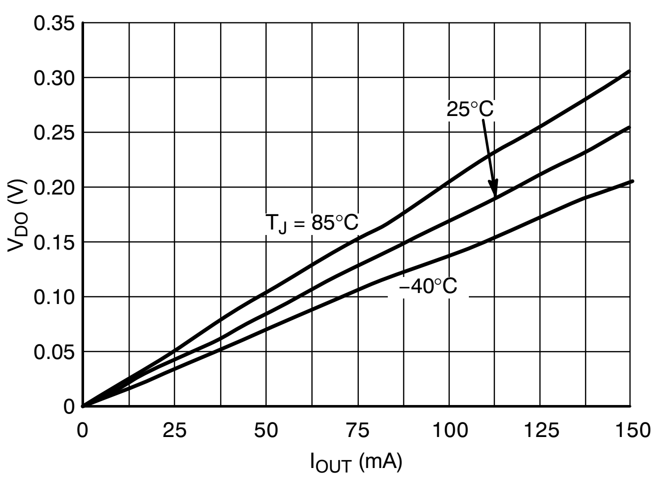


Figure 7. Dropout Voltage vs. Output Current 2.5 V Version

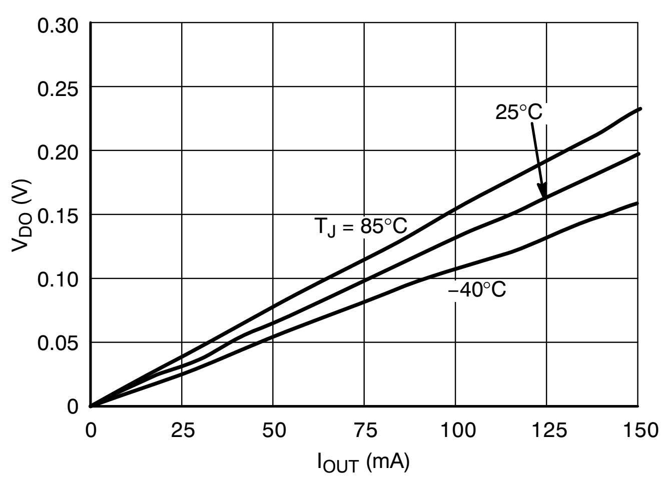


Figure 8. Dropout Voltage vs. Output Current 3.3 V Version

TYPICAL CHARACTERISTICS

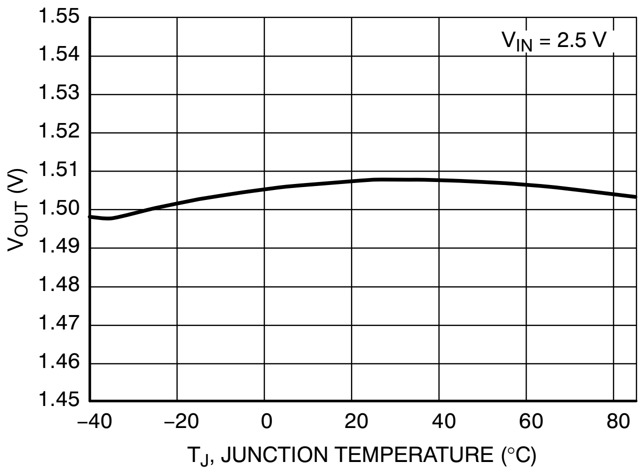


Figure 9. Output Voltage vs. Temperature, 1.5 V Version

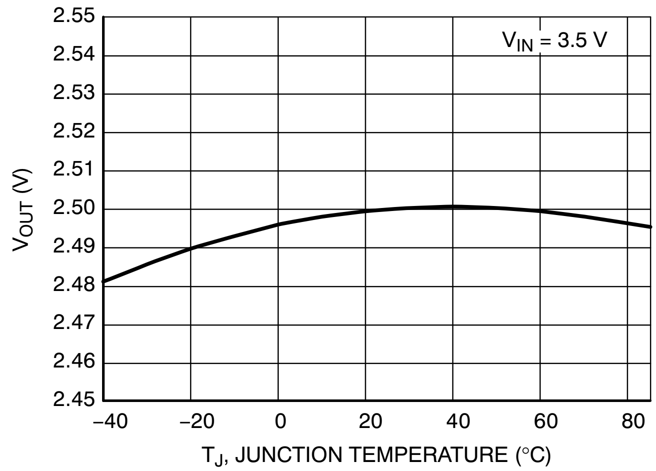


Figure 10. Output Voltage vs. Temperature, 2.5 V Version

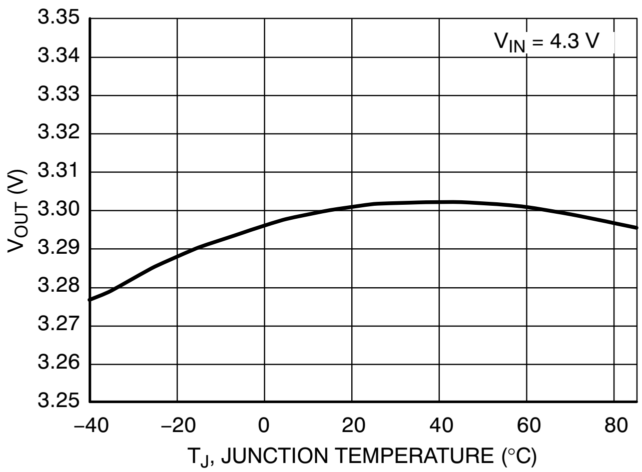


Figure 11. Output Voltage vs. Temperature, 3.3 V Version

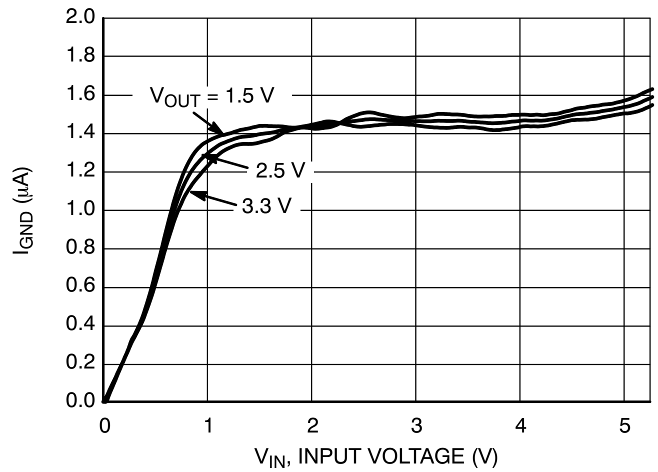


Figure 12. Supply Current vs. Input Voltage

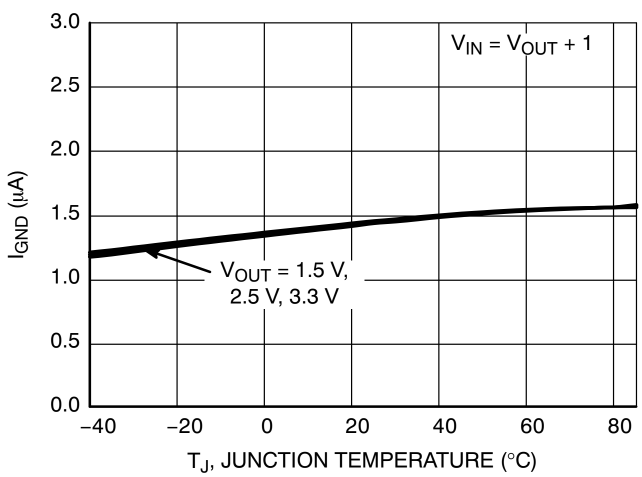


Figure 13. Supply Current vs. Temperature

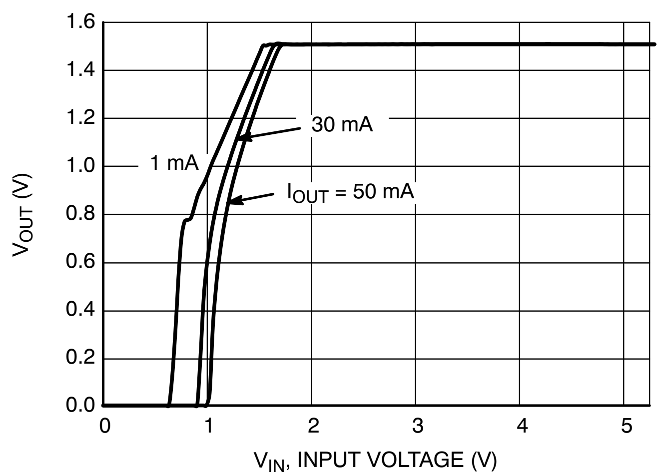


Figure 14. Output Voltage vs. Input Voltage, 1.5 V Version

TYPICAL CHARACTERISTICS

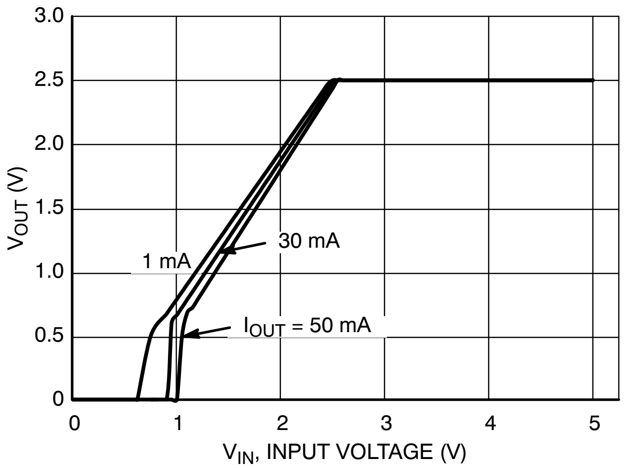


Figure 15. Output Voltage vs. Input Voltage, 2.5 V Version

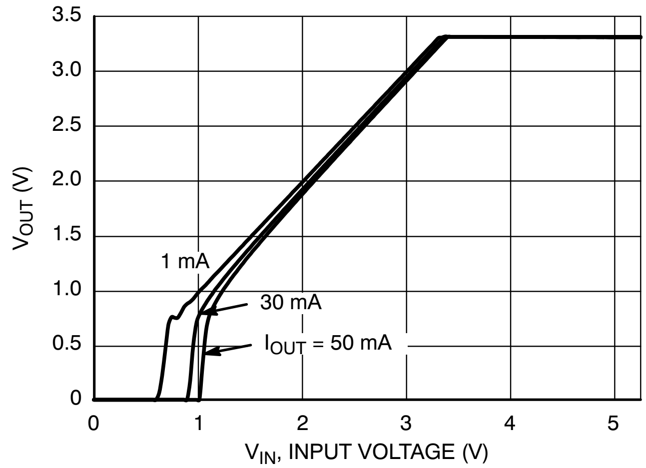


Figure 16. Output Voltage vs. Input Voltage, 3.3 V Version

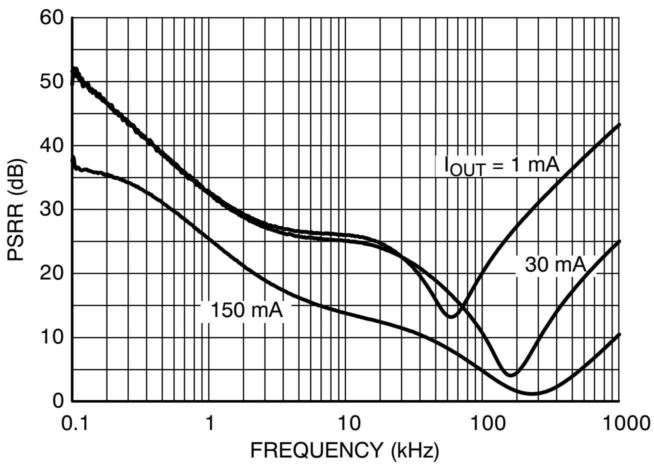


Figure 17. PSRR, 1.5 V Version, V_{IN} = 2.5 V

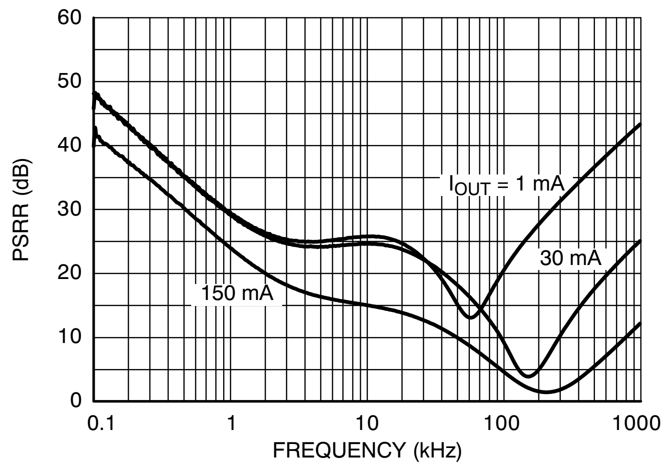


Figure 18. PSRR, 2.5 V Version, V_{IN} = 3.5 V

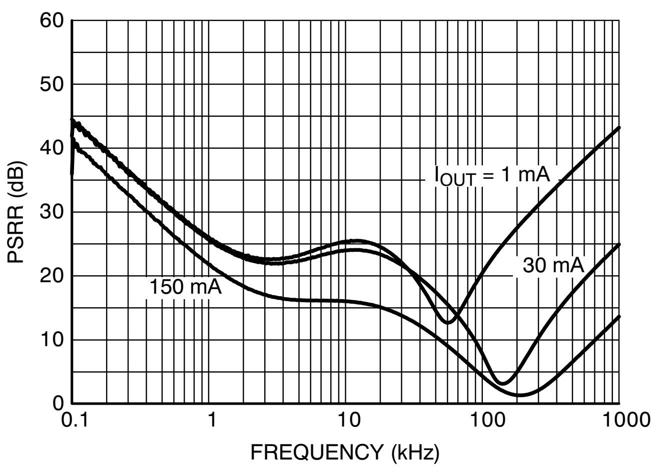


Figure 19. PSRR, 3.3 V Version, V_{IN} = 4.3 V

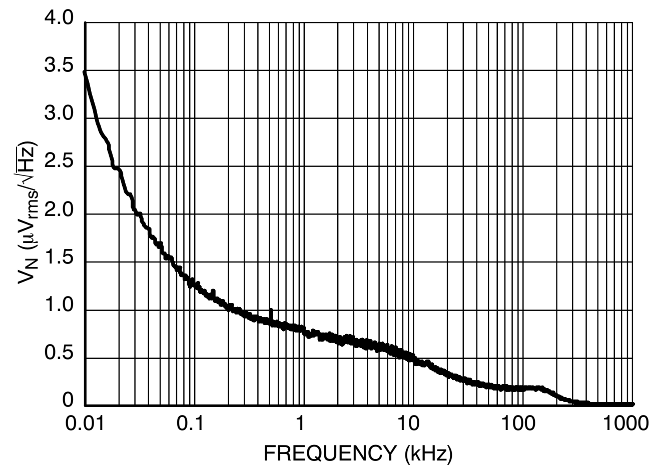


Figure 20. Output Voltage Noise, 1.5 V Version, V_{IN} = 2.5 V, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

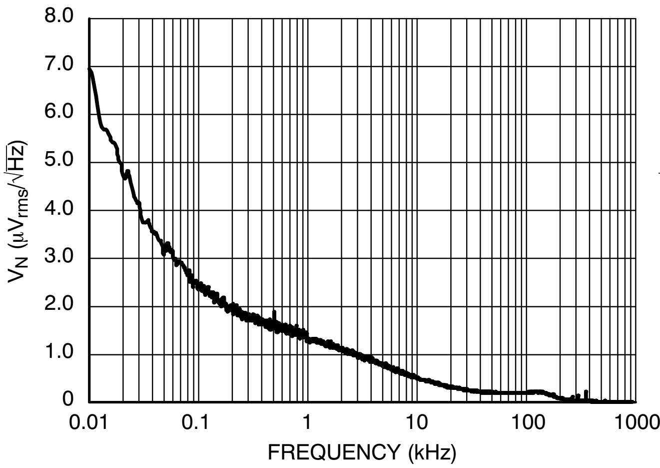


Figure 21. Output Voltage Noise, 2.5 V Version, V_{IN} = 3.5 V, I_{OUT} = 30 mA

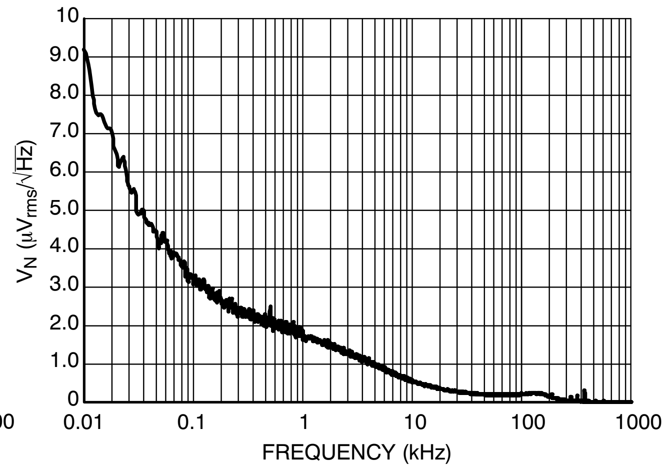


Figure 22. Output Voltage Noise, 3.3 V Version, V_{IN} = 4.3 V, I_{OUT} = 30 mA

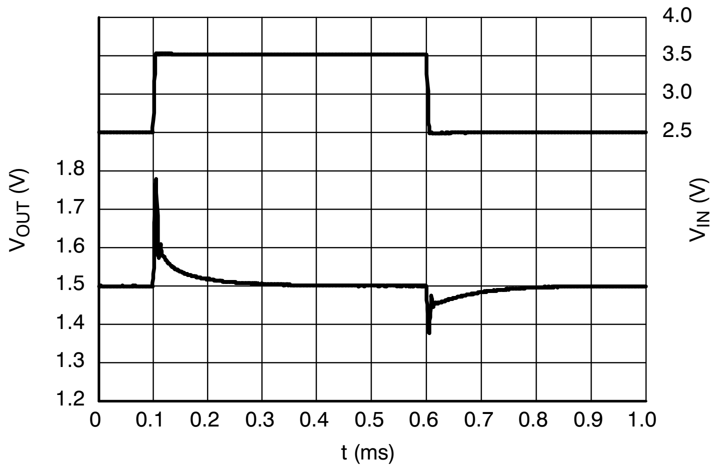


Figure 23. Line Transients, 1.5 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

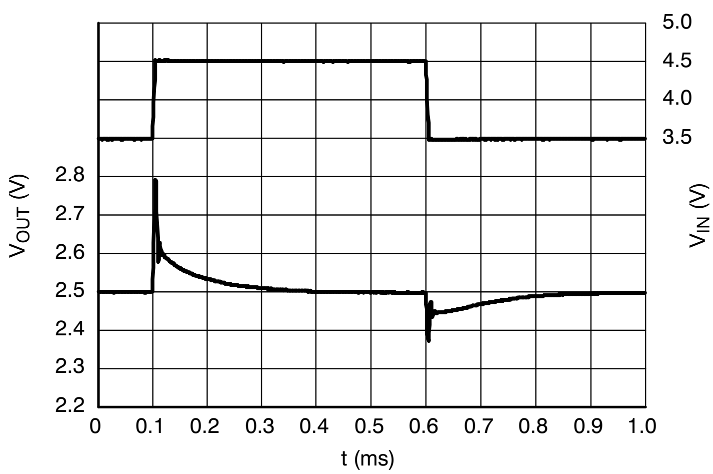


Figure 24. Line Transients, 2.5 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

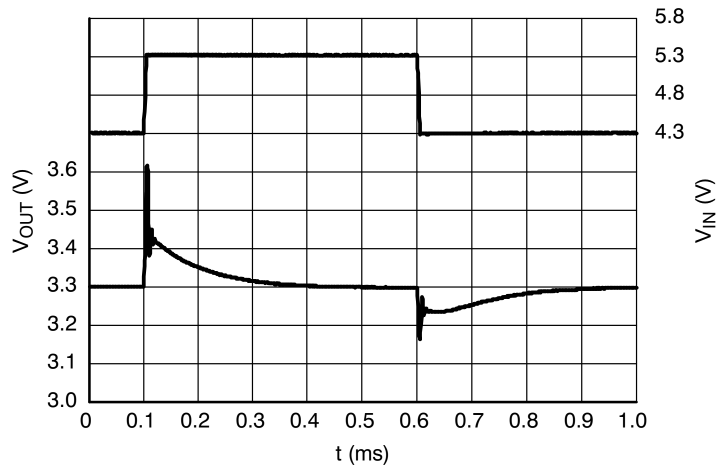


Figure 25. Line Transients, 3.3 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30$ mA

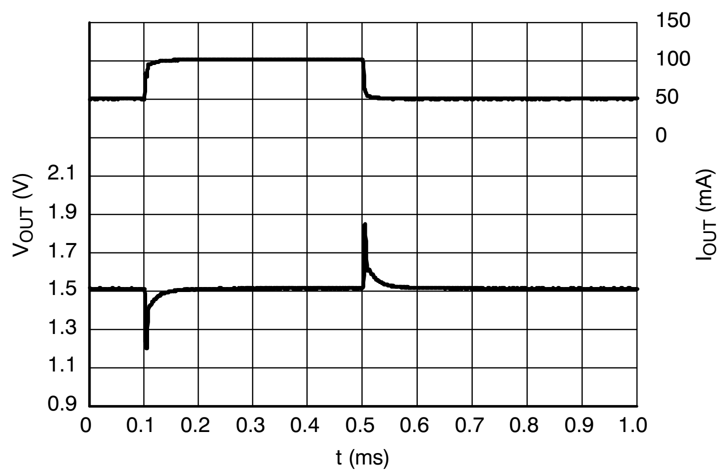


Figure 26. Load Transients, 1.5 V Version, $I_{OUT} = 50 – 100$ mA, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 2.5$ V

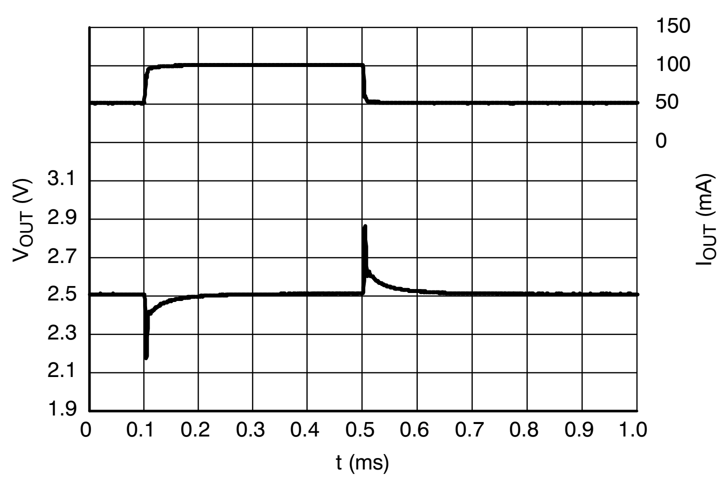


Figure 27. Load Transients, 2.5 V Version, $I_{OUT} = 50 – 100$ mA, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 3.5$ V

TYPICAL CHARACTERISTICS

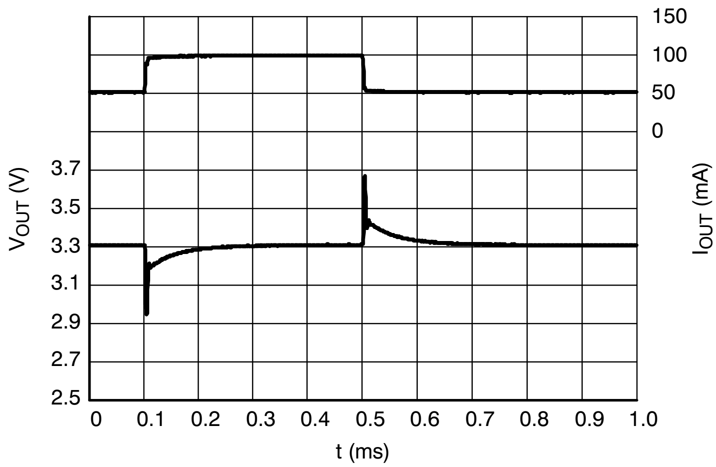


Figure 28. Load Transients, 3.3 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 4.3 V

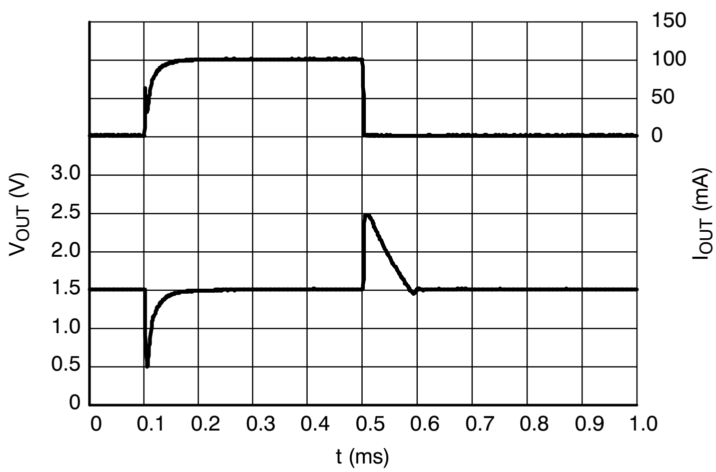


Figure 29. Load Transients, 1.5 V Version, I_{OUT} = 1 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.5 V

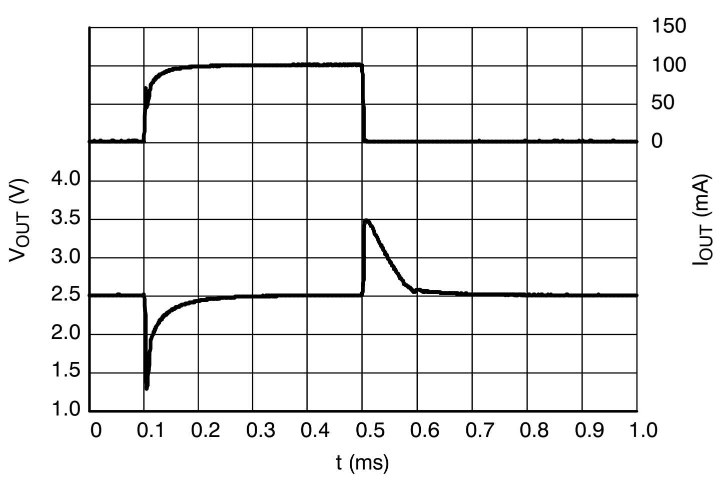


Figure 30. Load Transients, 2.5 V Version, I_{OUT} = 1 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.5 V

TYPICAL CHARACTERISTICS

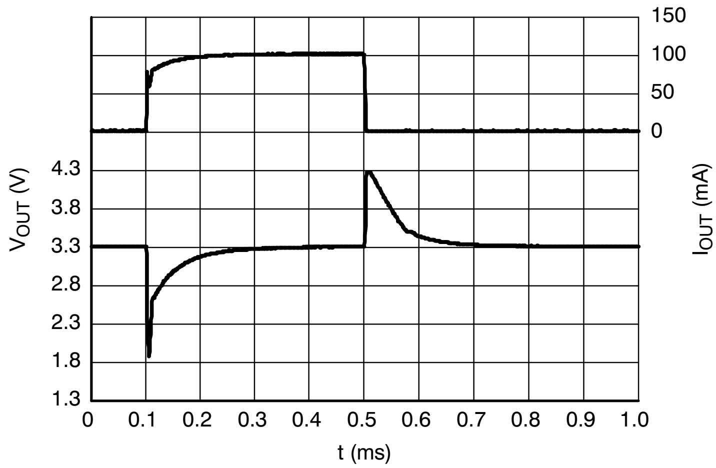


Figure 31. Load Transients, 3.3 V Version,
I_{OUT} = 1 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 4.3 V

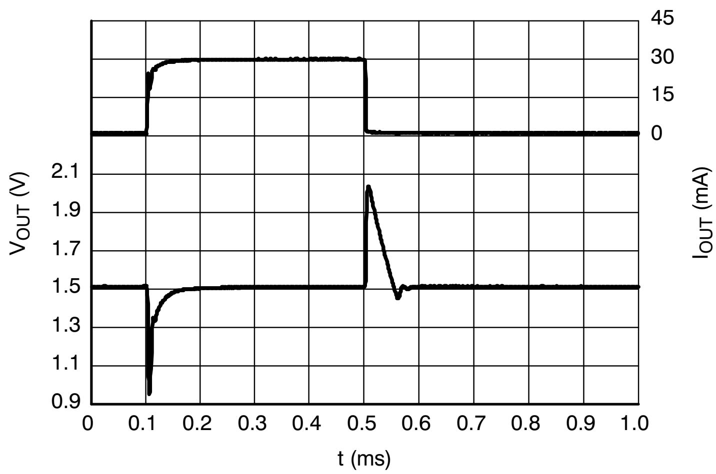


Figure 32. Load Transients, 1.5 V Version,
I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.5 V

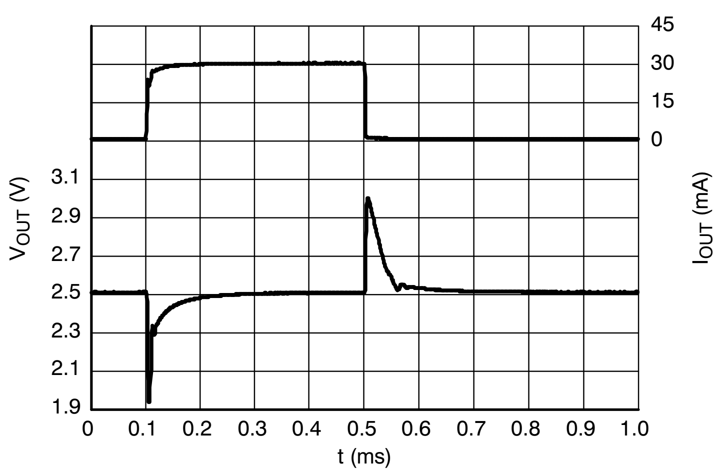


Figure 33. Load Transients, 2.5 V Version,
I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.5 V

TYPICAL CHARACTERISTICS

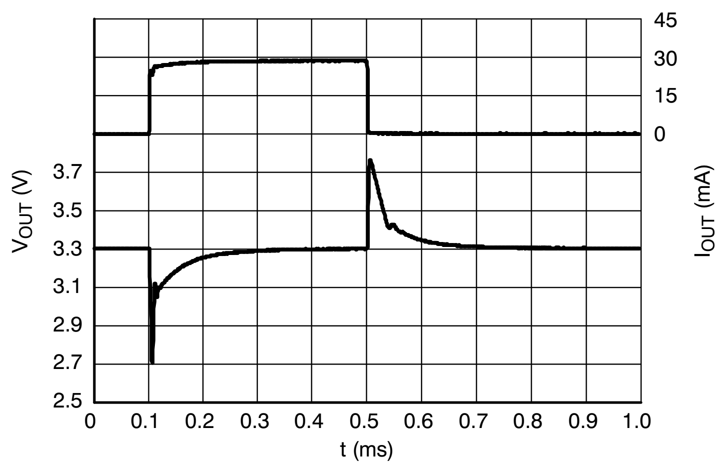


Figure 34. Load Transients, 3.3 V Version, I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 4.3 V

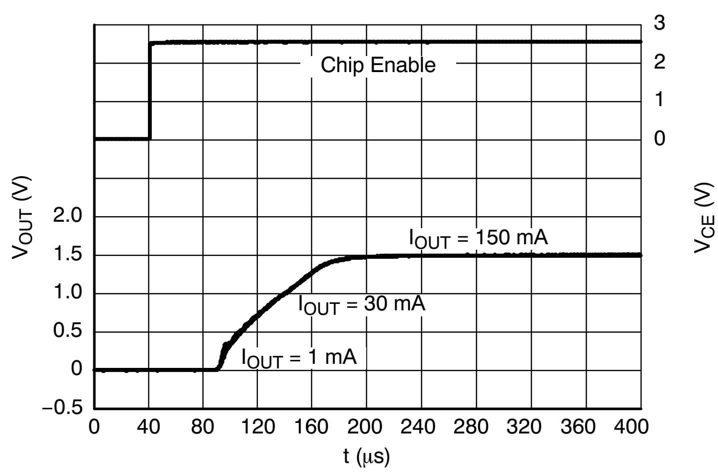


Figure 35. Start−up, 1.5 V Version NCP4681x, V_{IN} = 2.5 V

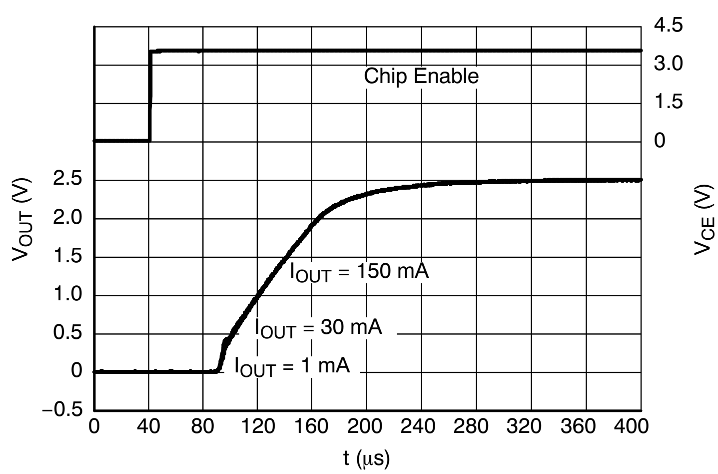


Figure 36. Start−up, 2.5 V Version NCP4681x, V_{IN} = 3.5 V

TYPICAL CHARACTERISTICS

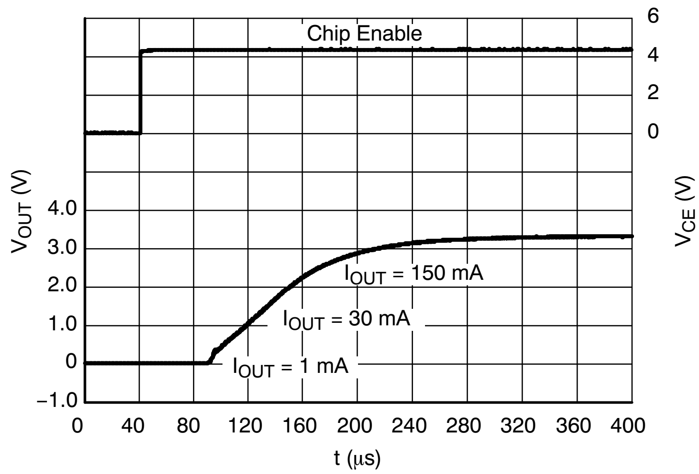


Figure 37. Start−up, 3.3 V Version NCP4681x, V_{IN} = 4.3 V

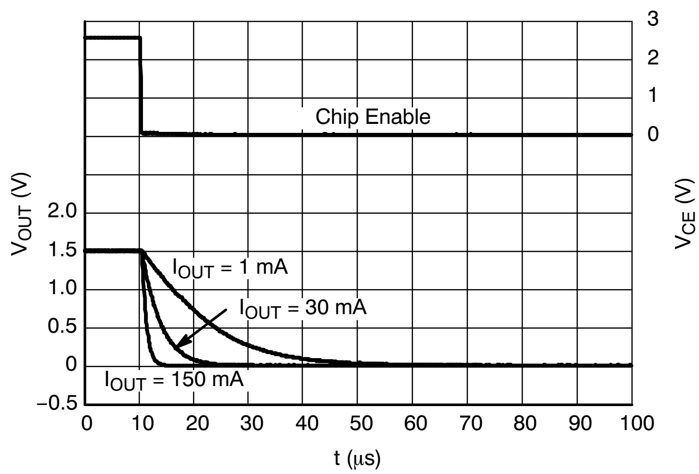


Figure 38. Shutdown, 1.5 V Version NCP4681D, V_{IN} = 2.5 V

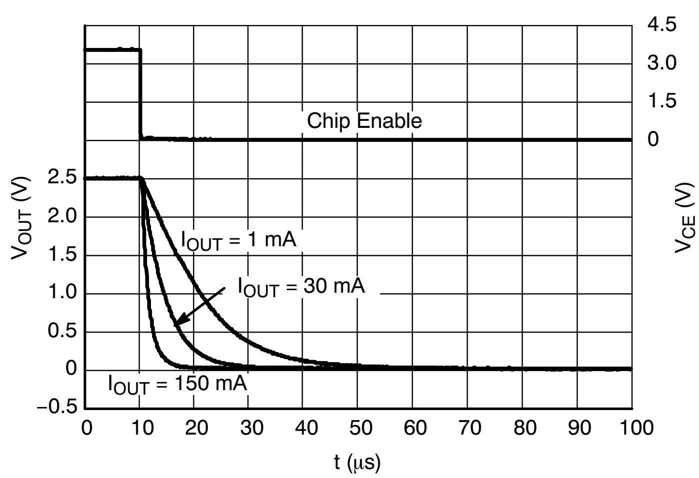


Figure 39. Shutdown, 2.5 V version NCP4681D, V_{IN} = 3.5 V

TYPICAL CHARACTERISTICS

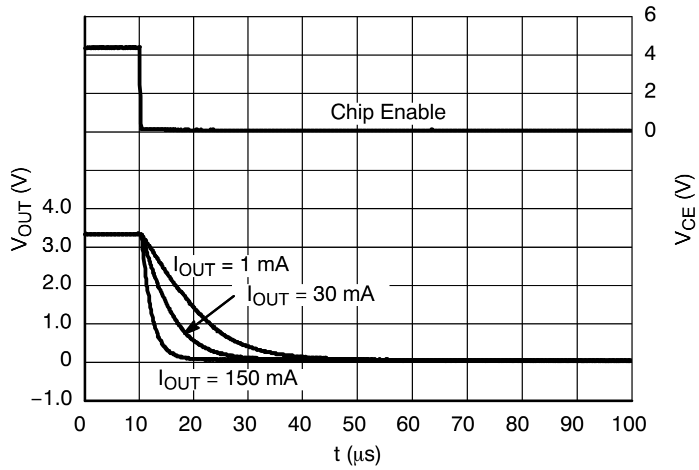


Figure 40. Shutdown, 3.3 V Version NCP4681D, V_{IN} = 4.3 V

APPLICATION INFORMATION

A typical application circuits for NCP4681 and NCP4684 series are shown in Figure 41.

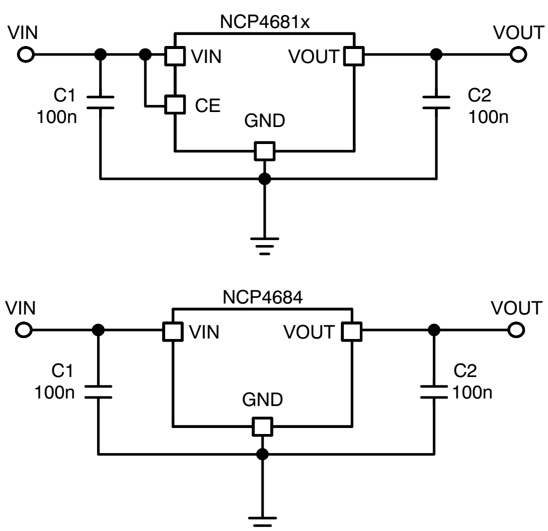


Figure 41. Typical Application Schematics

Input Decoupling Capacitor (C1)

A 0.1 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4681/4. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 0.1 μF ceramic output decoupling capacitor is enough to achieve stable operation of the IC. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger capacitor values and lower ESR improves dynamic parameters.

Enable Operation (NCP4681 Only)

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source. If the enable function is not needed connect CE pin to VIN.

Constant Slope Circuit

The constant slope circuit is used as a soft start circuit that allows the output voltage to start up slowly with a defined slope. This circuit minimizes inrush current at start up and also prevents against overshoot of the output voltage. The Constant slope circuit is fully built in and no external components are needed. Start up time and the output voltage slope is defined internally and there is no way for the user to change it. Start up into bigger output capacitor doesn't make any problem due to cooperation of constant slope circuit and current limit circuit.

Current Limit

This regulator includes a fold−back current limiting circuit. This type of protection doesn't limit output current up to specified current capability in normal operation, but when an over current situation occurs, the output voltage and current decrease until the over current condition ends. Typical characteristics of this protection scheme are shown in the Output voltage versus Output current graphs in the characterization section of this datasheet.

Output Discharger

The NCP4681D version includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal

As power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

PCB layout

Make the VIN and GND line as large as practical. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

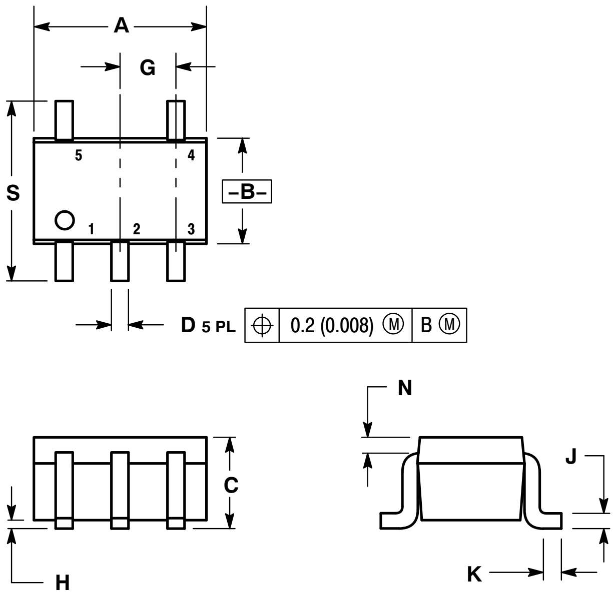
ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4681DMX29TCG	2.9 V	Auto discharge	B (fixed)*	XDFN0808 (Pb−Free)	10000 / Tape & Reel
NCP4681DMX33TCG	3.3 V	Auto discharge	B (fixed)*	XDFN0808 (Pb−Free)	10000 / Tape & Reel
NCP4681DMX35TCG	3.5 V	Auto discharge	B (fixed)*	XDFN0808 (Pb−Free)	10000 / Tape & Reel
NCP4681HMX35TCG	3.5 V	Enable high	B (fixed)*	XDFN0808 (Pb−Free)	10000 / Tape & Reel
NCP4681DSQ15T1G	1.5 V	Auto discharge	AQ15	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4681DSQ25T1G	2.5 V	Auto discharge	AQ25	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4681DSQ28T1G	2.8 V	Auto discharge	AQ28	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4681DSQ33T1G	3.3 V	Auto discharge	AQ33	SC−70 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Marking codes for XDFN0808 packages are unified.
**To order other package and voltage variants, please contact your ON Semiconductor sales representative.

PACKAGE DIMENSIONS

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE K

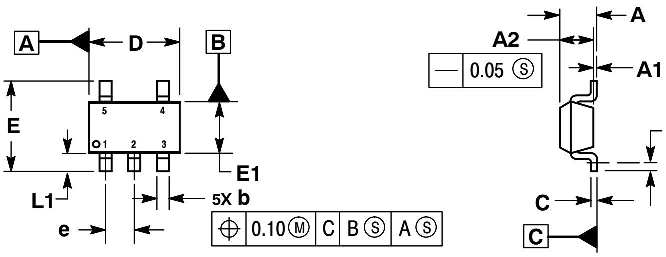


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

PACKAGE DIMENSIONS

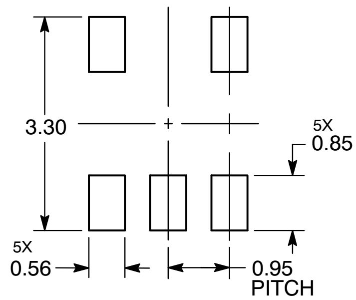
SOT−23 5−LEAD
CASE 1212−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

RECOMMENDED SOLDERING FOOTPRINT*

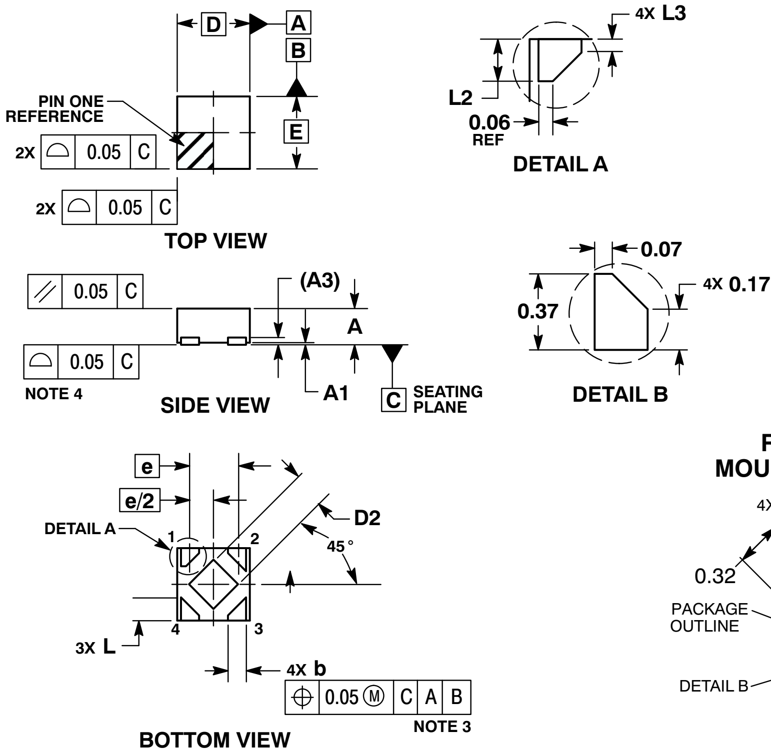


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

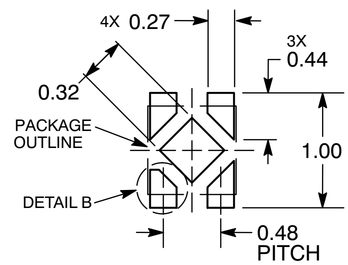
XDFN4 0.8x0.8, 0.48P
CASE 711AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
A3	0.10 REF	
b	0.17	0.27
D	0.80 BSC	
D2	0.20	0.30
E	0.80 BSC	
e	0.48 BSC	
L	0.23	0.33
L2	0.17	0.27
L3	0.01	0.11

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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