

MN101D01F / G / Y

VTR Servo

Type	MN101D01F / G / Y
ROM (×8-Bit)	96 K / 128 K / 128 K
RAM (×8-Bit)	2 560 / 3 072 / 3 072
Minimum Instruction Execution Time	With Main Clock operated 0.1397 μs (at 4.5 V to 5.5 V, 14.32 MHz) When Sub-Clock operated 71.5 μs (at 2.2 V to 5.5 V fixed to 14.32 MHz internal frequency division) 61 μs (at 2.2 V to 5.5 V, 32.768 kHz)
Interrupts	• RESET • Runaway • External 0, 1, 2, 3, 4/key input (P50 to 54) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Capstan FG • Control • HSW • Cylinder FG • VSYNC • Synchronous Output • OSD • XDS • Serial 0 • Serial 1 • Serial 2 • A/D (common with PWM 14 reference frequency)
Timer Counter	<p>Timer Counter 0: 16-Bit × 1 (Timer Output, Clock Function [max 2 s]) Clock Source 1/2, 1/4, 1/8, 1/16 of System Clock, 1/512 of XI Oscillation Clock or OSC Oscillation Clock Interrupt Source Overflow of Timer Counter 0</p> <p>Timer Counter 1: 16-Bit × 1 (Timer Output, linear Timer Counter Function) Clock Source 1/2, 1/4, 1/8, 1/16, CTL Signal of System Clock Interrupt Source Overflow of Timer Counter 1</p> <p>Timer Counter 2: 16-Bit × 1 (Timer Output, Input Capture (DCTL Specified Edge), Duty Judgment of DCTL Signal) Clock Source 1/2, 1/4, 1/8, 1/12, 1/16, 1/24 of System Clock Interrupt Source .Overflow of Timer Counter 2, Input of DCTL Specified Edge, Underflow of Timer 2 Shift Register 4-Bit Counter, Coincidence of Timer 2 Shift Register with Timer 2 Shift Register Compare Register</p> <p>Timer Counter 3: 16-Bit × 1 (Timer Output, Detection of Serial Indexing, Generation of Remote Control Output Carrier Frequency) Clock Source. 1/2, 1/4, 1/8, 1/16 of System Clock Interrupt Source Overflow of Timer Counter 3</p> <p>Timer Counter 4: 16-Bit × 1 (Timer Output, Event Count (P15 Input), Generation of Serial Transmission Clock) Clock Source . 1/8, 1/16 of System Clock, External Clock Input Interrupt Source Overflow of Timer Counter 4, Coincidence of Timer Counter 4 with OCR4</p> <p>Timer Counter 5: 17-Bit × 1 (Watchdog, Stable Oscillation Waiting Function) Clock Source System Clock Watchdog Interrupt Source 1/2¹⁶, 1/2¹⁹ of Timer Counter 5 Clear by Stable Oscillation ..After 256 Counts by Timer Counter 5 (2¹⁸ Counts of OSC Oscillation Clock)</p> <p>Timer Counter 6: 16-Bit × 1 (Clock Function [max 2 s]) Clock Source . 1/512 of OSC Oscillation Clock, XI Oscillation Clock, 1/4, 1/8, 1/64, 1/128 of System Clock Interrupt Source 1/2¹³, 1/2¹⁴, 1/2¹⁶, Overflow of Timer Counter 6</p>
Serial Interface	<p>Serial 0: 8-Bit × 1 (Synchronous Type/Start-Stop Synchronous Type) (Transfer Direction of MSB/LSB Selectable) Synchronous Type Clock Source 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of System Clock, 2-Division Timer 4 Output, $\overline{\text{SBT0}}$ Pin Input Clock for UART 8-Division of Above Clock, 2-Division Timer 4 Output, $\overline{\text{SBT0}}$ Pin Input</p> <p>Serial 1: 8-Bit × 1 (Synchronous Type/Remote Control Transmission/Simple Remote Control Receive) (Transfer Direction of MSB/LSB Selectable, Start Condition Function) Clock Source 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of System Clock, 2-Division Timer 4 Output, $\overline{\text{SBT1}}$ Pin Input Remote Control Clock 2-Division Timer Output</p> <p>Serial 2: 8-Bit × 1 (I²C) (Master Transmission/Reception, Slave Transmission/Reception) Clock Source . . . 1/72, 1/80, 1/84, 1/96, 1/102, 1/112, 1/128, 1/144, 1/160, 1/168, 1/192, 1/224, 1/256, 1/320, SCK Pin Input of System Clock</p>

OSD			Accommodation with Menu or Super Impose Display
			Applicable Broadcasting System NTSC, PAL, PAL-M, PAL-N
			Screen Configuration 24 Characters × 2n Rows (n = 1 to 6)
			Character Type Max 512 Character Types (Variable)
			Character Size 12 × 18 Dots
			Enlarged Characters Each × 2, × 3 or × 4 Settings in Horizontal and Vertical
			Character Interpolation None
			Background Color 8-Hue Settable (Settable in The Row Unit at Menu Display)
			Background Intensity 8 Gradations Settable in The Row Unit
			Character Color White
			Character Intensity 8 Gradations Settable in The Row Unit
			Frame Function 1-Dot frame in 4 or 8 Directions
			Frame Intensity 4 Gradations Settable in The Row Unit
			Box Shade Function Settable in The Character Unit (Only at Composite Output with 128 Character Types or More)
			Blinking None (Covered by Software)
			Inverted Character Settable in The Character Unit
			Halftone Settable in The Row Unit in 2 Intensity Gradations (Setting in The Row Unit)
			Input Composite Video Signal Input (Output Level 1 V[p-p] / 2 V[p-p])
			Clamp Method Sync Chip Clamp, Clamp Level in 4 Levels
			Output Composite Video Output
			Digital Output (6 pins)
			8 Character and Background Colors Each Settable at Digital Output
			Measure Against Image Fluctuation Built-In AFC Circuit
			Sync Signal Detection Function Detection Functions for Horizontal and Vertical Sync Signals (Integral System) With Horizontal Sync Signal Interpolation Function
XDS			Built-In U S Closed Caption Data Slicer (Optional 2 Line Data can be Extracted)
ROM Correction			Correcting Address Designation Up to 2 Addresses Possible
			Correction Method Correction Program Being Saved in Internal RAM
I/O Pins	I/O	73	• Common use 73 ports 0, 1, 2, 4, 5, 6, 7, A, B, by-bit
	Input	4	• Common use 4
A/D			8-Bit × 12ch (Without S/H)
PWM			13-Bit × 2ch (at Repetition Cycle 572 μs, 14.32 MHz), 10-Bit × 2ch (at Repetition Cycle 71.5 μs, 14.32 MHz), 14-Bit × 1ch (at Repetition Cycle 1.144 μs, 14.32 MHz)
ICR			18-Bit × 6ch
OCR			16-Bit × 7ch, 8-Bit × 1ch
Special Ports			Buzzer Output, 3-State Output (PTO) VLP Pin, Synchronous Output 7, 3-State Synchronous Output 4, Remote Control Receive, CTL Amp, Built-In FG Amp, Output of 1/2 OSC Oscillation Clock (2 V[p-p]), Output of 1/4 OSC Oscillation Clock (1 V[p-p])
Notes			VISS/VASS Detection Function
Package			QFP100-P-1818

See the next page for electrical characteristics, support tool and pin assignment.

Electrical Characteristics

Supply Current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating Supply Current	IDD1	14.32 MHz operation without load, VDD = 5 V		60	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 2.7 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply Current at STOP	IDSP	Stop of oscillation without load		0	20	μA
Supply Current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

(Ta = 25 °C±2 °C, VDD = 5.0 V, VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion Relative Error	ΔNLAD				±3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage			0		5	V

(Ta = 25 °C±2 °C, VDD = 5.0 V, VSS = 0 V)

Support Tool

In-Circuit Emulator

PX-ICE101C / D + PX-PRB101D01-C / D

EPROM built-in Type

Type	MN101DP01G / 01Y OTP MN101DP01GFA / 01YAF ATP MN101DP01GAC / 01YAC [All ES (Engineering Sample) available]
ROM (× 8-Bit)	128 K
RAM (× 8-Bit)	3 072
Minimum Instruction Execution Time	0.1397 μs (at 4.5 V to 5.5 V, 14.32 MHz) 71.5 μs (at 2.2 V to 5.5 V fixed to 14.32 MHz internal division)
Package	QFP100-P-1818B OTP QFP100-P-1818B ATP With Ceramic Window

Pin Assignment



QFP100-P-1818B

Maintenance/Discontinued Includes planned discontinuation type
 Please visit following URL about latest information.
<http://www.semicon.panasonic.co.jp/en/>

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