![National Semiconductor logo] **National Semiconductor**

DS36BC956
Low Power BiCMOS HEX Differential Bus Transceiver

General Description

The DS36BC956 is a low power BiCMOS, six bit RS-485 Differential Bus Transceiver optimally designed for high speed parallel multipoint I/O buses including SCSI-1, -2, -3 and IPI interfaces. The device is offered in a thermally enhanced 48L SSOP package, offering a balance between integration and power dissipation (Junction Temperature) in an extremely small foot print. Three devices can implement a complete SCSI initiator or target interface.
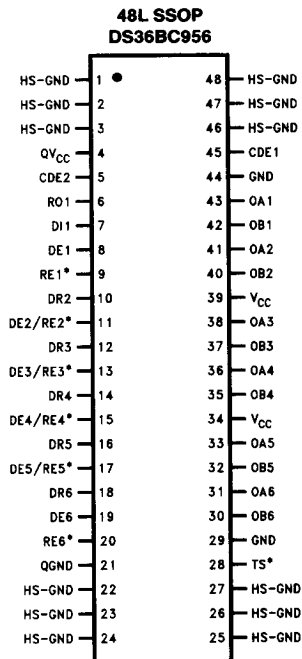
For maximum flexibility the device provides three different types of transceivers. Channel one is a type 1 configuration, with separate receiver output, driver input, and enable pins. Channels 2, 3, 4, 5 are type 2 transceivers, and provide a direction control pin and a bi-directional data pin. These channels are ideal for use on data lines and bi-directional control lines. Channel six is a type 3 transceiver, with a bi-directional data pin, and separate enable pins. This allows it to be configured as a driver, receiver, or transceiver and is ideal for use on single direction control lines.

Features

- Meets EIA RS-485 multipoint standard
- Meets SCSI-2 differential specifications
- Low power BiCMOS design
- High speed design/low skew specifications
- Available in thermally enhanced 48L SSOP package
- Glitch free driver outputs on power up and down
- Thermal shutdown protection and reporting pin (TS*)
- Wide common mode range: $-7V$ to $+12V$
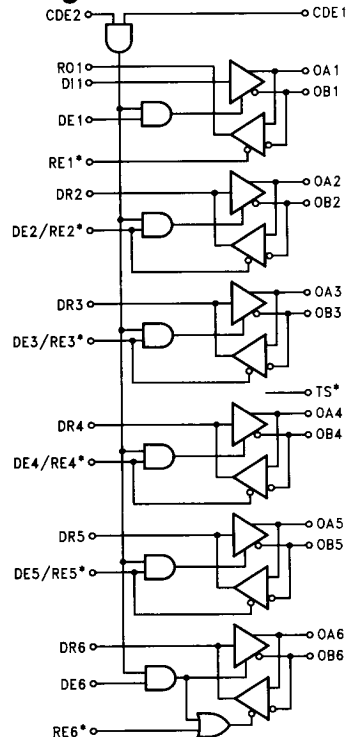- 35 mV minimum hysteresis
- Flow-through pin-out

Connection Diagram

48L SSOP
DS36BC956

HS-GND	1	48	HS-GND
HS-GND	2	47	HS-GND
HS-GND	3	46	HS-GND
QV$_{CC}$	4	45	CDE1
CDE2	5	44	GND
RO1	6	43	OA1
DI1	7	42	OB1
DE1	8	41	OA2
RE1*	9	40	OB2
DR2	10	39	V$_{CC}$
DE2/RE2*	11	38	OA3
DR3	12	37	OB3
DE3/RE3*	13	36	OA4
DR4	14	35	OB4
DE4/RE4*	15	34	V$_{CC}$
DR5	16	33	OA5
DE5/RE5*	17	32	OB5
DR6	18	31	OA6
DE6	19	30	OB6
RE6*	20	29	GND
QGND	21	28	TS*
HS-GND	22	27	HS-GND
HS-GND	23	26	HS-GND
HS-GND	24	25	HS-GND

TL/F/11874–1

Order Number DS36BC956MEA
See NS Package Number MS48A

Logic Diagram

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Note: * denotes active LOW pin

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}, QV_{CC})	7V
Input Voltage (DR, DI, CDE, DE/RE*, DE, RE*)	5.5V
Driver Output Voltage/Receiver	
Input Voltage (OA, OB)	−10V to +15V
Receiver Output Voltage (DR, RO)	5.5V
Thermal Shutdown Report Pin (TS*)	5.5V
Maximum Package Power Dissipation @ +25°C	
48L SSOP Package	2016 mW
(derate SSOP Package 16.2 mW/°C above +25°C)	

Storage Temperatrure Range	−65°C to +150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Maximum Junction Temperature (T_J)	+150°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7.0	+12	V
Operating Temperature (T_A)			
DS36BC956	0	70	°C

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 12)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_O	Output Voltage	$I_O = 0$ mA (V_{OA}, V_{OB})		0		V_{CC}	V
V_{OD0}	Differential Driver Output Voltage (No Load)	$I_L = 0$ mA, $R_L = \infty$ *(Figure 1)*		1.5		V_{CC}	V
V_{OD1}	Differential Driver Output Voltage (Full Load)	$I_O = 60$ mA, $V_{CM} = 0$V		1.5	1.7		V
V_{OD2}	Differential Driver Output Voltage (Termination Load)	$R_L = 100\Omega$, (422) *(Figure 1, Note 3)*		0.5 V_{OD1} or 2.0	2.5		V
		$R_L = 54\Omega$ *(Figure 1)* (485)		1.5	2.2		V
V_{OD3}	Differential Driver Output Voltage	$V_{TEST} = -7$V to $+12$V *(Figure 2)* (485)	OA, OB	1.5		5.0	V
$\Delta|V_{OD2}|$, $\Delta|V_{OD3}|$	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	*(Figure 1, Note 4)* (422 and 485)				0.2	V
V_{OD4}	Differential Driver Output Voltage (SCSI-3)			1.0	2.2		V
V_{OC}	Driver Common Mode Output Voltage (Note 5)	$R_L = 54\Omega$ or 100Ω *(Figure 1)* (422 and 485)		−1.0	2.1	3.0	V
$\Delta|V_{OC}|$	Change in Magnitude of Common Mode Output Voltage	*(Figure 1, Note 4)* (422 and 485)				0.2	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -55$ mA		2.7	3.0		V
V_{OL}	Output Voltage LOW	$I_{OL} = 55$ mA			1.5	1.7	V
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW		DR, DI			0.8	V
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA				−1.5	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.4$V (Note 6)				20	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.4$V (Note 6)				−100	μA

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Electrical Characteristics (Continued)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 12)

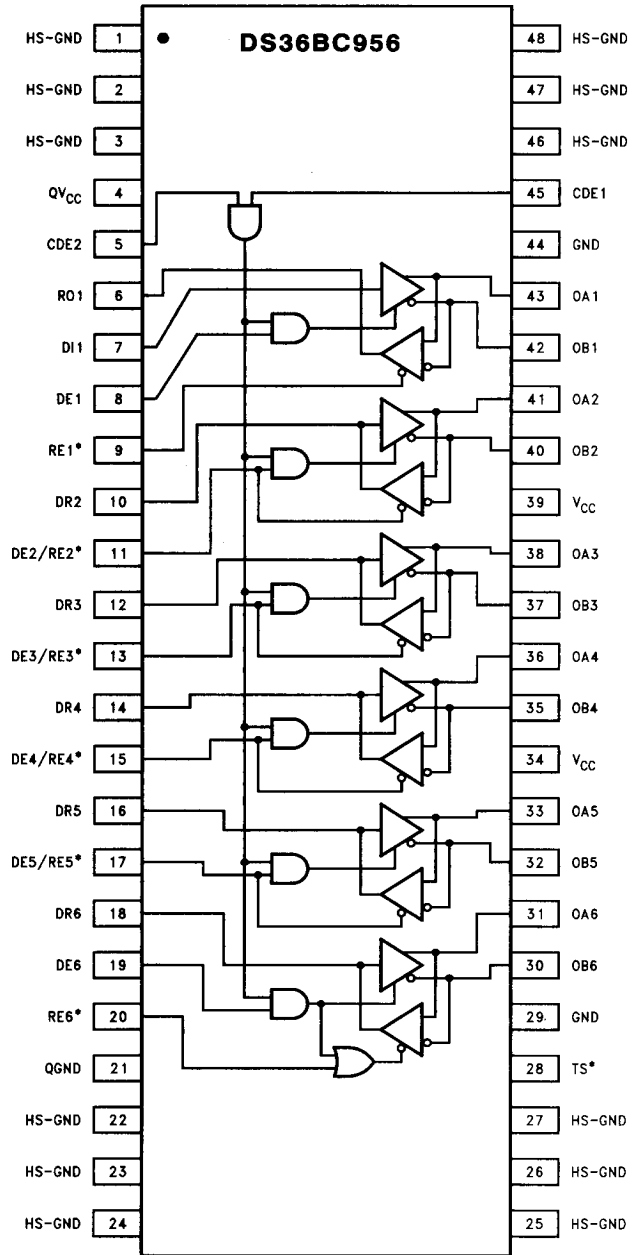| Symbol	Parameter	Conditions			Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS (Continued)									
I_{OSD}	Driver Short-Circuit Output Current (Note 7)	$V_O = -7V$	(485)		OA, OB			-250	mA
		$V_O = 0V$	(422)					-150	mA
		$V_O = +12V$	(485)					250	mA
RECEIVER CHARACTERISTICS									
V_{OH}	Output Voltage HIGH *(Figure 3)*	$V_{ID} = 0.20V$	$I_{OH} = -0.4$ mA		DR, RO	2.4	3.3		V
			$I_{OH} = -0.1$ mA			3.0	3.5		V
		$V_{ID} = $ Open	$I_{OH} = -0.4$ mA			2.4			V
V_{OL}	Output Voltage LOW	$V_{ID} = -0.20V$, $I_{OL} = 8$ mA *(Figure 3)*					0.3	0.5	V
V_{TH}	Differential Input HIGH Threshold Voltage (Note 8)	$V_O = V_{OH}$, $I_O = -0.4$ mA (422 and 485)			OA, OB			200	mV
V_{TL}	Differential Input LOW Threshold Voltage (Note 8)	$V_O = V_{OL}$, $I_O = 8.0$ mA (422 and 485)				-200			mV
V_{HST}	Hysteresis (Note 9)	$V_{CM} = 0V$					35		mV
I_{OSR}	Short Circuit Output Current	$V_O = 0V$ (Note 7)			DR, RO	-15	-30	-100	mA
I_{OZR}	TRI-STATE® Output Current	$V_O = $ GND, 0.4V, 2.4V, V_{CC}			RO			20	μA
DEVICE CHARACTERISTICS									
V_{IH}	Enable Input Voltage HIGH				DE/RE*, CDE, DE, RE*	2.0			V
V_{IL}	Enable Input Voltage LOW							0.8	V
V_{CL}	Enable Input Clamp Voltage	$I_{CL} = -18$ mA						-1.5	V
I_{IH}	Enable Input Current HIGH	$V_{CC} = 5.25V$ and $V_{CC} = 3.0V$						20	μA
I_{IL}	Enable Input Current LOW							-20	μA
I_{IN}	Line Input Current (Note 10)	Other Input = 0V DE/RE*, CDE, and DE = 0.8V	$V_I = +12V$		OA, OB		0.5	1.0	mA
			$V_I = -7V$				-0.4	-0.8	mA
I_{ING}	Line Input Current (Power Up/Down)	Other Input = 0V DE/RE*, CDE, and DE = 2.0V $V_{CC} = 3.0V$	$V_I = +12V$				0.5	1.0	mA
			$V_I = -7V$				-0.4	-0.8	mA
V_{OL}	Output Voltage LOW	$I_{OL} = 8$ mA			TS*		0.3		V
I_{CCD}	No Load Supply Current (Note 11)	DR On, REC Off			V_{CC}		16	TBD	mA
I_{CCR}		DR Off, REC On					23	TBD	mA
I_{CCX}		DR Off, REC Off					8	TBD	mA

Switching Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Note 12)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DRIVER SINGLE-ENDED CHARACTERISTICS						
t_{PZH}	Output Enable Time To High Level	$R_L = 110\Omega$ *(Figure 8)*		30	60	ns
t_{PZL}	Output Enable Time To Low Level	$R_L = 110\Omega$ *(Figure 7)*		30	60	ns
t_{PHZ}	Output Disable Time From High Level	$R_L = 110\Omega$ *(Figure 8)*		30	60	ns
t_{PLZ}	Output Disable Time From Low Level	$R_L = 110\Omega$ *(Figure 7)*		30	60	ns
DRIVER DIFFERENTIAL CHARACTERISTICS (ΔV_{CC} = TBD mV, ΔT_A = TBD°C)						
t_{PLHD}	Differential Propagation Delay (Note 13)	$R_L = 54\Omega$, $C_L = 50$ pF, CD = 50 pF *(Figure 4)*	tm1	9	tm1 + 4	ns
		R1 = R3 = 165Ω, R2 = 75Ω, CD = 60 pF *(Figure 5)*	tm2	9	tm2 + 4	ns
t_{PHLD}	Differential Propagation Delay (Note 13)	$R_L = 54\Omega$, $C_L = 50$ pF, CD = 50 pF *(Figure 4)*	tm3	9	tm3 + 4	ns
		R1 = R3 = 165Ω, R2 = 75Ω, CD = 60 pF *(Figure 5)*	tm4	9	tm4 + 4	ns
t_r, t_f	Transition Times	$R_L = 54\Omega$, $C_L = 50$ pF, CD = 50 pF *(Figure 4)*	2	4	16	ns
		R1 = R3 = 165Ω, R2 = 75Ω, CD = 60 pF *(Figure 5)*	2	4	16	ns
t_{SKD}	|t_{PLHD}–t_{PHLD}| Differential Driver Skew	$R_L = 54\Omega$, $C_L = 50$ pF, CD = 50 pF *(Figure 4)*		TBD	TBD	ns
		R1 = R3 = 165Ω, R2 = 75Ω, CD = 60 pF *(Figure 5)*		TBD	TBD	ns
t_{PZD}	Differential Output Enable Time	R1 = R3 = 165Ω, R2 = 75Ω CD = 60 pF *(Figure 6)*		30	60	ns
t_{PDZ}	Differential Output Disable Time			30	60	ns
RECEIVER CHARACTERISTICS (ΔV_{CC} = TBD mV, ΔT_A = TBD°C)						
t_{PLHD}	Differential Propagation Delay	$C_L = 50$ pF, *(Figure 9)*	tm5	TBD	tm5 + 5	ns
t_{PHLD}	Differential Propagation Delay		tm6	TBD	tm6 + 5	ns
t_{SKD}	|t_{PLHD} – t_{PHLD}| Differential Receiver Skew			TBD	TBD	ns
t_{PZH}	Output Enable Time To High Level	$C_L = 15$ pF *(Figure 10)*		30	80	ns
t_{PZL}	Output Enable Time To Low Level			30	80	ns
t_{PHZ}	Output Disable Time From High Level			30	80	ns
t_{PLZ}	Output Disable Time From Low Level			30	80	ns

Note: TBD denotes "To Be Determined" and will be specified once characterization of the device is complete.
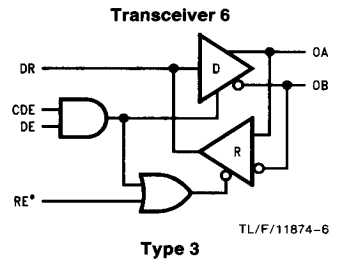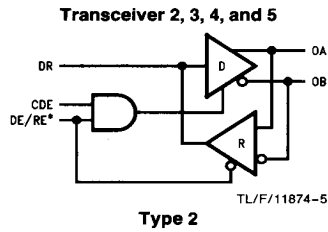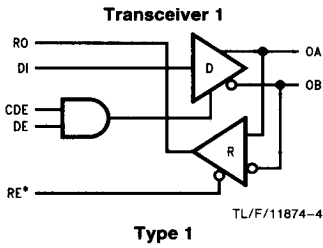
3

Logic Diagram (Continued)

DS36BC956

Left			Right	
HS-GND	1		48	HS-GND
HS-GND	2		47	HS-GND
HS-GND	3		46	HS-GND
QV$_{CC}$	4		45	CDE1
CDE2	5		44	GND
RO1	6		43	OA1
DI1	7		42	OB1
DE1	8		41	OA2
RE1*	9		40	OB2
DR2	10		39	V$_{CC}$
DE2/RE2*	11		38	OA3
DR3	12		37	OB3
DE3/RE3*	13		36	OA4
DR4	14		35	OB4
DE4/RE4*	15		34	V$_{CC}$
DR5	16		33	OA5
DE5/RE5*	17		32	OB5
DR6	18		31	OA6
DE6	19		30	OB6
RE6*	20		29	GND
QGND	21		28	TS*
HS-GND	22		27	HS-GND
HS-GND	23		26	HS-GND
HS-GND	24		25	HS-GND

Note: * denotes active low pin.

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Logic Diagram (Continued)

Transceiver 1

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Type 1

Transceiver 2, 3, 4, and 5

TL/F/11874-5

Type 2

Transceiver 6

TL/F/11874-6

Type 3

Truth Tables

TRANSCEIVERS: 2, 3, 4, 5

Enables			Driver	Receiver
CDE1	CDE2	DE/RE*		
L	X	H	OFF	OFF
X	L	H	OFF	OFF
L	X	L	OFF	ON
X	L	L	OFF	ON
H	H	H	ON	OFF
H	H	L	OFF	ON

TRANSCEIVERS: 1, 6

DRIVER

Enables			Driver
CDE1	CDE2	DE	
L	X	H	OFF
X	L	H	OFF
L	X	L	OFF
X	L	L	OFF
H	H	H	ON
H	H	L	OFF

RECEIVER

Enable	Receiver
RE*	
H	OFF
L	ON

Note: For REC6 to be active (ON), DE6 must be L (LOW).

DRIVER

Driver	Input	Outputs	
	DR or DI	0A	OB
OFF	X	Z	Z
ON	L	L	H
ON	H	H	L

RECEIVER

Receiver	Inputs	Output
	OA–OB	DR or RO
OFF	X	Z
ON	OPEN	H
ON	≥ +200 mV	H
ON	≤ −200 mV	L

3

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Parameter Measurement Information
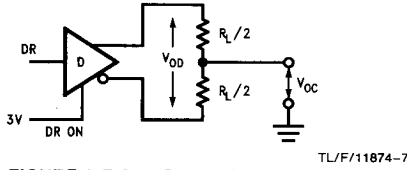
FIGURE 1. Driver Output (V_{OD}, V_{OC})

TL/F/11874–7
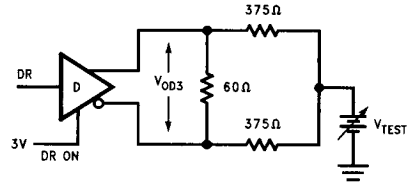
FIGURE 2. Driver Output (V_{OD3})

TL/F/11874–8
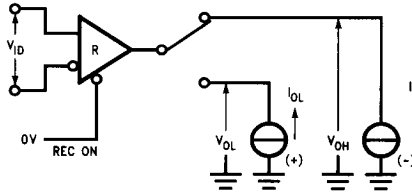
FIGURE 3. Receiver Output (V_{OH}, V_{OL})

TL/F/11874–9
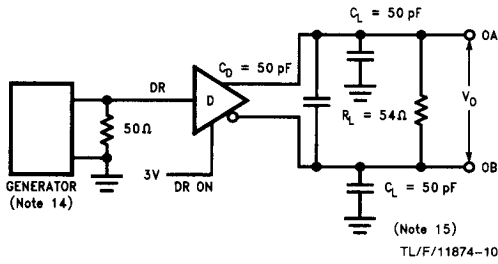
FIGURE 4. Driver Differential Propagation Delay and Transition Timing (t_{PLHD}, t_{PHLD}, t_r, t_f)
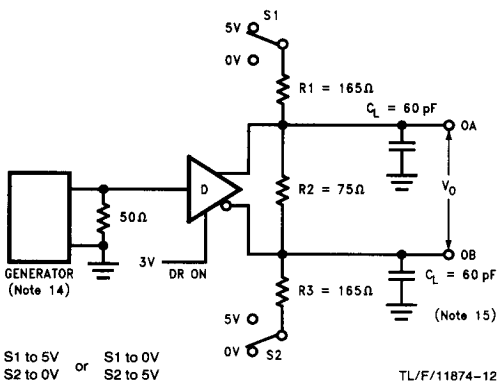
TL/F/11874–10

TL/F/11874–11
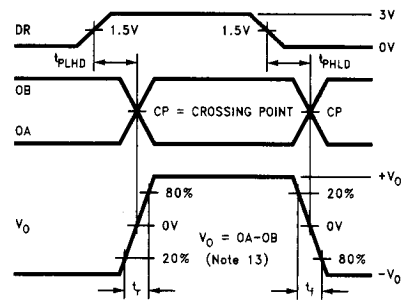
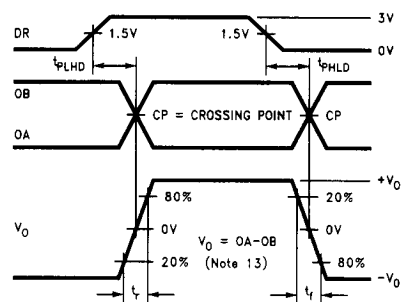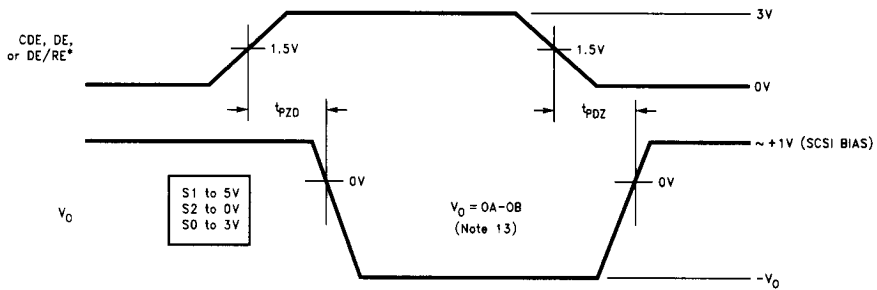S1 to 5V   or   S1 to 0V
S2 to 0V   S2 to 5V

FIGURE 5. Driver Differential Propagation Delay and Transition Timing with SCSI Termination (t_{PLHD}, t_{PHLD}, t_r, t_f)

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TL/F/11874–13

Parameter Measurement Information (Continued)

5V S1
0V
R1 = 165Ω
C_L = 60 pF OA

3V S3 DR D
0V
R2 = 75Ω V_O

OB
C_L = 60 pF
(Note 15)

CDE, DE,
or DE/RE* R3 = 165Ω
50Ω
5V
0V S2

GENERATOR
(Note 14)

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CDE, DE,
or DE/RE*
1.5V 3V
1.5V
0V
t_{PZD} t_{PDZ}

$+V_O$

V_O
S1 to 0V
S2 to 5V
S3 to 3V
0V V_O = OA–OB
(Note 13)
0V

~ –1V (SCSI BIAS)
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CDE, DE,
or DE/RE*
1.5V 3V
1.5V
0V
t_{PZD} t_{PDZ}

~ +1V (SCSI BIAS)

V_O
S1 to 5V
S2 to 0V
S0 to 3V
0V V_O = OA–OB
(Note 13)
0V
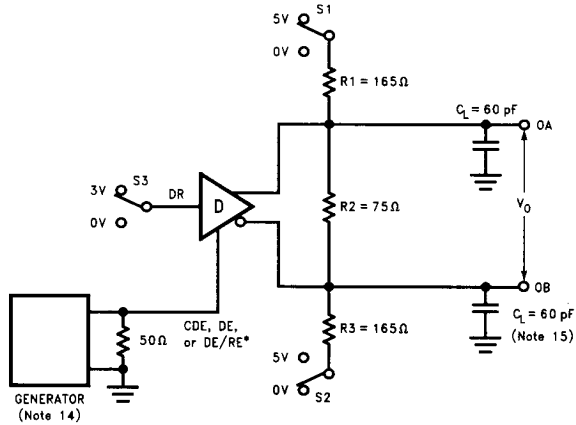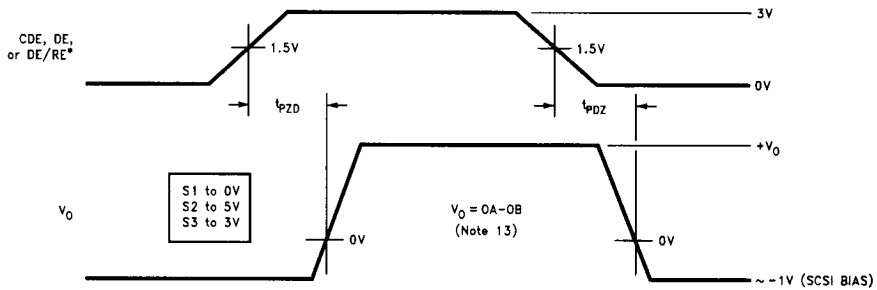
$-V_O$
TL/F/11874–27

FIGURE 6. Driver Differential Enable and Disable Times with SCSI Termination (t_{PZD}, t_{PDZ})

3

Parameter Measurement Information (Continued)
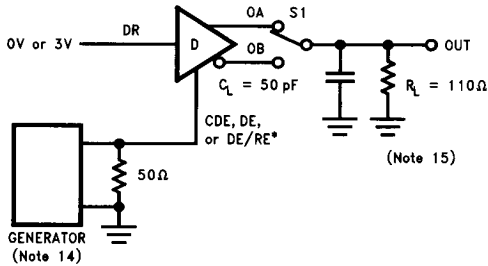

5V

$R_L = 110\Omega$

0V or 3V → D

OA S1

OB

OUT

$C_L = 50\,pF$
(Note 15)

CDE, DE,
or DE/RE*

50Ω
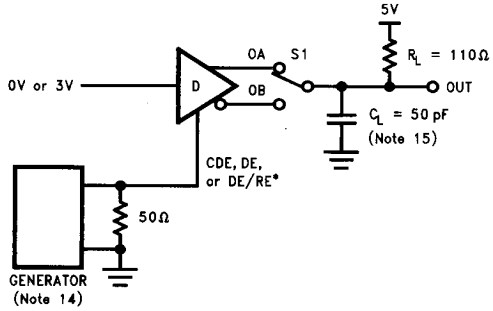
GENERATOR
(Note 14)

S1 to OA for DI = 0V
S1 to OB for DI = 3V

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CDE, DE
or DE/RE*

3V

1.5V   1.5V

0V

t_{PZL} t_{PLZ}

OUT

5V

2.3V

$V_{OL} + 0.5V$

0.5V

V_{OL}

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FIGURE 7. Driver Enable and Disable Timing (t_{PZL}, t_{PLZ})

0V or 3V → DR → D

OA S1

OB

OUT

$C_L = 50\,pF$

$R_L = 110\Omega$

CDE, DE,
or DE/RE*

(Note 15)

50Ω

GENERATOR
(Note 14)
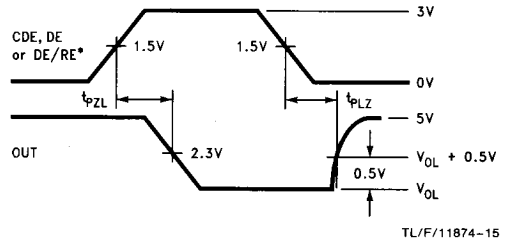
S1 to OA for DI = 3V
S1 to OB for DI = 0V

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CDE, DE
or DE/RE*

3V

1.5V   1.5V

0V

t_{PZH} t_{PHZ}

V_{OH}

0.5V

OUT

2.3V

$V_{OH} - 0.5V$

GND

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FIGURE 8. Driver Enable and Disable Timing (t_{PZH}, t_{PHZ})

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Parameter Measurement Information (Continued)

GENERATOR
(Note 14)

Vg

Vg

50 Ω

50 Ω

0V

OA

OB

R

REC ON

OUT

C_L = 50 pF
(Note 15)

OB

OA

3V

2V

2V

1V

t_{PLHD}

t_{PHLD}

OUT

1.5V
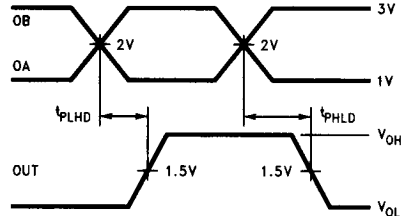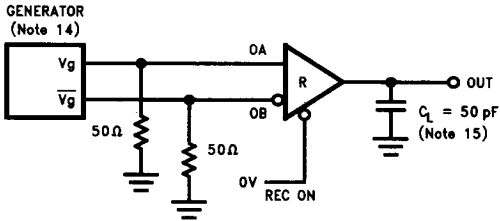
1.5V

V_{OH}

V_{OL}
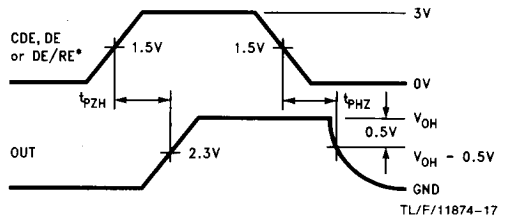
TL/F/11874–18

TL/F/11874–19

FIGURE 9. Receiver Differential Propagation Delay Timing (t_{PLHD}, t_{PHLD})

1.5V

−1.5V

S1

OA

OB

C_L = 15 pF

OUT
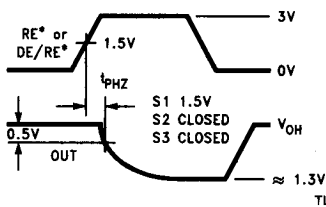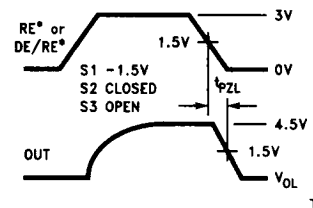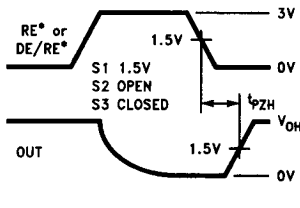
2 kΩ

5V

S2
(Note 16)

GENERATOR
(Note 14)

RE* or
DE/RE*

50 Ω

5 kΩ

(Note 15)

S3

TL/F/11874–20

RE* or
DE/RE*

1.5V

3V

0V

S1 1.5V
S2 OPEN
S3 CLOSED

t_{PZH}

OUT

1.5V

V_{OH}

0V

TL/F/11874–21

RE* or
DE/RE*

1.5V

3V

0V

S1 −1.5V
S2 CLOSED
S3 OPEN

t_{PZL}

4.5V

OUT

1.5V

V_{OL}

TL/F/11874–22

RE* or
DE/RE*

1.5V

3V

0V

t_{PHZ}

S1 1.5V
S2 CLOSED
S3 CLOSED

0.5V

OUT

V_{OH}

≈ 1.3V

TL/F/11874–23

RE* or
DE/RE*

1.5V

S1 −1.5V
S2 CLOSED
S3 CLOSED

3V

0V

t_{PLZ}
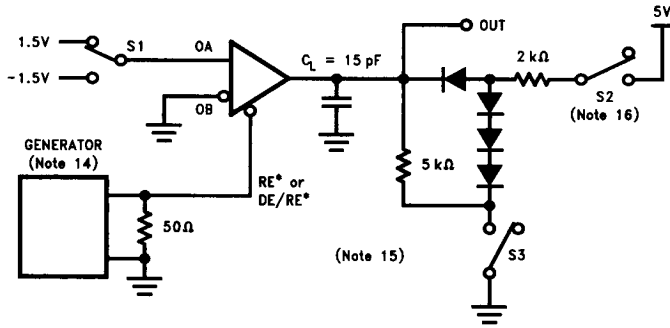
≈ 1.3V

OUT

0.5V

V_{OL}

TL/F/11874–24

FIGURE 10. Receiver Enable and Disable Timing (t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ})

3

Parameter Measurement Information (Continued)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: The minimum limit is either 2.0V or 50% of the magnitude of V_{OD1}, whichever is greater.

Note 4: $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes state.

Note 5: In TIA/EIA-422-A and TIA/EIA-485 standards, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: I_{IH} and I_{IL} include driver input current and receiver TRI-STATE leakage current on DR(2-6).

Note 7: Short one output at a time to avoid causing a thermal shutdown of the device due to excessive power dissipation.

Note 8: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 9: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

Note 10: I_{IN} includes the receiver input current and TRI-STATE leakage current.

Note 11: Total package supply current.

Note 12: All typicals are given for $V_{CC} = 5.0V$ and $T_A = +25°C$.

Note 13: Differential propagation delays are calculated from single-ended propagation delays at the cross point.

Note 14: The input pulse is supplied by a generator having the following characteristics: $f = 1.0$ MHz, 50% duty cycle, t_r and $t_f < 6.0$ ns, $Z_0 = 50\Omega$.

Note 15: C_L includes probe and stray capacitance.

Note 16: Diodes are 1N916 or equivalent.

Pin Descriptions

V_{CC} (Pins 34, 39)—**Power Supply Pin:** Positive power supply pins for TIA/EIA-485 driver output structures. Both pins must be connected to power supply rail for proper operation of the drivers. V_{CC} range is specified from 4.75V to 5.25V, nominally 5.0V.

GND (Pins 29, 44)—**Ground Pin:** Ground pins for TIA/EIA-485 driver output structures. Both pins must be connected to ground plane for proper operation of the drivers.

QV_{CC} (Pin 4)—**Quiet Power Supply Pin:** Positive power supply pin for internal driver logic, thermal shutdown circuitry, and receivers. This pin must be connected to a power supply rail for the device to operate properly. QV_{CC} range is specified from 4.75V to 5.25V, nominally 5.0V.

QGND (Pin 21)—**Quiet Ground Pin:** Ground pin for internal driver logic, thermal shutdown circuitry, and receivers. This pin must be connected to a ground plane for the device to operate properly.

HS-GND (Pins 1, 2, 3, 22, 23, 24, 25, 26, 27, 46, 47, 48)—**Heat Sink Ground Pin:** Ground pins connected internally to an enhanced lead frame to improve the thermal performance of the package. These pins should be connected to the ground plane for maximum heat transfer. Additional PCB copper foil can be added to further enhance the thermal capabilities of the package.

CDE1,2 (Pins 45, 5)—**Common Driver Enable:** Common Driver Enable for TRI-STATE control of driver output stage. A HIGH on the driver enable pins enables the driver outputs. A LOW on a CDE pin will TRI-STATE all driver outputs.

DE1,6 (Pins 8, 19)—**Driver Enable:** Driver Enable for TRI-STATE control of driver output stage. A HIGH on the driver enable pins enables the driver output. A LOW on a DE pin will TRI-STATE the respective channels driver outputs.

DI1 (Pin 7)—**Driver Input Pin:** TTL/CMOS pin that is used as driver input.

RE*1,6 (Pins 9, 20)—**Receiver Enable Bar:** Receiver Enable for TRI-STATE control of receiver output stage. A LOW on this pin enables the receiver output. A HIGH on this pin will TRI-STATE the respective channel's receiver output.

DE/RE*2,3,4,5 (Pins 11 13, 15, 17)—**Driver Enable/Receiver Enable Bar:** Driver Enable/Receiver Enable pin provides direction control of the respective transceiver. A HIGH on this pin enables the driver output and will TRI-STATE the receiver output stage. A LOW on this pin will TRI-STATE the driver outputs and enable the receiver output stage.

DR2,3,4,5,6 (Pins 10, 12, 14, 16, 18)—**Driver Input/Receiver Output Pin:** Bi-directional TTL/CMOS pin that is used as driver input or receiver output depending upon the state of the enable pins. The driver input accepts TTL/CMOS levels. The receiver output stages are specified with TTL and CMOS loading conditions.

OA1,2,3,4,5,6 (Pins 43, 41, 38, 36, 33, 31)—**True Driver Output/Receiver Input Pin:** This pin is the true driver output (same state as input state) or the true receiver input pin depending upon enable state.

OB1,2,3,4,5,6 (Pins 42, 40, 37, 35, 32, 30)—**Inverted Driver Output/Receiver Input Pin:** This pin is the inverted driver output (opposite state of input) or the inverted receiver input pin depending upon enable state.

TS* (Pin 28)—**Thermal Shutdown:** This pin reports the occurrence of thermal shutdown which will TRI-STATE the driver outputs. Thermal shutdown typically results from severe bus faults which produce excessive on chip power dissipation. If this power dissipation elevates the function temperature above +150°C, the internal thermal shutdown circuitry is triggered and the TS* pin is asserted. The TS* pin is an open collector pin. This allows the TS* outputs of several devices to be wire ORed.

RO1 (Pin 6)—**Receiver Output Pin:** The receiver output pin is specified with TTL and CMOS loading conditions.