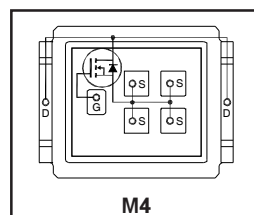


- Logic Level
- Advanced Process Technology
- Optimized for Automotive DC-DC, Motor Drive and other Heavy Load Applications
- Exceptionally Small Footprint and Low Profile
- High Power Density
- Low Parasitic Parameters
- Dual Sided Cooling
- 175°C Operating Temperature
- Repetitive Avalanche Capability for Robustness and Reliability
- Lead free, RoHS and Halogen free

$V_{(BR)DSS}$	<b>40V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>2.2mΩ</b>
	<b>3.0mΩ</b>
$I_D$ (Silicon Limited)	<b>112A</b>
$Q_g$	<b>52nC</b>



Applicable DirectFET Outline and Substrate Outline ①

<b>SB</b>	<b>SC</b>		<b>M2</b>	<b>M4</b>		<b>L4</b>	<b>L6</b>	<b>L8</b>	
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### Description

The AUIRL7736M2 combines the latest Automotive HEXFET® Power MOSFET Silicon technology with the advanced DirectFET® packaging technology to achieve exceptional performance in a package that has the footprint of an SO-8 or 5X6mm PQFN and only 0.7mm profile. The DirectFET® package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET® package allows dual sided cooling to maximize thermal transfer in automotive power systems.

This HEXFET® Power MOSFET is designed for applications where efficiency and power density are of value. The advanced DirectFET® packaging platform coupled with the latest silicon technology allows the AUIRL7736M2 to offer substantial system level savings and performance improvement specifically in high frequency DC-DC, motor drive and other heavy load applications on ICE, HEV and EV platforms. The AUIRL7736M2 can be utilized together with the AUIRL7732S2 as a sync/control MOSFET pair in a buck converter topology. This MOSFET utilizes the latest processing techniques to achieve low on-resistance and low  $Q_g$  per silicon area. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for high current automotive applications.

### Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	40	V
$V_{GS}$	Gate-to-Source Voltage	± 16	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)④	112	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)④	79	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	179	
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)③	22	
$I_{DM}$	Pulsed Drain Current ⑦	450	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	63	W
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.5	
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ⑥	68	mJ
$E_{AS}(\text{tested})$	Single Pulse Avalanche Energy Tested Value ⑥	119	
$I_{AR}$	Avalanche Current ⑤	See Fig. 18a,18b,16,17	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ
$T_P$	Peak Soldering Temperature	260	°C
$T_J$	Operating Junction and	-55 to + 175	
$T_{STG}$	Storage Temperature Range		

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	60	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ③	20	—	
$R_{\theta JCan}$	Junction-to-Can ④⑩	—	2.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ④	0.42		W/°C

HEXFET® is a registered trademark of International Rectifier.


## Static Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)

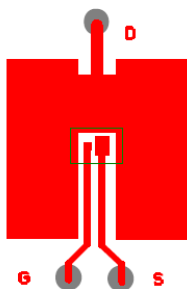
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.03	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.2	3.0	m $\Omega$	$V_{GS} = 10V, I_D = 67A$ ⑦
		—	3.2	4.3		$V_{GS} = 4.5V, I_D = 56A$ ⑧
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1.8	2.5	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-6.9	—	mV/ $^\circ\text{C}$	
$g_{fs}$	Forward Transconductance	152	—	—	S	$V_{DS} = 10V, I_D = 67A$
$R_G$	Gate Resistance	—	0.9	—	$\Omega$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	5	$\mu A$	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$

## Dynamic Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)

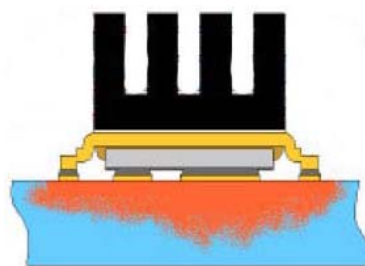
	Parameter	Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge	—	52	78	nC	$V_{DS} = 20V$ $V_{GS} = 4.5V$ $I_D = 67A$ See Fig.11
$Q_{gs1}$	Pre-Vth Gate-to-Source Charge	—	8.1	—		
$Q_{gs2}$	Post-Vth Gate-to-Source Charge	—	6.2	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	33	—		
$Q_{godr}$	Gate Charge Overdrive	—	4.7	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	39.2	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
$Q_{oss}$	Output Charge	—	31	—		
$t_{d(on)}$	Turn-On Delay Time	—	48	—	ns	$V_{DD} = 20V, V_{GS} = 4.5V$ ⑨ $I_D = 67A$ $R_G = 6.8\Omega$
$t_r$	Rise Time	—	210	—		
$t_{d(off)}$	Turn-Off Delay Time	—	56	—		
$t_f$	Fall Time	—	76	—		
$C_{iss}$	Input Capacitance	—	5055	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	960	—		
$C_{riss}$	Reverse Transfer Capacitance	—	525	—		
$C_{oss}$	Output Capacitance	—	3540	—		
$C_{oss}$	Output Capacitance	—	860	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	1306	—		

## Diode Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)

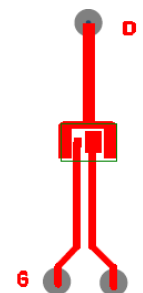
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	112	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ⑩	—	—	450		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$I_S = 67A, V_{GS} = 0V$ ⑦
$t_{rr}$	Reverse Recovery Time	—	32	48	ns	$I_F = 67A, V_{DD} = 20V$
$Q_{rr}$	Reverse Recovery Charge	—	23	35	nC	$di/dt = 100A/\mu s$ ⑦



③ Surface mounted on 1 in. square Cu (still air).



④ Mounted to a PCB with small clip heatsink (still air)



⑤ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

Notes ① through ⑩ are on page 11

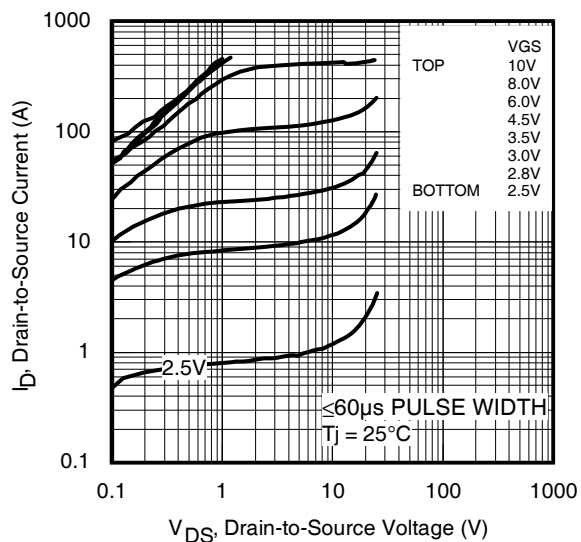
## Qualification Information<sup>†</sup>

<b>Qualification Level</b>		Automotive (per AEC-Q101) <sup>††</sup>	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		MEDIUM-CAN	MSL1, 260°C
<b>ESD</b>	Machine Model	Class M4 (+/- 400V) <sup>†††</sup> AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000V) <sup>†††</sup> AEC-Q101-001	
	Charged Device Model	N/A AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

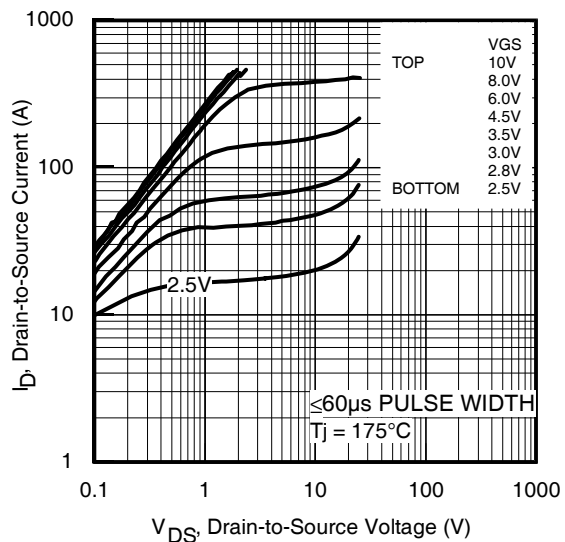
† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com>

†† Exceptions to AEC-Q101 requirements are noted in the qualification report.

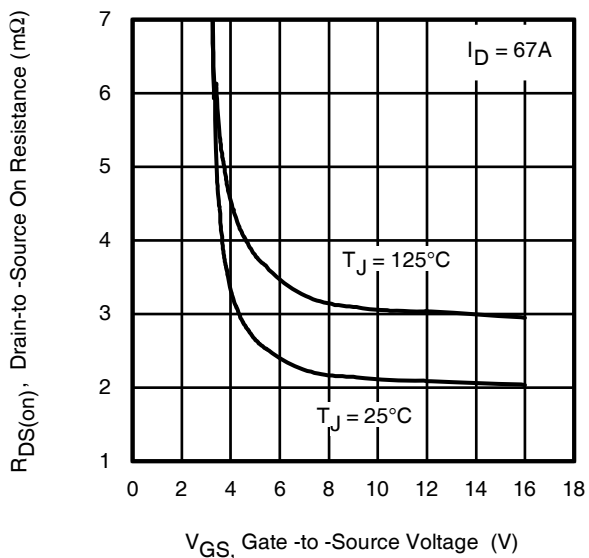
††† Highest passing voltage.



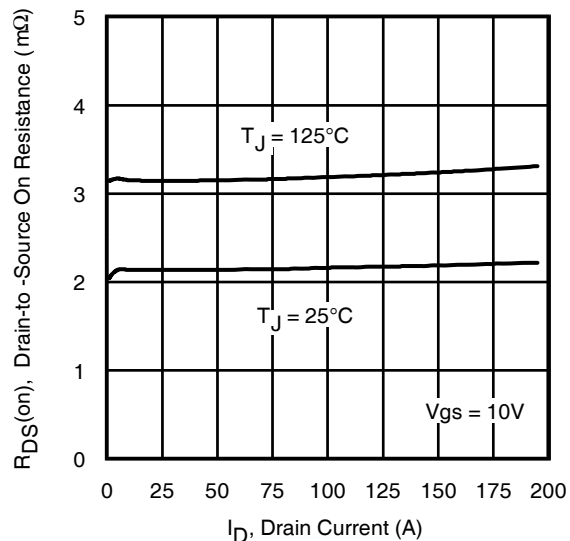
**Fig 1.** Typical Output Characteristics



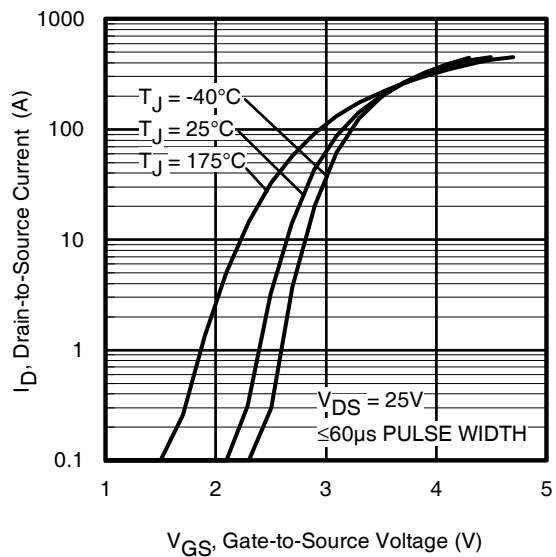
**Fig 2.** Typical Output Characteristics



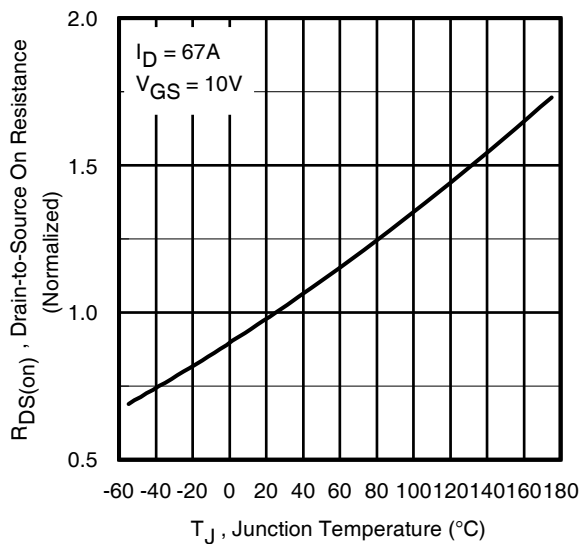
**Fig 3.** Typical On-Resistance vs. Gate Voltage



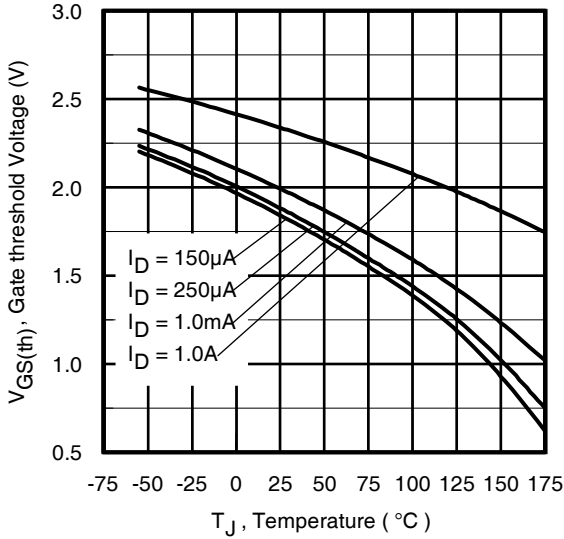
**Fig 4.** Typical On-Resistance vs. Drain Current



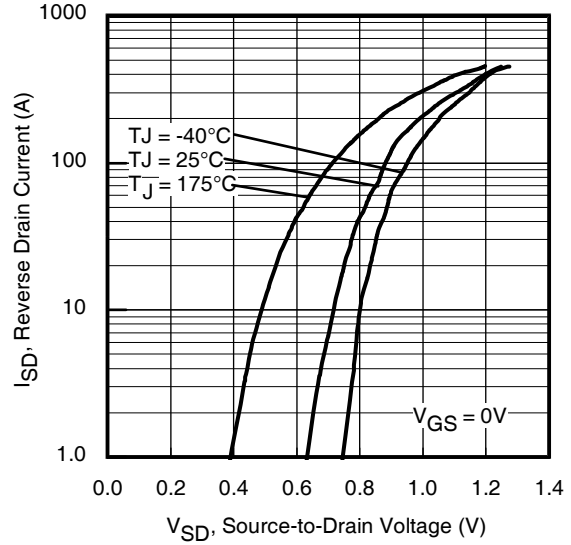
**Fig 5.** Typical Transfer Characteristics



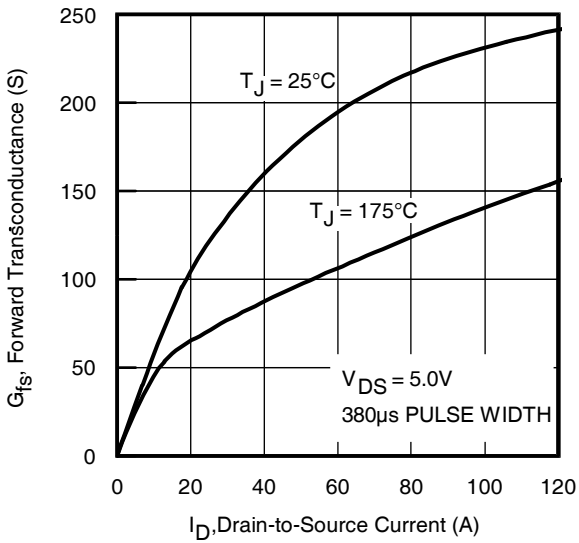
**Fig 6.** Normalized On-Resistance vs. Temperature



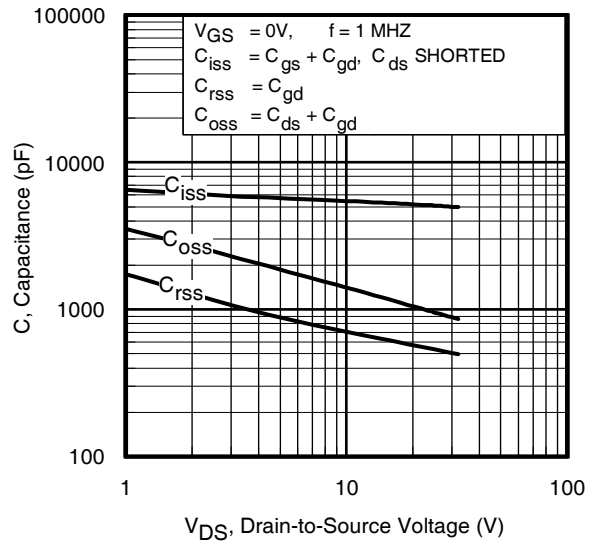
**Fig 7.** Typical Threshold Voltage vs. Junction Temperature



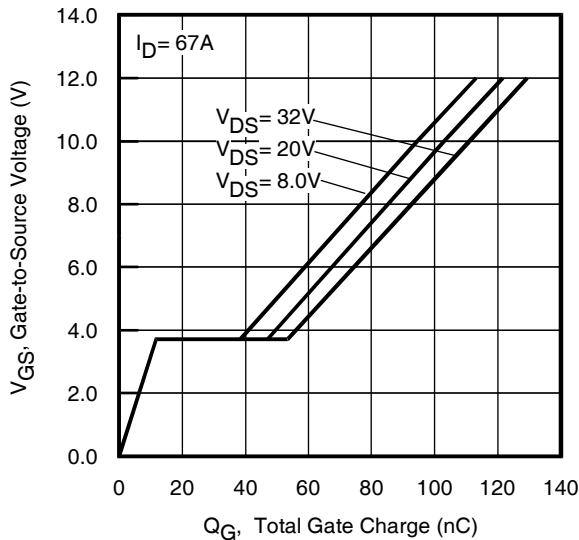
**Fig 8.** Typical Source-Drain Diode Forward Voltage



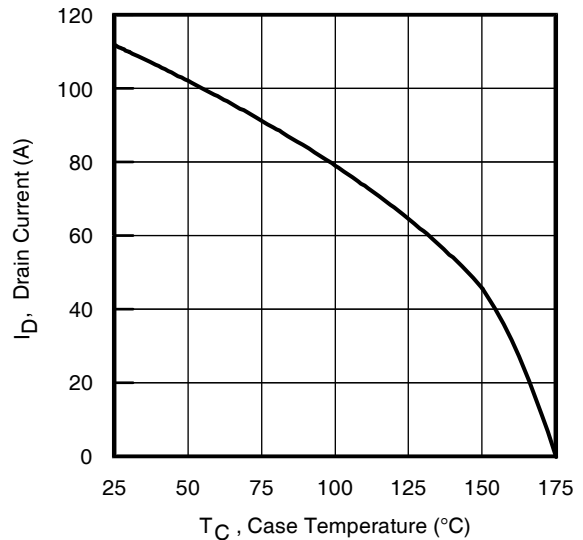
**Fig 9.** Typical Forward Transconductance Vs. Drain Current



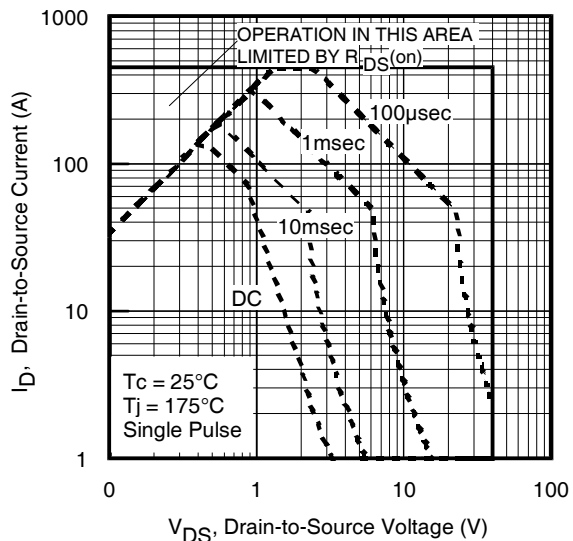
**Fig 10.** Typical Capacitance vs. Drain-to-Source Voltage



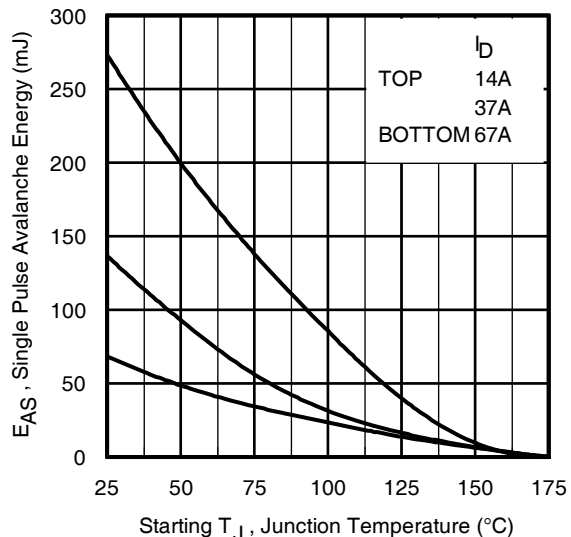
**Fig.11** Typical Gate Charge vs. Gate-to-Source Voltage  
www.irf.com



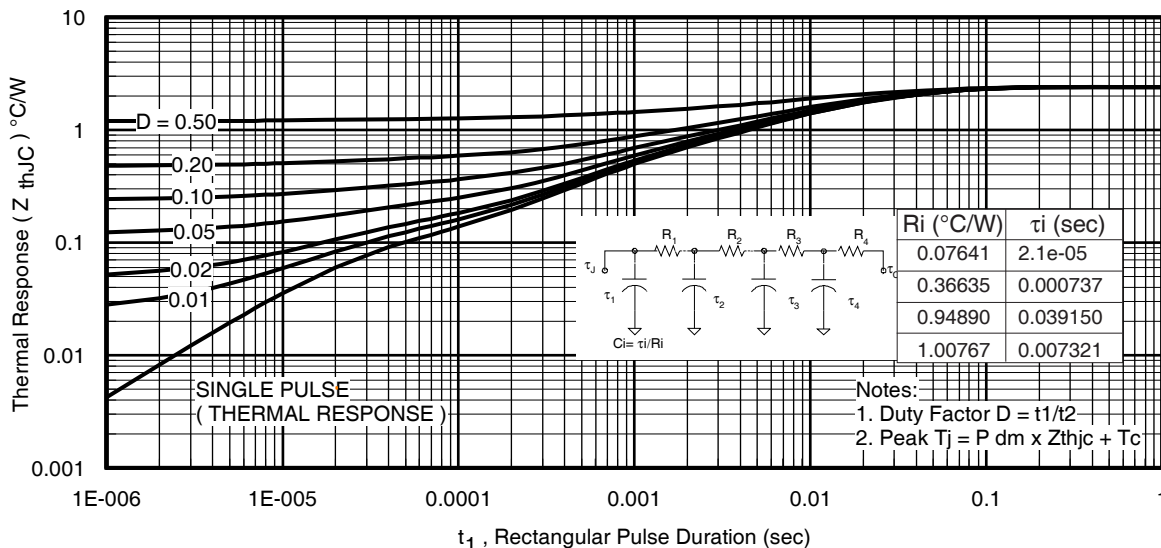
**Fig 12.** Maximum Drain Current vs. Case Temperature



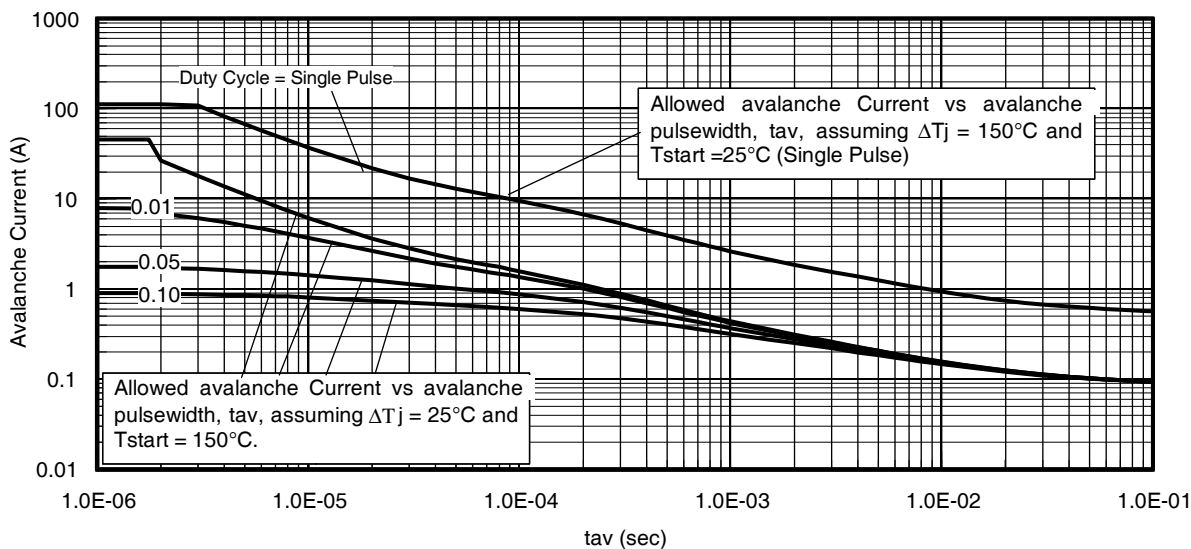
**Fig 13.** Maximum Safe Operating Area



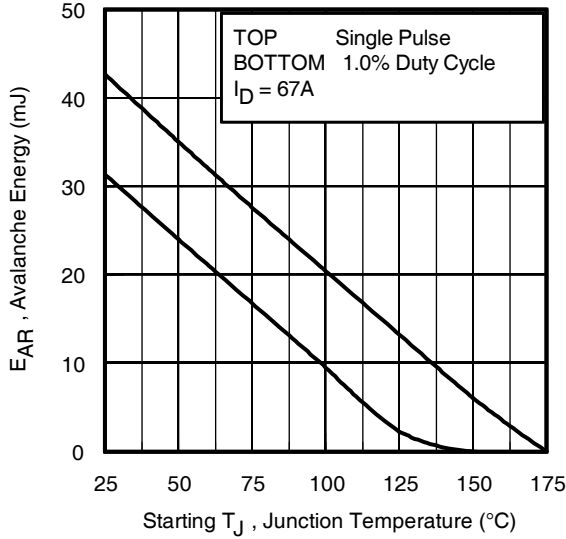
**Fig 14.** Maximum Avalanche Energy vs. Temperature



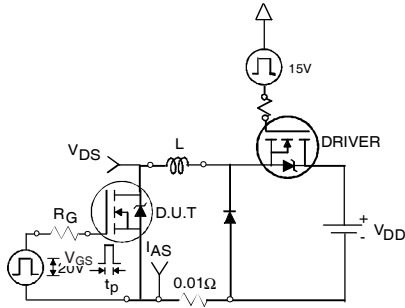
**Fig 15.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Fig 16.** Typical Avalanche Current vs. Pulsewidth



**Fig 17.** Maximum Avalanche Energy vs. Temperature

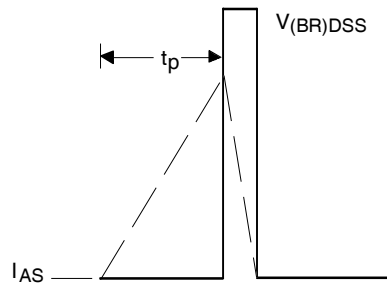


**Fig 18a.** Unclamped Inductive Test Circuit

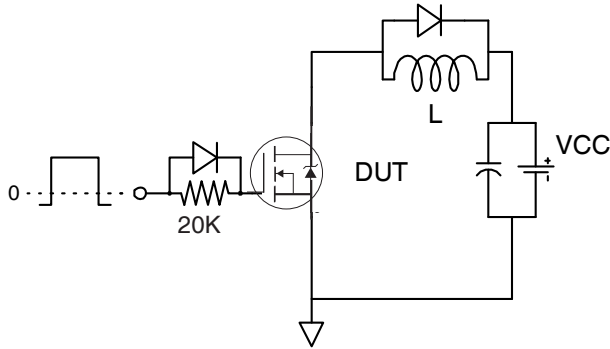
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) \cdot \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

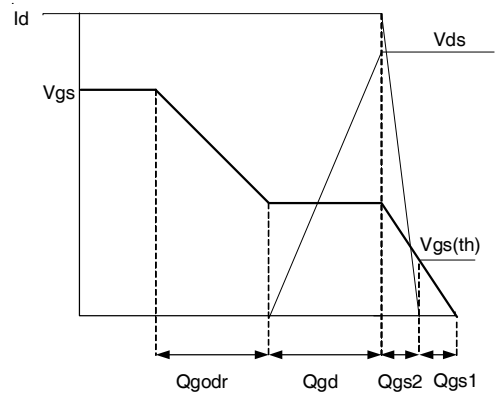
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



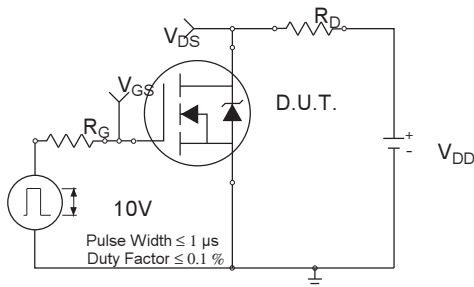
**Fig 18b.** Unclamped Inductive Waveforms



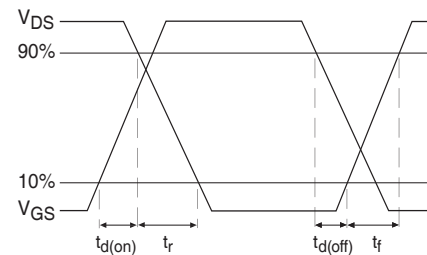
**Fig 19a.** Gate Charge Test Circuit



**Fig 19b.** Gate Charge Waveform



**Fig 20a.** Switching Time Test Circuit



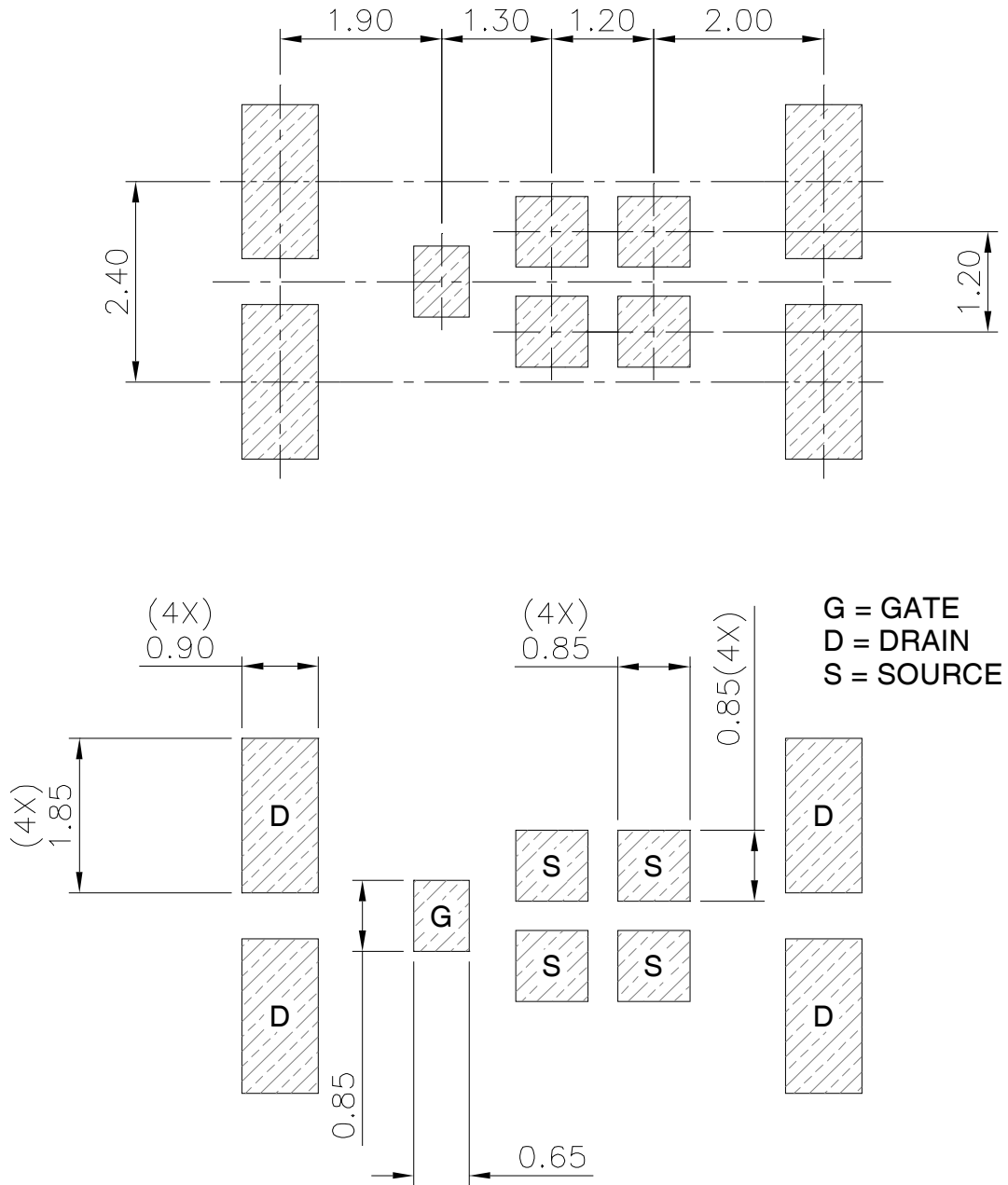
**Fig 20b.** Switching Time Waveforms

**Notes on Repetitive Avalanche Curves , Figures 16, 17:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 16, 17).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 15)

## DirectFET® Board Footprint, M4 (Medium Size Can).

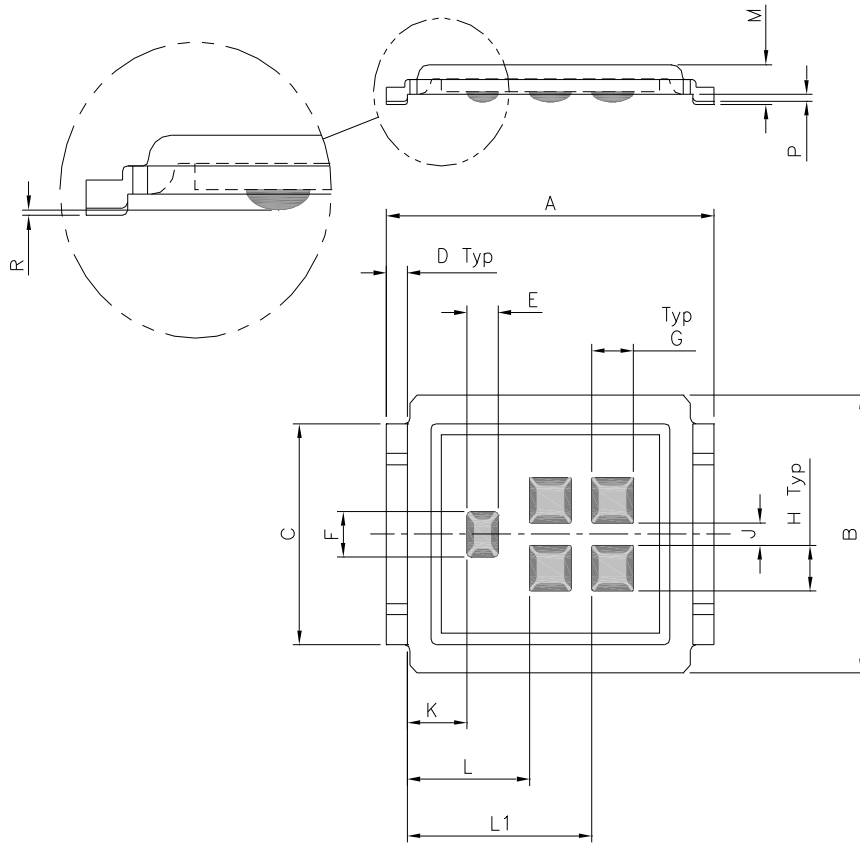
Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations





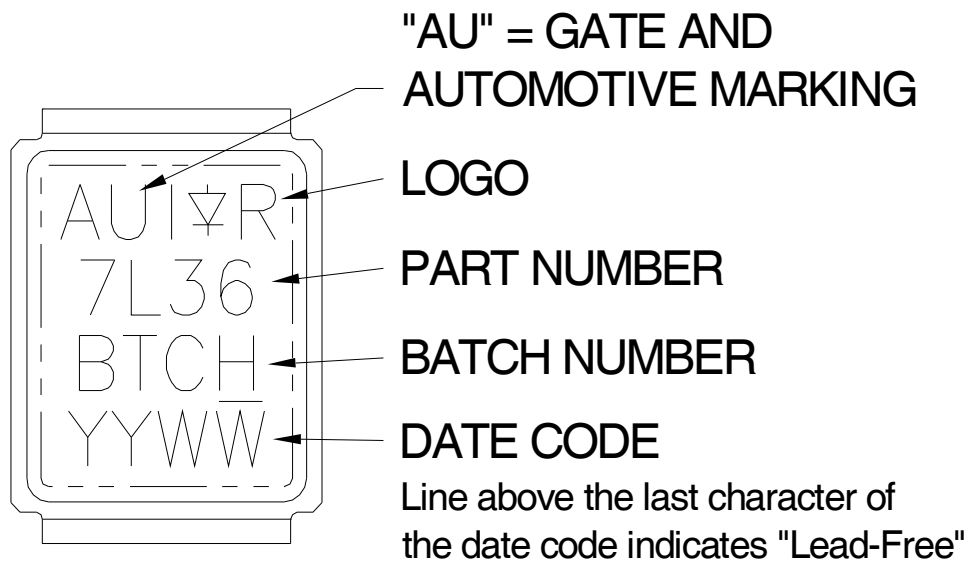
## DirectFET® Outline Dimension, M4 Outline (Medium Size Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations



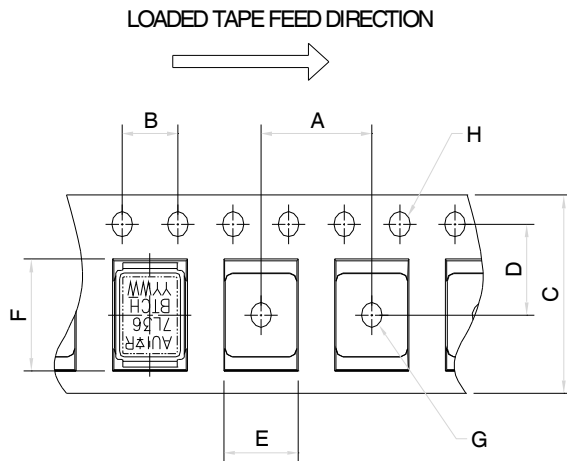
CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	0.78	0.82	0.031	0.032
G	0.78	0.82	0.031	0.032
H	0.78	0.82	0.031	0.032
J	0.38	0.42	0.015	0.017
K	1.10	1.20	0.043	0.047
L	2.30	2.40	0.090	0.094
L1	3.50	3.60	0.138	0.142
M	0.68	0.74	0.027	0.029
P	0.09	0.17	0.003	0.007
R	0.02	0.08	0.001	0.003

## DirectFET® Part Marking



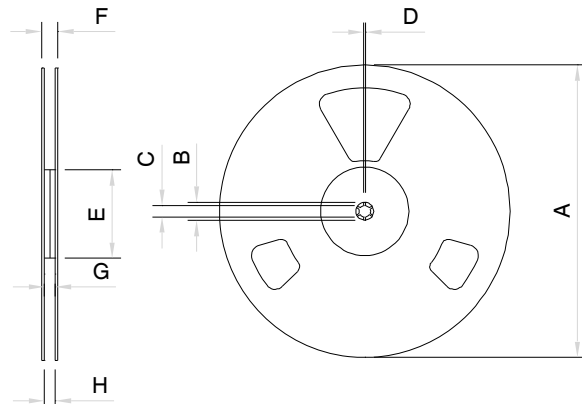
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## DirectFET® Tape & Reel Dimension (Showing component orientation).



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	NC	0.059	NC
H	1.50	1.60	0.059	0.063



NOTE: Controlling dimensions in mm  
Std reel quantity is 4800 parts. (ordered as AUIRL7736M2TR). For 1000 parts on 7" reel, order AUIRL7736M2TR1

CODE	REEL DIMENSIONS							
	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

### Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④  $T_C$  measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.

- ⑥ Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.030\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 67\text{A}$ ,  $V_{GS} = 20\text{V}$ .
- ⑦ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑧ Used double sided cooling, mounting pad with large heatsink.
- ⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑩  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

## IMPORTANT NOTICE

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IR warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with IR's standard warranty. Testing and other quality control techniques are used to the extent IR deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

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