AKD4683-B
AK4683 Evaluation Board Rev.0

FEATURE

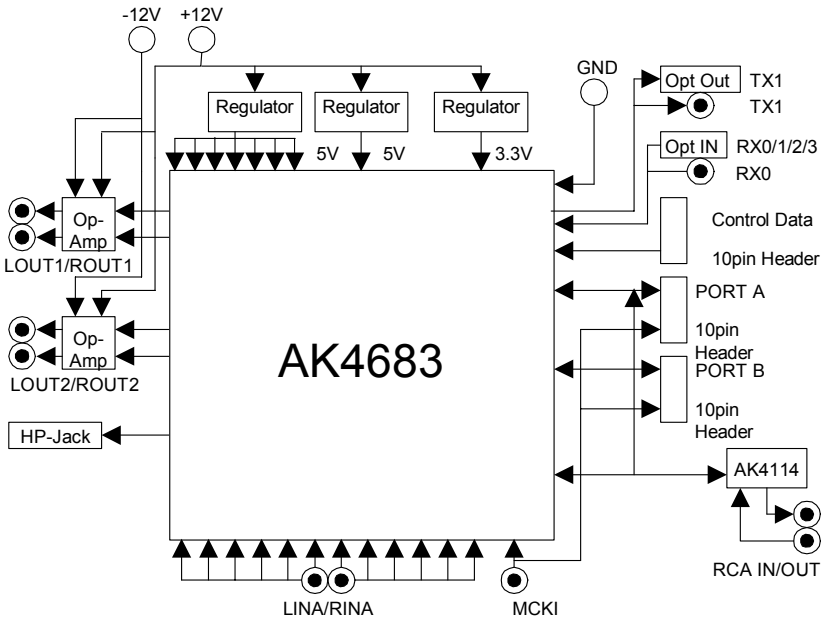
AKD4683-B is an evaluation board for AK4683, a single chip 24bit CODEC that has two channels of ADC and four channels of DAC with internal DIR, DIT. This board has interfaces with AKM's evaluation boards for A/D converter and D/A converter and makes easy to evaluate AK4683. Also this board has the digital audio interface and then achieves the interface with digital audio systems via opt-connector or RCA connector.

■ Ordering guide

AKD4683-B --- AK4683 Evaluation Board
10 wire flat cable for connection with printer port of PC (IBM-AT compatible machine), control software for AK4683, driver for control software on Windows 2000/XP are packed with this.
Control software does not work on Windows NT
Windows 2000/XP needs an installation of driver.
Windows 95/98/ME does not need an installation of driver.

FUNCTION

- ☐ **On-board clock generator (use AK4114)**
- ☐ **Compatible with 2 types of digital audio interface**
  - **Optical output/input and RCA input/output**
  - **10pin header for interface with external data source (x2)**
- ☐ **RCA connector for clock input with external clock source**
- ☐ **10pin header for register control**



(Note) AK4114 has DIR, DIT and X'tal oscillator.
Figure 1. AKD4683-B Block Diagram
(* Circuit diagram and PCB layout are attached at the end of this manual.)

EVALUATION BOARD MANUAL

■ Operating sequence

(1) **Set up power supply lines.**
[+12V] (Orange) = +12V
[-12V] (Blue) = -12V
[AVSS1] (Black) = 0V
[AVSS2] (Black) = 0V
[DVSS] (Black) = 0V
[PVSS] (Black) = 0V
[HVSS] (Black) = 0V
[DGND] (Black) = 0V

Each supply line should be distributed from the power supply unit.

(2) **Set up evaluation mode and jumper pins.** (Refer to the following item.)

(3) **Connect cables.** (Refer to the following item.)

(4) **Power on.**
The AK4683 should be reset once bringing PDN (SW3) "L" upon power-up.

(5) **Set up control software registers.** (Refer to the following item.)

■ Evaluation modes

(1) DAC with internal DIR

1. Connection of connector

In case of digital input through RX0, optical connector PORT5 (TORX176) or RCA connector J14 (RX0) are available. In case of digital input through RX1, RX2 or RX3, only the optical connector PORT5 is available.

2. Setting of jumper pin

RX0 and RX1-3 should not select optical connector at the same time.
In case of digital input through RX1, RX2 or RX3, set jumpers JP32 (RX1), JP34 (RX2) or JP36 (RX3) as Table 2. Set unused channels to GND.

Connector	JP33 (RX0)	
Optical (PORT5)	OPT	Default
RCA (J14)	RCA	

Table 1. Set-up of RX0

Input	JP32 (RX1)	JP34 (RX2)	JP36 (RX3)
RX1	OPT	GND	GND
RX2	GND	OPT	GND
RX3	GND	GND	OPT

Table 2. Set-up of RX1, RX2, and RX3

3. Setting of toggle switch

Set SW1 (AK4114-PDN) to OFF.

(2) ADC with internal DIT

1. Connection of connector

For digital output, optical connector PORT3 (TOTX176) or RCA connector J13 (TX1) are available.

2. Setting of jumper pin

JP30 (TX1) controls digital output (optical connector PORT3 or RCA connector J13).

Connector	JP30(TX)
Optical (PORT3)	OPT
RCA (J13)	RCA

Default

Table 3. Set-up of TX

3. Setting of toggle switch

Set SW1 (AK4114-PDN) to OFF.

(3) DAC with external DIR

1. Connection of connector

For digital input, RCA connector J10 (AK4114-RX0) is available.

2. Setting of jumper pin

Setting of interface signal of PORTA/PORTB: AK4114 (U5) is as follows.
(Default input of PORTA is SDTIA1.)

PORT	JP22 (BICKA)	JP24 (OLRCKA)	JP16 (ILRCKA)	JP17 (SDTIA1)	JP19 (SDTIA2)	JP20 (SDTIA3)
PORTA	Short	Open	Short	DIR	GND	GND
PORTB	Open	Open	Open	GND	GND	GND

Table 4. Set-up of AK4114 interface (1/2)

PORT	JP27 (BICKB)	JP28 (LRCKB)	JP25 (SDTIB)	JP21 (MCLK-SEL)	JP29 (MCLK)	JP15 (XTIA)	JP23 (SDTO)
PORTA	Open	Open	GND	MCKO1	Open	Open	SDTOA
PORTB	Short	Short	DIR	MCKO1	Open	Open	SDTOB

Table 5. Set-up of AK4114 interface (2/2)

3. Setting of toggle switch

Set SW1 (AK4114-PDN) to ON.

4. Setting of DIP switch

Set SW2 (PORTA-DIR/4683): 2pin (DIF1) to OFF.

(4) ADC with external DIT

1. Connection of connector

For digital output, RCA connector J11 (AK4114-TX1) is available.

2. Setting of jumper pin

Setting of interface signal of PORTA/PORTB: AK4114 (U5) is as follows.

PORT	JP22 (BICKA)	JP24 (OLRCKA)	JP16 (ILRCKA)	JP17 (SDTIA1)	JP19 (SDTIA2)	JP20 (SDTIA3)
PORTA	Short	Short	Open	GND	GND	GND
PORTB	Open	Open	Open	GND	GND	GND

Table 6. Set-up of AK4114 interface (1/2)

PORT	JP27 (BICKB)	JP28 (LRCKB)	JP25 (SDTIB)	JP21 (MCLK-SEL)	JP29 (MCLK)	JP15 (XTIA)	JP23 (SDTO)
PORTA	Open	Open	GND	Open	Open	Short	SDTOA
PORTB	Short	Short	GND	Open	Open	Short	SDTOB

Table 7. Set-up of AK4114 interface (2/2)

3. Setting of toggle switch

Set SW1 (AK4114-PDN) to ON.

4. Setting of DIP switch

Set SW2 (PORTA-DIR/4683): 4pin (CM0) to ON.

(5) Internal loop back (Analog input → ADC → DAC → Analog output)

1. Connection of connector

For analog input, RCA connector J3 (LINA)/ J6 (RINA) are available.
For analog output, RCA connector J1 (LOUT1)/ J4 (ROUT1), J2 (LOUT2)/ J5 (ROUT2) are available.

2. Setting of jumper pin

Input	JP1 (LIN1)/ JP7 (RIN1)	JP2 (LIN2)/ JP8 (RIN2)	JP3 (LIN3)/ JP9 (RIN3)	JP4 (LIN4)/ JP10 (RIN4)	JP5 (LIN5)/ JP11 (RIN5)	JP6 (LIN6)/ JP12 (RIN6)	
LIN1/ RIN1	LINA/ RINA	Open	Open	Open	Open	Open	(Default)
LIN2/ RIN2	Open	LINA/ RINA	Open	Open	Open	Open	
LIN3/ RIN3	Open	Open	LINA/ RINA	Open	Open	Open	
LIN4/ RIN4	Open	Open	Open	LINA/ RINA	Open	Open	
LIN5/ RIN5	Open	Open	Open	Open	LINA/ RINA	Open	
LIN6/ RIN6	Open	Open	Open	Open	Open	LINA/ RINA	

Table 8. Set-up of LINA/RINA

Input	JP1 (LIN1)/ JP7 (RIN1)	JP2 (LIN2)/ JP8 (RIN2)	JP3 (LIN3)/ JP9 (RIN3)	JP4 (LIN4)/ JP10 (RIN4)	JP5 (LIN5)/ JP11 (RIN5)	JP6 (LIN6)/ JP12 (RIN6)
LIN1/ RIN1	LINB/ RINB	Open	Open	Open	Open	Open
LIN2/ RIN2	Open	LINB/ RINB	Open	Open	Open	Open
LIN3/ RIN3	Open	Open	LINB/ RINB	Open	Open	Open
LIN4/ RIN4	Open	Open	Open	LINB/ RINB	Open	Open
LIN5/ RIN5	Open	Open	Open	Open	LINB/ RINB	Open
LIN6/ RIN6	Open	Open	Open	Open	Open	LINB/ RINB

Table 9. Set-up of LINB/RINB

3. Setting of toggle switch

Set SW1 (AK4114-PDN) to OFF.

■ Register control

AKD4683-B can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (uP-I/F) to PC by 10-line flat cable packed with this. Take care of the direction of connector. There is a mark at pin#1. The pin layout of PORT4 is as Figure 2.

Mode	SW2_8
4-wire Serial	L
I2C	H

Table 10. Set-up of Parallel mode and Serial mode

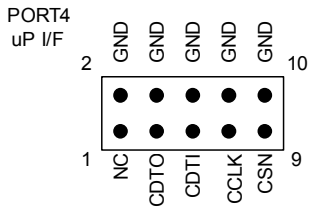


Figure 2. PORT4 pin layout

Control software is packed with this evaluation board. Software operation procedure is included in evaluation board manual.

■ Set-up DIP switch (SW2)

No.	Name	ON ("H")	OFF ("L")	Default
1	DIF0	Setting of AK4114 Audio Interface Format (Refer Table 12.)		OFF
2	DIF1			ON
3	DIF2			ON
4	CM0	Selection of AK4114 Clock Mode (Clock Source) (Refer Table 13.)		OFF
5	CM1			OFF
6	OCKS0	Selection of AK4114 Master Clock Output frequency (Refer Table 14.)		OFF
7	OCKS1			OFF
8	I2C	I^2C-bus control mode	4-wire serial control mode	OFF

Table 11. Set up modes of AK4114 (U5) and AK4683 (U1)

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
							I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	<Default>
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 12. AK4114 Audio Interface Format

Mode	CM1	CM0	UNLOCK	PLL	X'tal	Clock source	SDTO	
0	0	0	-	ON	ON (Note1)	PLL	RX	<Default>
1	0	1	-	OFF	ON	X'tal	DAUX	
2	1	0	0	ON	ON	PLL	RX	
			1	ON	ON	X'tal	DAUX	
3	1	1	-	ON	ON	X'tal	DAUX	

Table 13. AK4114 Clock Mode (Clock Source)

No.	OCKS1	OCKS0	MCKO1	MCKO2	X'tal	fs (max)	
0	0	0	256fs	256fs	256fs	96 kHz	<Default>
1	0	1	256fs	128fs	256fs	96 kHz	
2	1	0	512fs	256fs	512fs	48 kHz	
3	1	1	128fs	64fs	128fs	192 kHz	

Table 14. AK4114 Master Clock Output Frequency

■ Toggle switch

[SW3] (PDN): Switch for power down reset of AK4683 (U1). Keep "H" during operation of AK4683 (U1). Power down reset of AK4683 will be done by setting SW3 (PDN) to "L" once, after power on.

[SW1] (AK4114-PDN): Switch for power down reset of AK4114 (U5). Keep "H" during operation of AK4114 (U5). Power down reset of AK4114 (U5) will be done by setting SW1 to "L" once, after power on.

■ LED indication

[LE1] (INT): LED for output of AK4683 (U1): INT. It turns on when output of AK4683 (U1): INT is "H".

[LED1] (ERF): LED for output of AK4114 (U5): INT0.It turns on when output of AK4114 (U5): INT0 is "H".

■ Set up Jumper pins

Jumper	Evaluation Mode				
	1	2	3	4	5
JP1 (LIN1)	LINA	LINA	LINA	LINA	LINA
JP2 (LIN2)	Open	Open	Open	Open	Open
JP3 (LIN3)	Open	Open	Open	Open	Open
JP4 (LIN4)	Open	Open	Open	Open	Open
JP5 (LIN5)	Open	Open	Open	Open	Open
JP6 (LIN6)	Open	Open	Open	Open	Open
JP7 (RIN1)	RINA	RINA	RINA	RINA	RINA
JP8 (RIN2)	Open	Open	Open	Open	Open
JP9 (RIN3)	Open	Open	Open	Open	Open
JP10 (RIN4)	Open	Open	Open	Open	Open
JP11 (RIN5)	Open	Open	Open	Open	Open
JP12 (RIN6)	Open	Open	Open	Open	Open
JP15 (XTIA)	Open	Open	Open	Short	Open
JP16 (ILRCKA)	Short	Short	Short	Open	Short
JP17 (SDTIA1)	GND	GND	DIR	GND	GND
JP19 (SDTIA2)	GND	GND	GND	GND	GND
JP20 (SDTIA3)	GND	GND	GND	GND	GND
JP21 (MCLK-SEL)	Open	Open	MCKO1	Open	Open
JP22 (BICKA)	Short	Short	Short	Short	Short
JP23 (SDTO)	SDTOA	SDTOA	SDTOA	SDTOA	SDTOA
JP24 (OLRCKA)	Open	Open	Open	Short	Open
JP25 (SDTIB)	GND	GND	GND	GND	GND
JP27 (BICKB)	Open	Open	Open	Open	Open
JP28 (LRCKB)	Open	Open	Open	Open	Open
JP29 (MCLK)	Open	Open	Open	Open	Open
JP30 (TX)	OPT	OPT	OPT	OPT	OPT
JP32 (RX1)	GND	GND	GND	GND	GND
JP33 (RX0)	OPT	OPT	OPT	OPT	OPT
JP34 (RX2)	GND	GND	GND	GND	GND
JP35 (GND)	Short	Short	Short	Short	Short
JP36 (RX3)	GND	GND	GND	GND	GND

(Default)

■ Set up control software registers

After the reset, setting example files are available as follows in CD-ROM to set registers in each evaluation modes.

Evaluation Mode 1
ADC/DAC: ak4683_adc_dac_mode1.akr
DIR/DIT: ak4683_dir_dit_mode1.akr

Evaluation Mode 2
ADC/DAC: ak4683_adc_dac_mode2.akr
DIR/DIT: ak4683_dir_dit_mode2.akr

Evaluation Mode 3
ADC/DAC: ak4683_adc_dac_mode3.akr
DIR/DIT: ak4683_dir_dit_mode3.akr

Evaluation Mode 4
ADC/DAC: ak4683_adc_dac_mode4.akr
DIR/DIT: ak4683_dir_dit_mode4.akr

Evaluation Mode 5
ADC/DAC: ak4683_adc_dac_mode5.akr
DIR/DIT: ak4683_dir_dit_mode5.akr

■ Analog Input Circuit

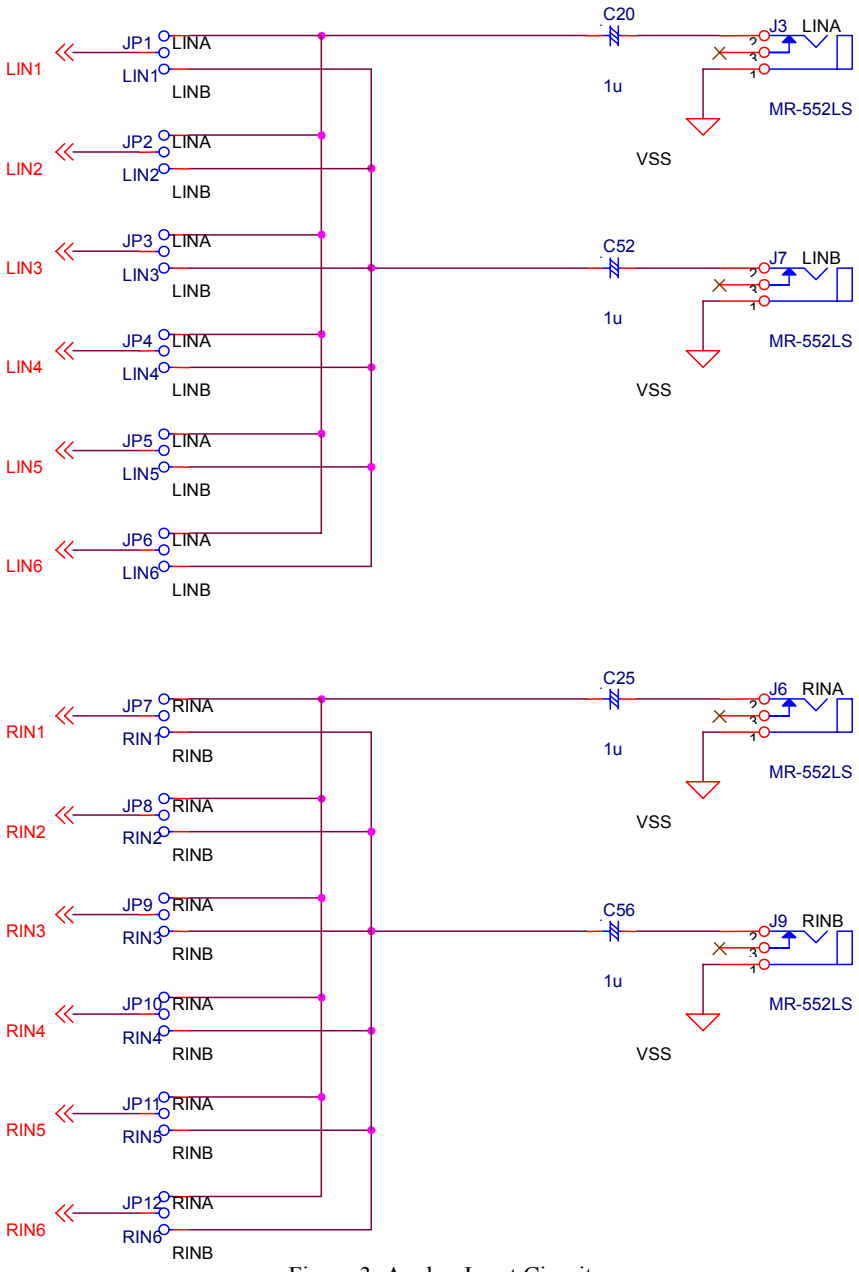


Figure 3. Analog Input Circuit

For analog input, RCA connector: J3 (LINA), J6 (RINA), J7 (LINB), J9 (RINB) are available to use.
Analog inputs are single-ended and input ranges of each channel are nominally 6.1Vpp@5V (R1~R12=47kΩ, R=14,15=24kΩ).

■ Analog Output Circuit

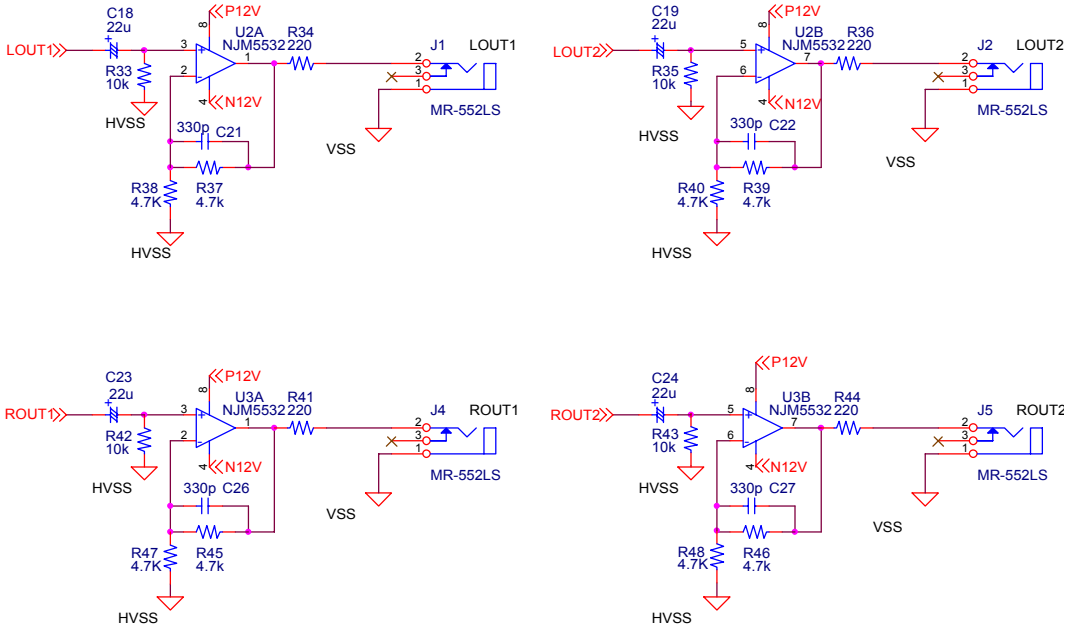


Figure 4. Analog Output Circuit

For analog output, RCA connector: J1 (LOUT1), J4 (ROUT1), J2 (LOUT2), J5 (ROUT2) are available to use.
Analog outputs are single-ended and output ranges of each channel are nominally 3.0Vpp@5V.
Output range: AOUT is proportional to AVDD2 (AOUT=0.6 x AVDD2=0.6 x 5=3.0).

■ Digital Input Circuit (Internal DIR)

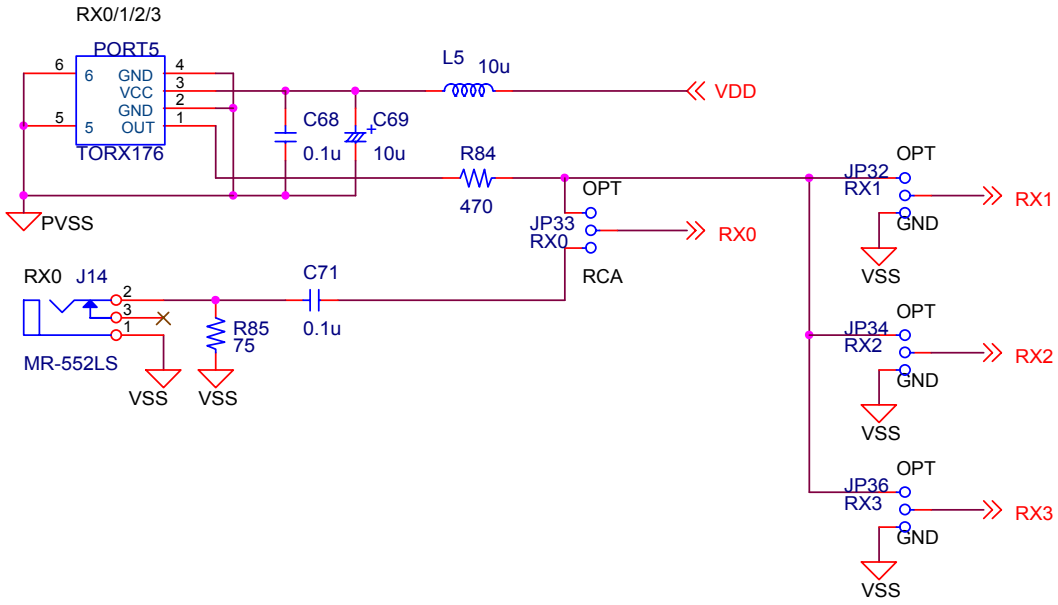


Figure 5. Digital Input Circuit (Internal DIR)

In case of input through RX0, optical connector PORT5 (TORX176) or RCA connector J14 (RX0) are available.
In case of input through RX1, RX2 or RX3, only the optical connector PORT5 is available.
Digital input: RX0, RX1, RX2 and RX3 is available to select overwriting IPS10 bit of control register (Addr=03H) of AK4683: DIR/DIT part by control software.

■ Digital Input Circuit (External DIR: PORT A)

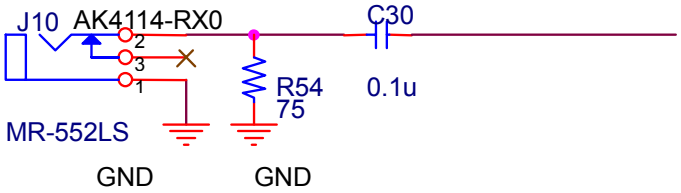


Figure 6. Digital Input Circuit (External DIR)

For digital input, RCA connector: J10 (AK4114-RX0) is available.

■ Digital Output Circuit (Internal DIT)

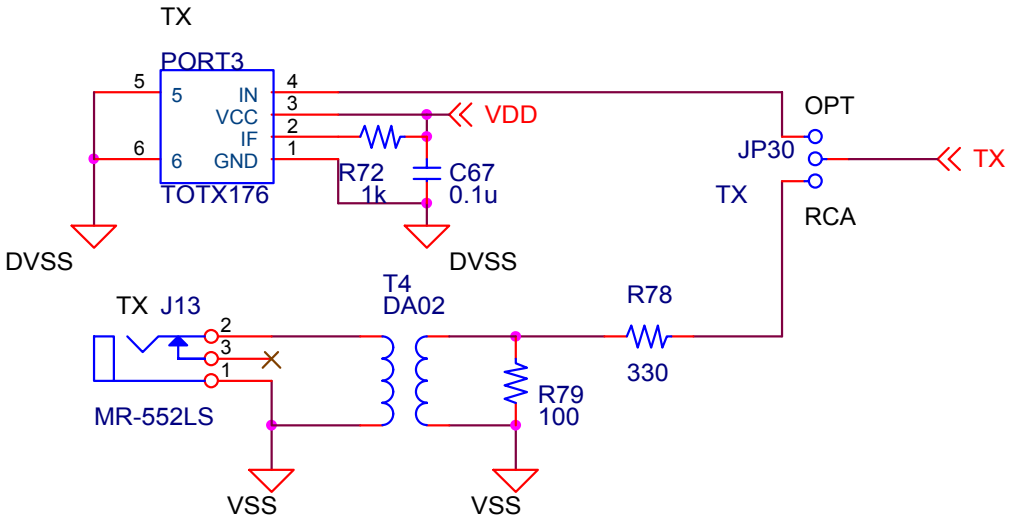


Figure 7. Digital Output Circuit (Internal DIT)

For digital output, optical connector PORT3 (TOTX176) or RCA connector J13 (TX1) are available.

■ Digital Output Circuit (External DIT)

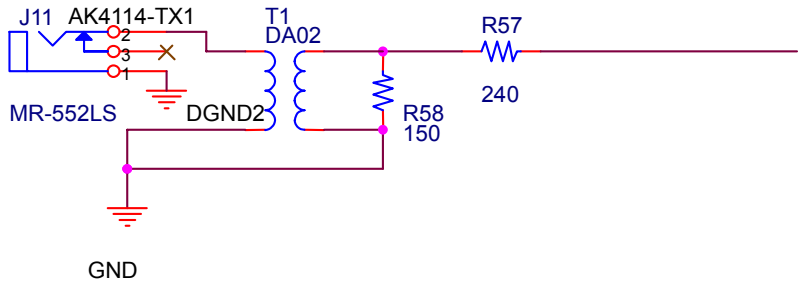


Figure 8. Digital Output Circuit (External DIT)

For digital output, RCA connector: J11 (AK4114-TX1) is available.

■ Headphone Output Circuit

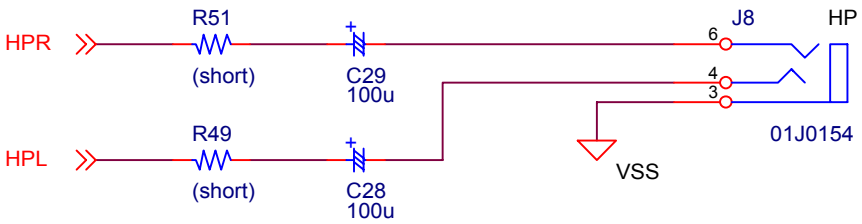


Figure 9. Headphone Output Circuit

For headphone output, stereo mini jack J8 (HP) are available.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4683-B according to previous term.

2. Connect IBM-AT compatible PC with AKD4683-B by 10-line type flat cable (packed with AKD4683-B). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4683-B Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive, and double-click the icon of "akd4683-b_adc_dac.exe"and "akd4683-b_dir_dit.exe", and set up the control program.
   akd4683-b_adc_dac.exe: AK4683 ADC/DAC control program
   akd4683-b_dir_dit.exe: AK4683 DIR/DIT control program

5. Then evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.

■ Explanation of each buttons

1. [Port Reset]: Set up the USB interface board (AKDUSBIF-A).
2. [Write default]: Initialize the registers.
3. [All Write]: Write all registers data that is currently displayed.
4. [Function1]: Dialog to write data by keyboard operation.
5. [Function2]: Dialog to write data by keyboard operation.
6. [Function3]: The sequence of register setting can be set and executed.
7. [Function4]: The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE]: Save the current register setting.
10. [OPEN]: Write the saved values to all register.
11. [Write]: Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog]: Dialog to evaluate ATT

This is a dialog corresponding to address: 0CH, 0DH, 0EH, 0FH, 10H, and 11H of AK4683.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to register by this interval.
Step Box: Data changes by this step.
Mode Select Box:

With checking this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

Without checking this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data to the file. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved to the file by [Save] is written to register. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

Set the control sequence.

Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step. This sequence can be saved and opened by [Save] and [Open] button on the [Function3] window. The extension of file name is “aks”.

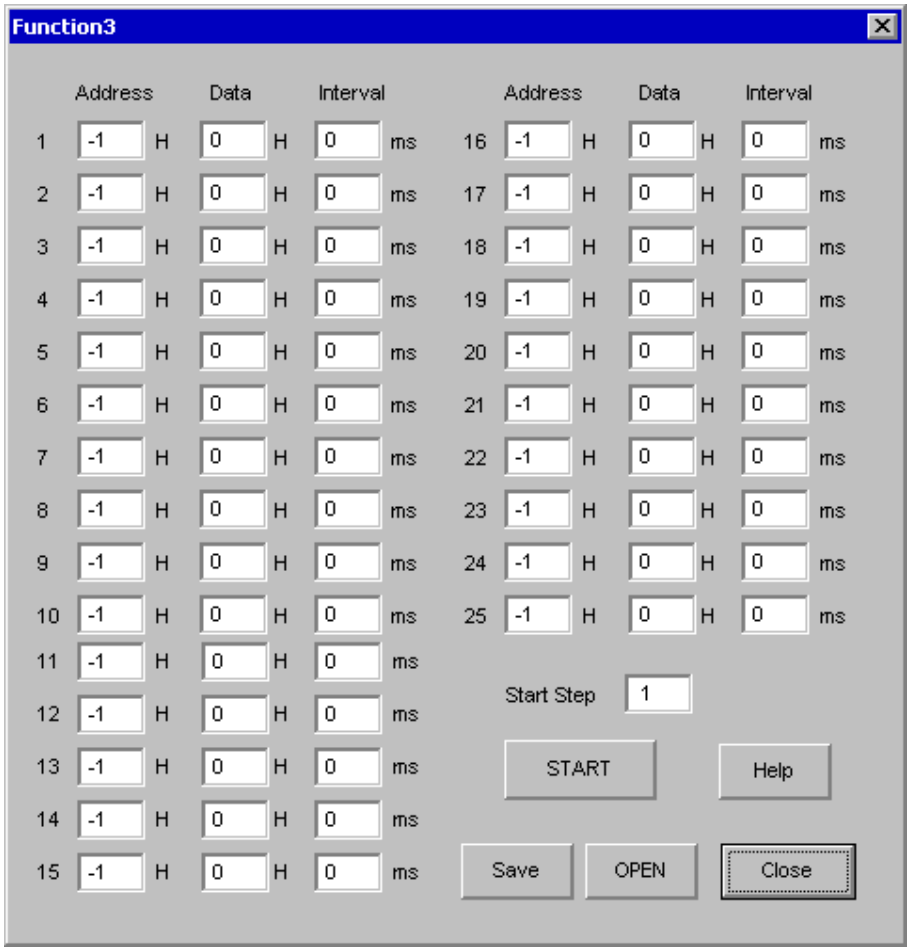


Figure 1. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

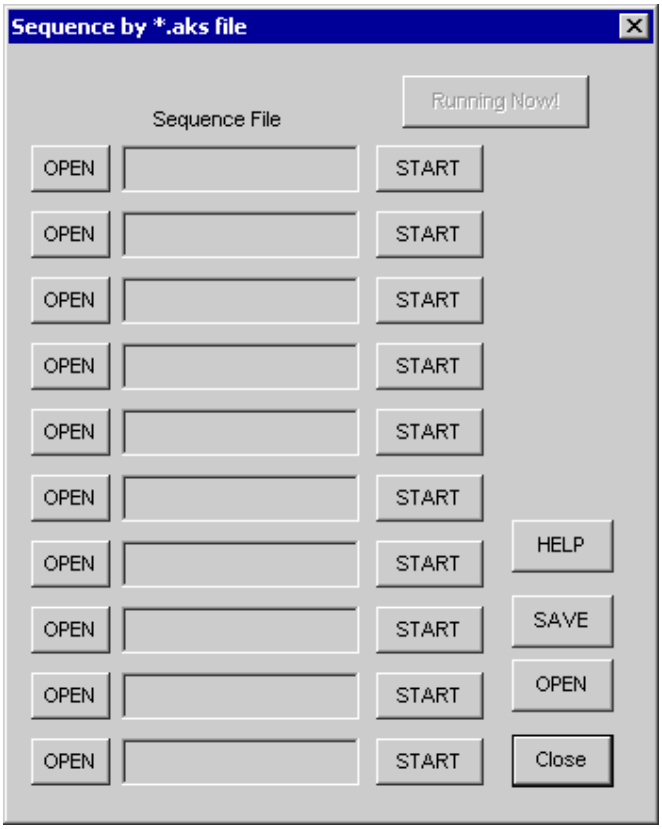


Figure 2. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 3.

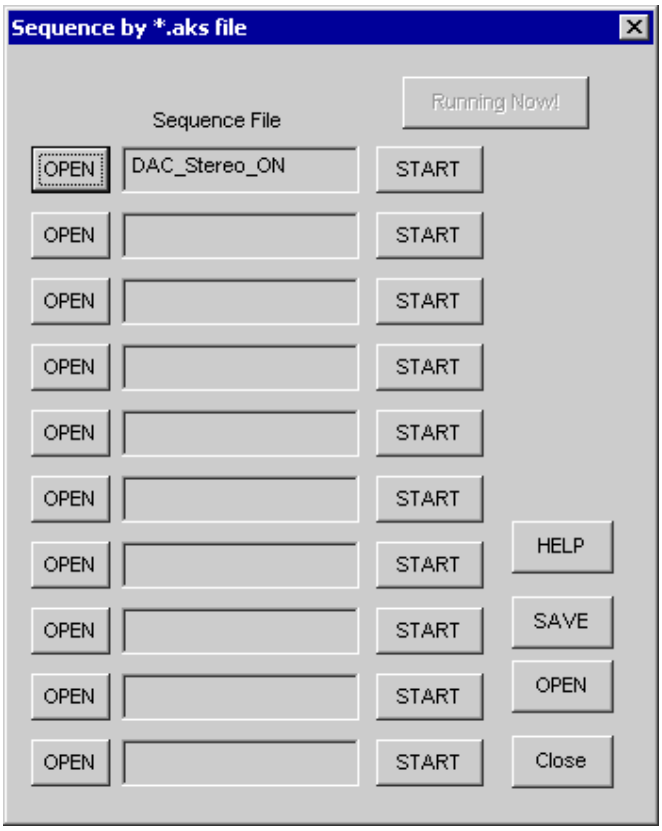


Figure 3. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The sequence file names can assign be saved. The file name is *.ak4.

[OPEN]: The sequence file names assign that are saved in *.ak4 are loaded.

6-3. Note

(1) [Function4] doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 4opens.

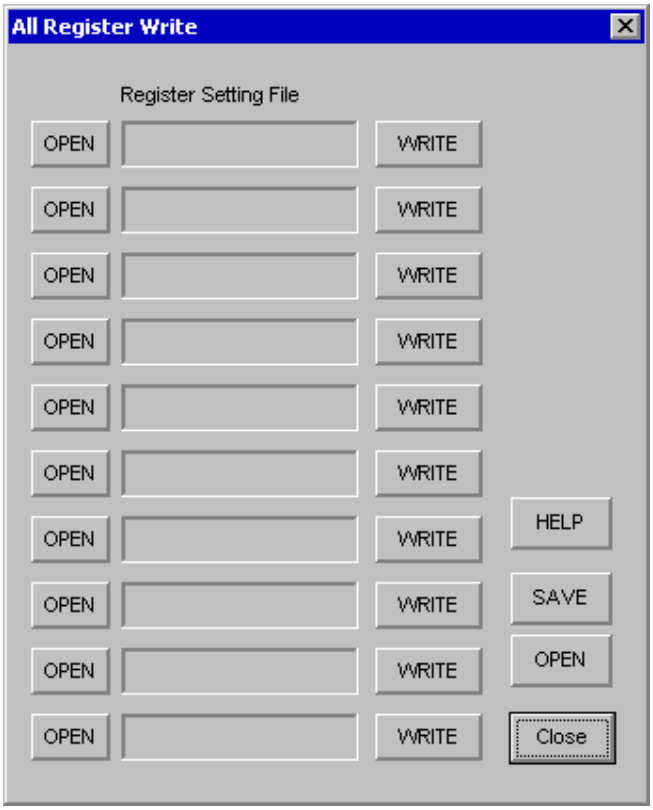


Figure 4. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

(2) Click [WRITE] button, then the register setting is executed.

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The register setting file names assign can be saved. The file name is *.ak5.

[OPEN]: The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

Measure Result

1) ADC part

[Measurement condition]

- Measurement unit: Audio Precision
- MCLK : 256fs (fs=48kHz, 96kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 20Hz~20kHz (fs=48kHz), 20Hz~40kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD1=AVDD2=DVDD=PVDD= TVDD=HVDD =5V,
- Interface : Internal DIT (fs=48kHz, 96kHz)
- Temperature : Room Temp

fs=48kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, -0.5dB	20kLPF	91.5 dB
DR	1kHz, -60dB	20kLPF	98.9 dB
DR	1kHz, -60dB	20kLPF, A-weighted	101.6 dB
S/N	No signal	20kLPF	99.0 dB
S/N	No signal	20kLPF, A-weighted	101.9 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, -0.5dB	fs/2	92.9 dB
DR	1kHz, -60dB	fs/2	98.0 dB
DR	1kHz, -60dB	20kLPF, A-weighted	103.1 dB
S/N	No signal	fs/2	98.0 dB
S/N	No signal	20kLPF, A-weighted	103.1 dB

2) DAC part

[Measurement condition]

- Measurement unit: Audio Precision
- MCLK : 256fs (fs=48kHz, 96kHz), 128fs (fs=192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- BW : 20Hz~20kHz (fs=48kHz), 20Hz~40kHz (fs=96kHz), 20Hz~40kHz (fs=192kHz)
- Resolution : 24bit
- Power Supply : AVDD1=AVDD2=DVDD=PVDD= TVDD=HVDD=5V
- Interface : Internal DIR (48kHz, 96kHz, 192kHz)
- Temperature : Room Temp

fs=48kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	20kLPF	98.0 dB
DR	1kHz, -60dB	20kLPF	103.7 dB
DR	1kHz, -60dB	22kLPF, A-weighted	105.8 dB
S/N	“0” data	20kLPF	103.4 dB
S/N	“0” data	22kLPF, A-weighted	106.0 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	40kLPF	96.5 dB
DR	1kHz, -60dB	40kLPF	102.0 dB
DR	1kHz, -60dB	22kLPF, A-weighted	105.8 dB
S/N	“0” data	40kLPF	101.0 dB
S/N	“0” data	22kLPF, A-weighted	106.0 dB

fs=192kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	40kLPF	96.8 dB
DR	1kHz, -60dB	40kLPF	102.5 dB
DR	1kHz, -60dB	22kLPF, A-weighted	105.8 dB
S/N	“0” data	40kLPF	101.2 dB
S/N	“0” data	22kLPF, A-weighted	105.8 dB

1.ADC

(ADC fs=48kHz)

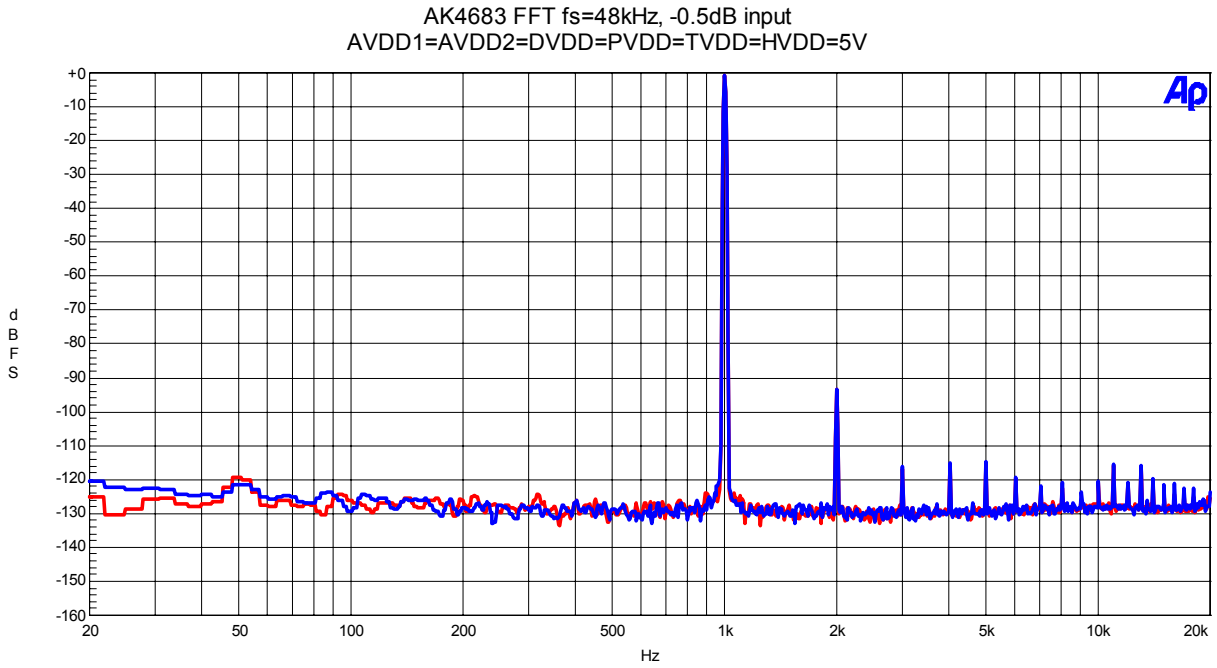


Figure 10. FFT(Input Frequency =1kHz,Input Level=-0.5dBFS)

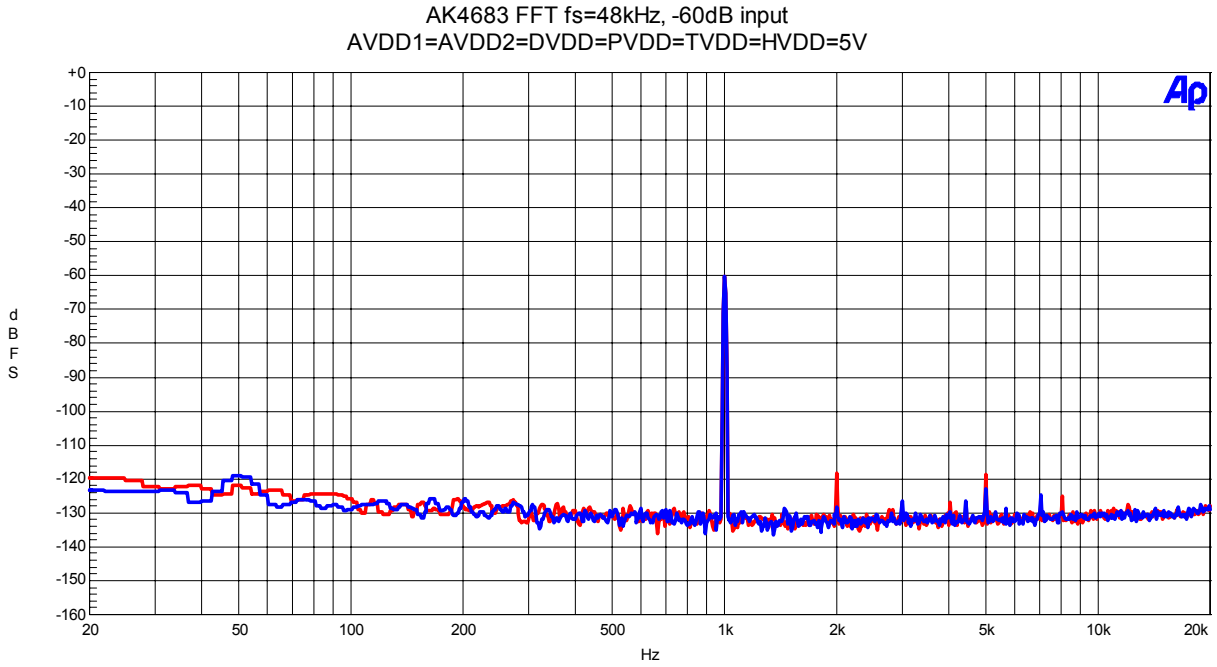


Figure 11. FFT(Input Frequency =1kHz,Input Level=-60dBFS)

(ADC fs=48kHz)

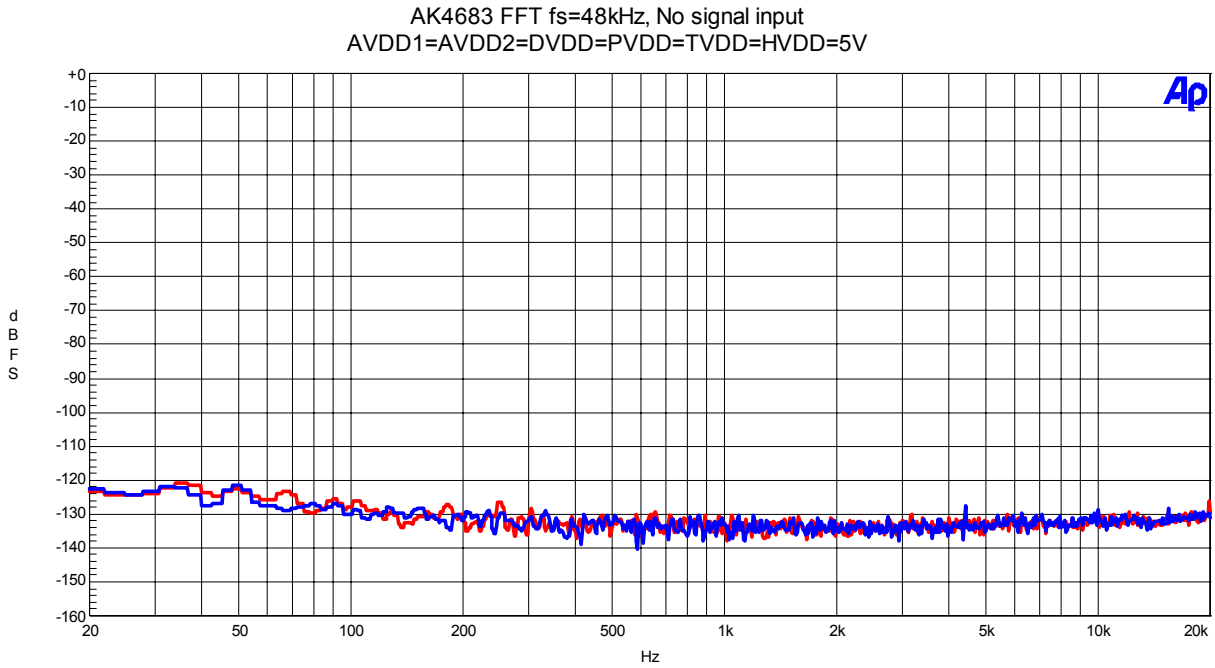


Figure 12. FFT(noise floor)

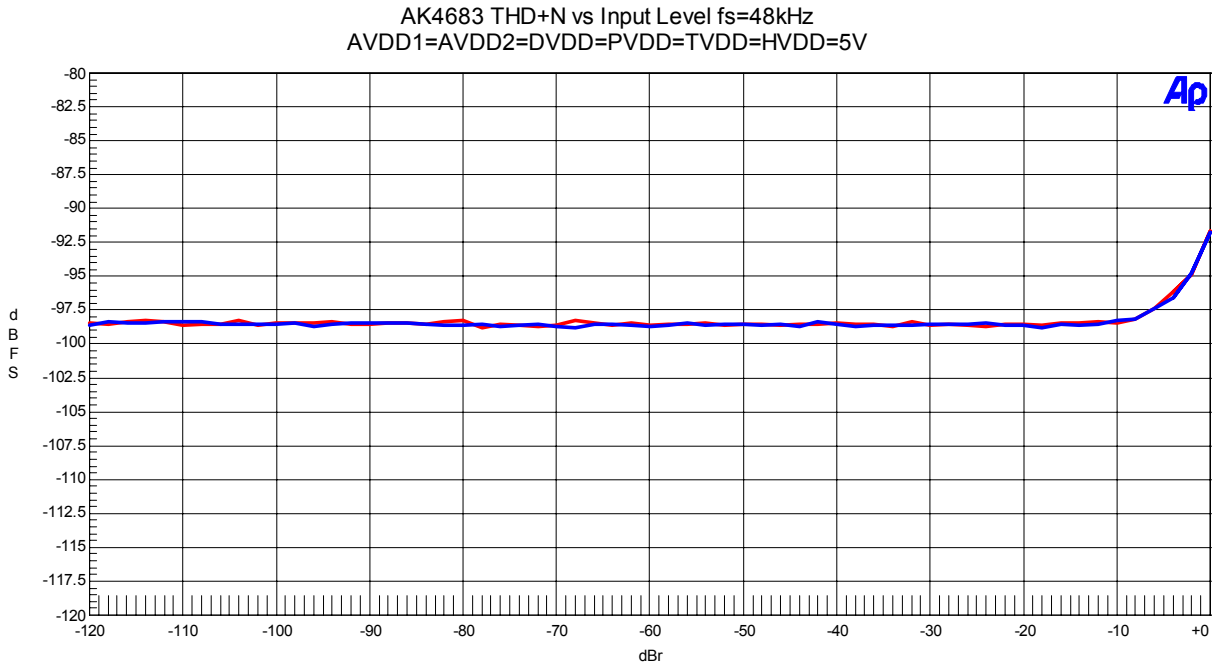


Figure 13. THD + N vs Input Level (Input Frequency =1kHz)

(ADC fs=48kHz)

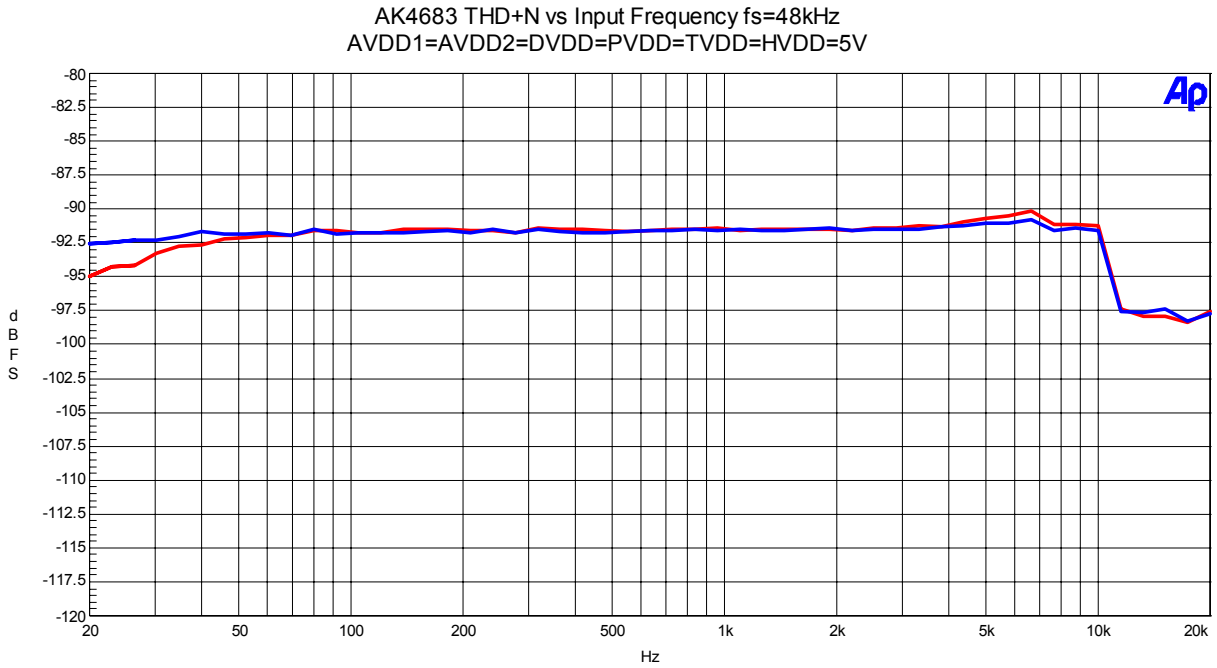


Figure 14. THD + N vs Input Frequency (Input Level=-0.5dBFS)

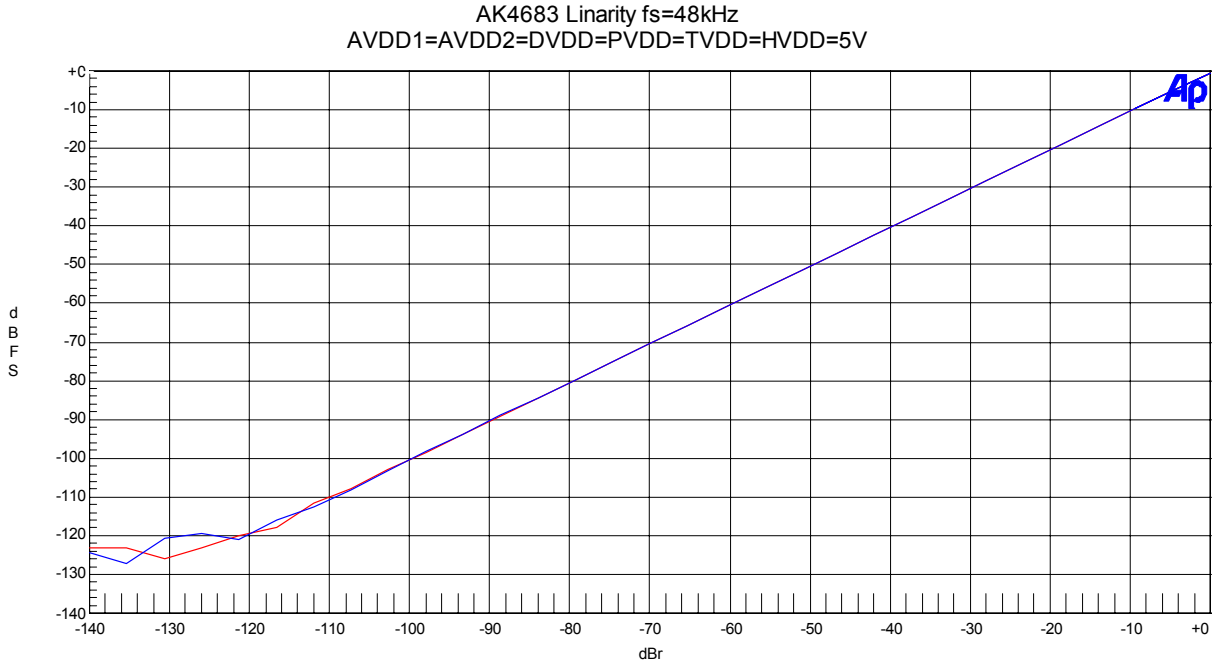


Figure 15. Linearity (Input Frequency =1kHz)

(ADC fs=48kHz)

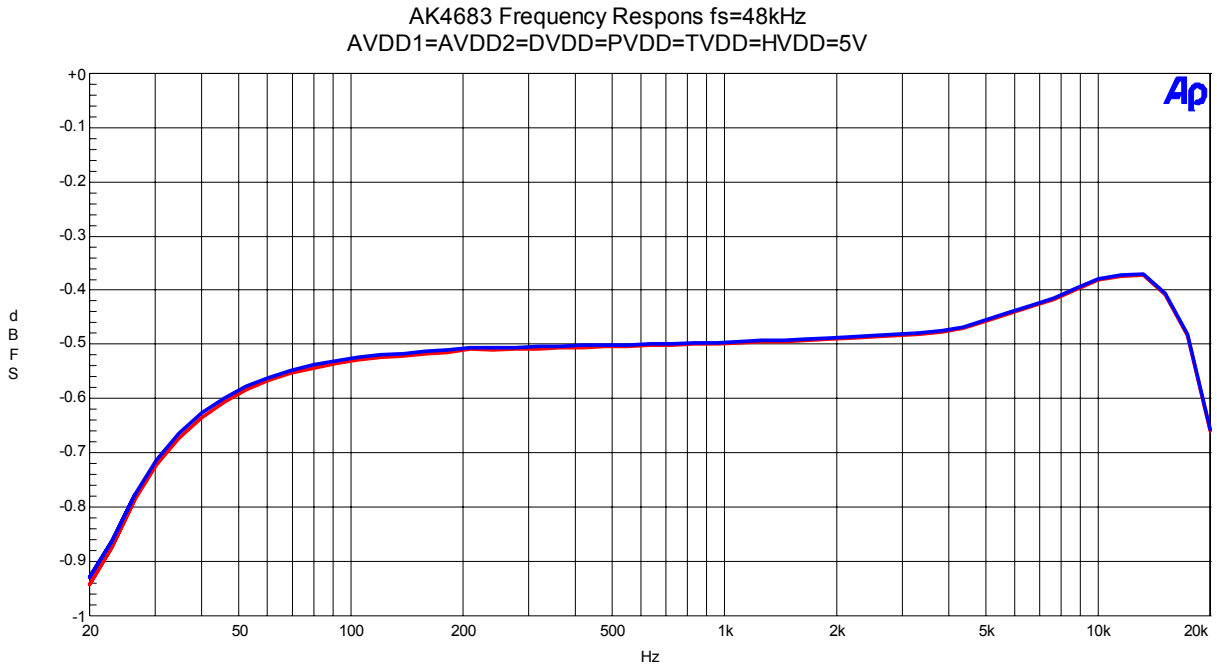


Figure 16. Frequency Response (Input Level=-0.5dBFS)

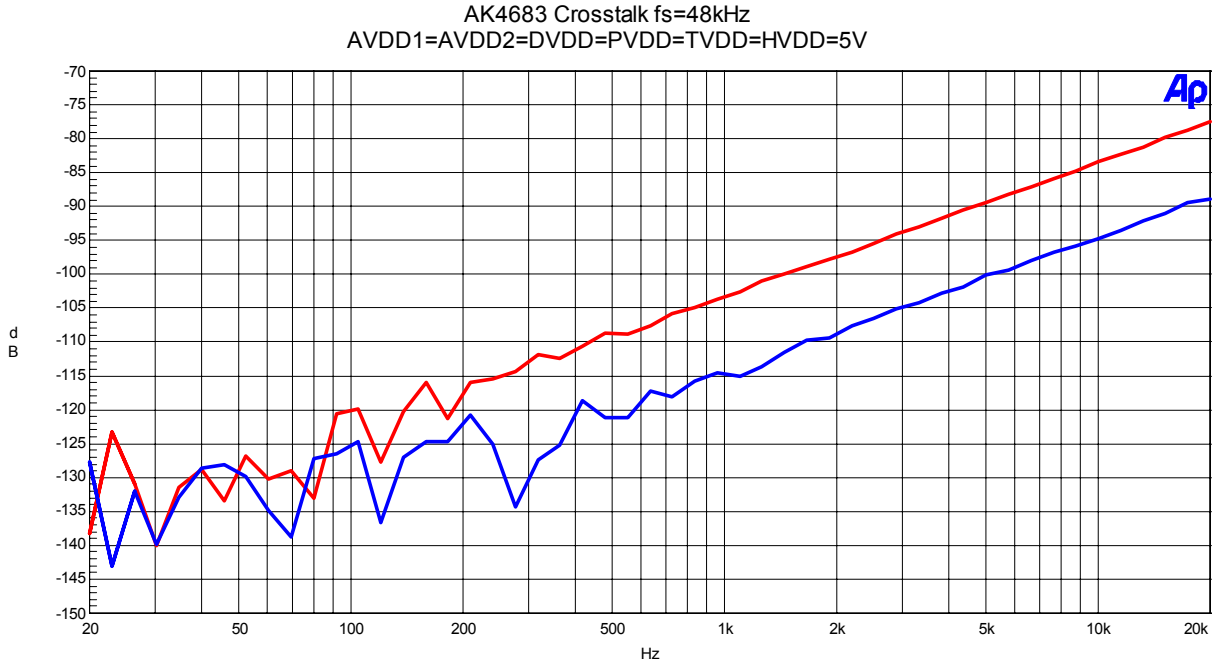


Figure 17. Crosstalk (Input Level=-0.5dBFS)

(ADC fs=96kHz)

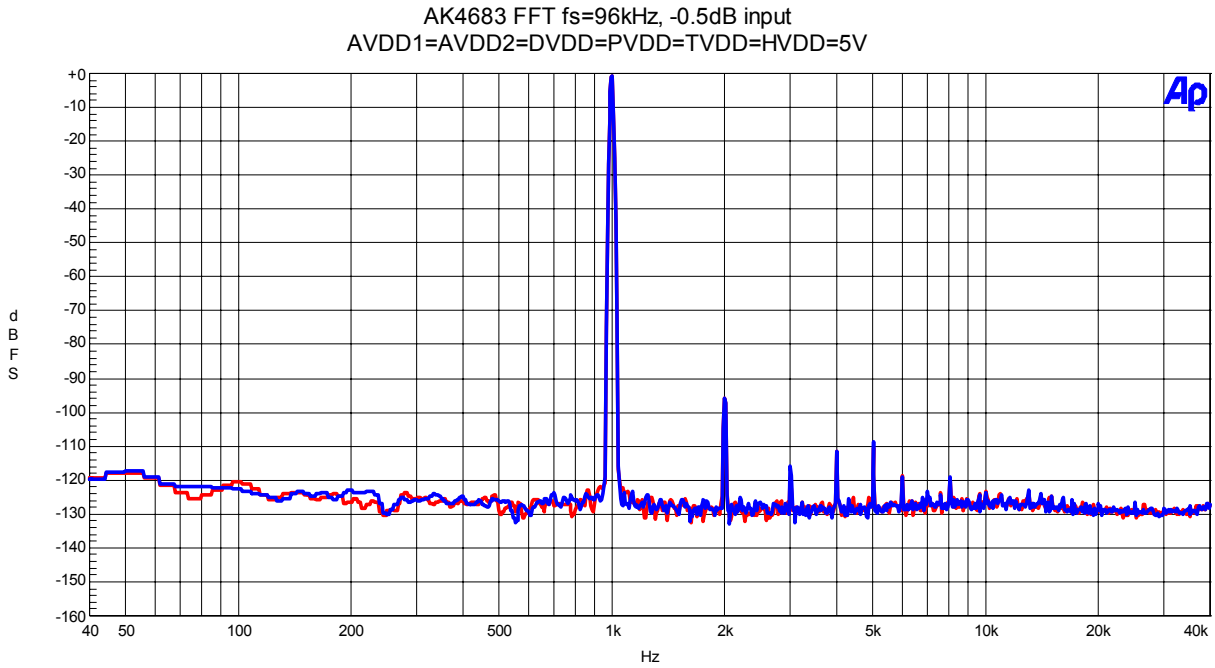


Figure 18. FFT(Input Frequency =1kHz,Input Level=-0.5dBFS)

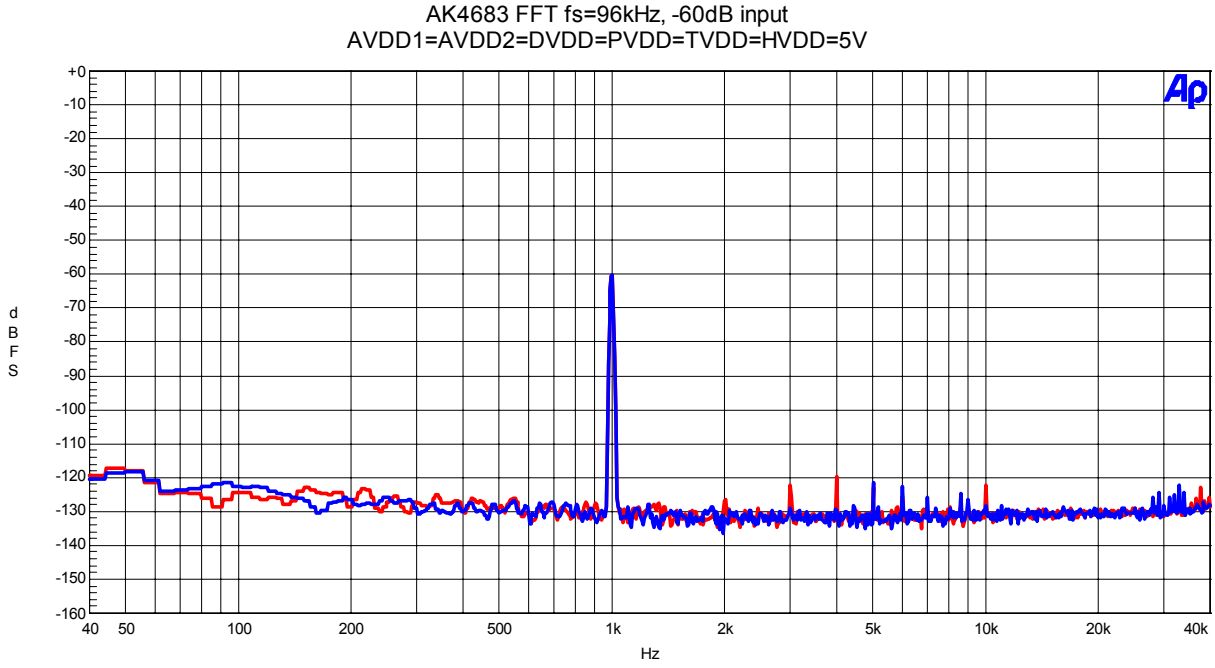


Figure 19. FFT(Input Frequency =1kHz,Input Level=-60dBFS)

(ADC fs=96kHz)

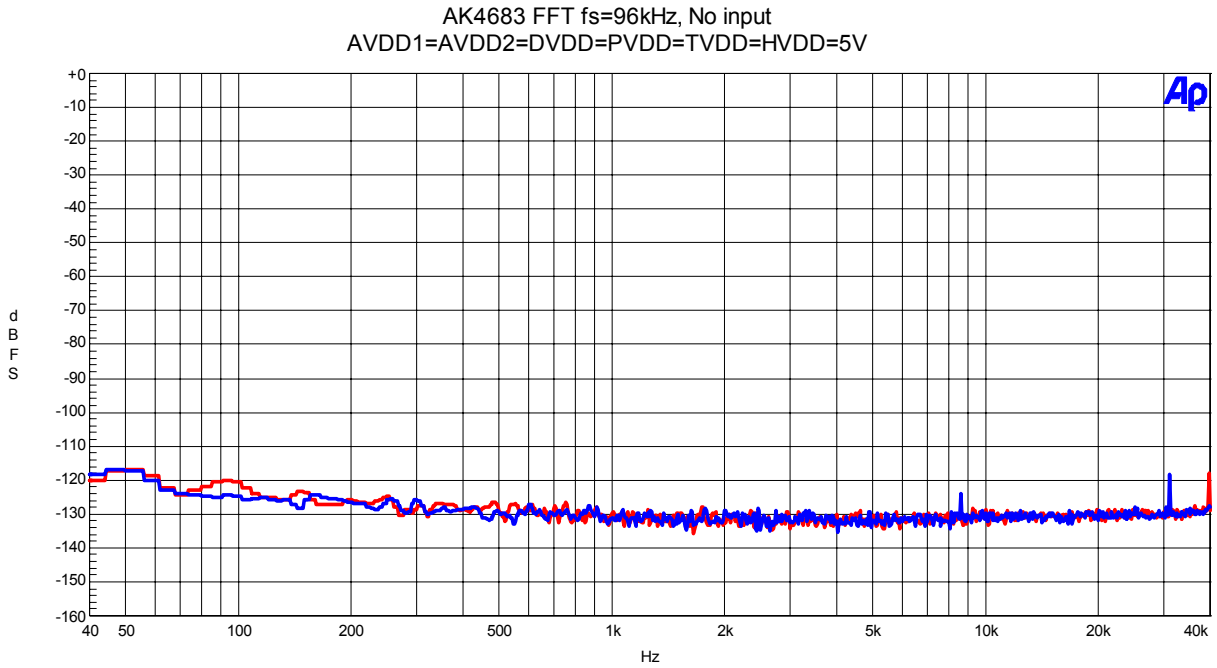


Figure 20. FFT(Noise floor)

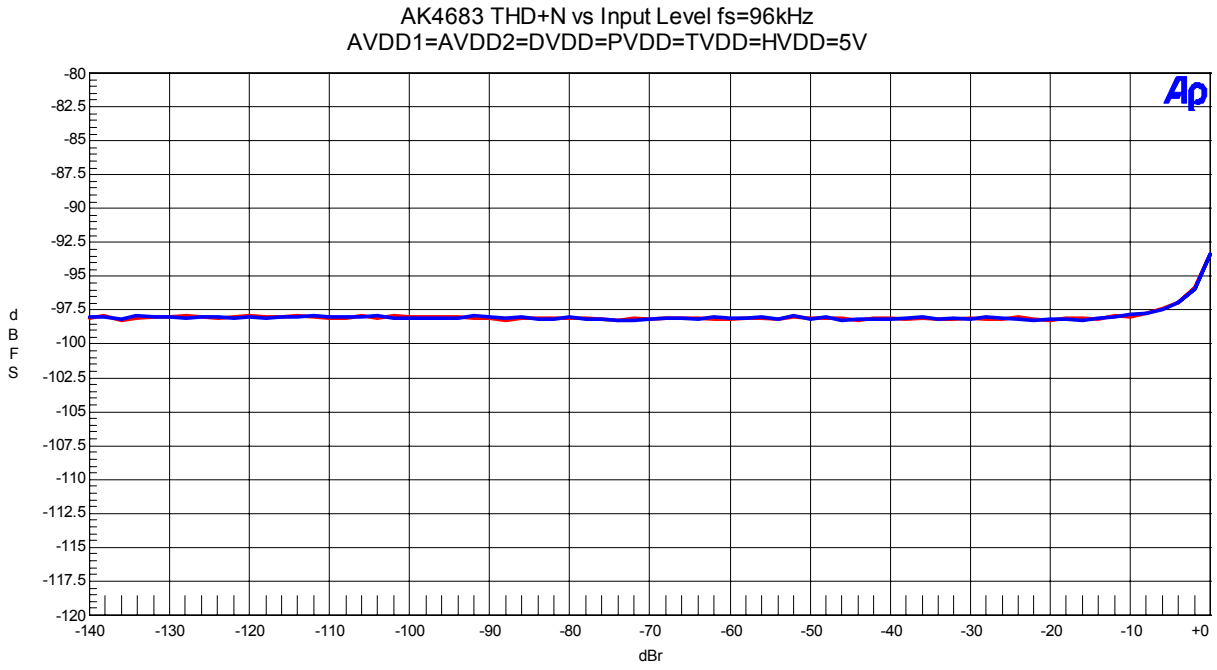


Figure 21. THD + N vs Input Level (Input Frequency =1kHz)

(ADC fs=96kHz)

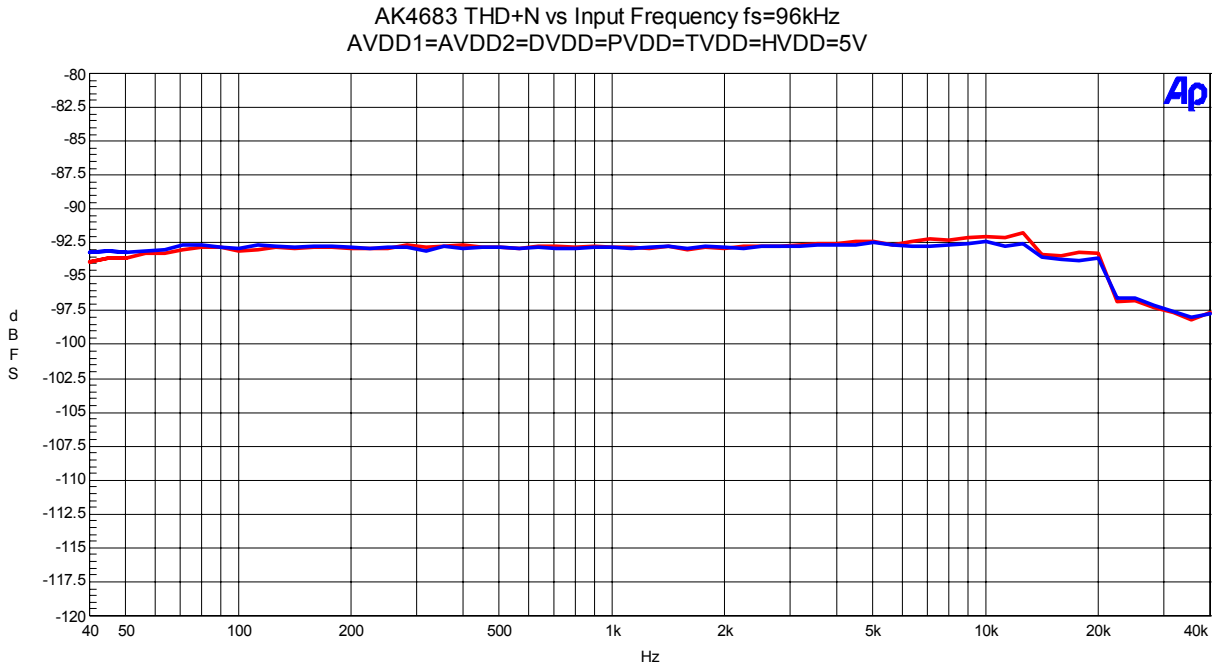


Figure 22. THD + N vs Input Frequency (Input Level=-0.5dBFS)

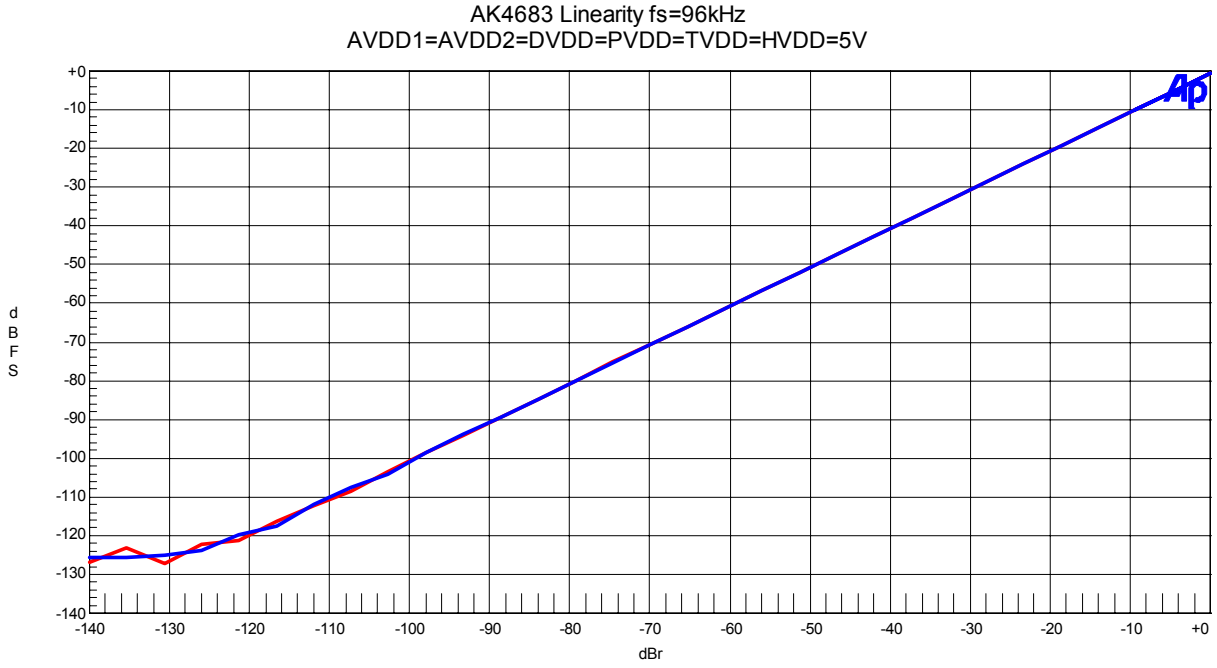


Figure 23. Linearity (Input Frequency =1kHz)

(ADC fs=96kHz)

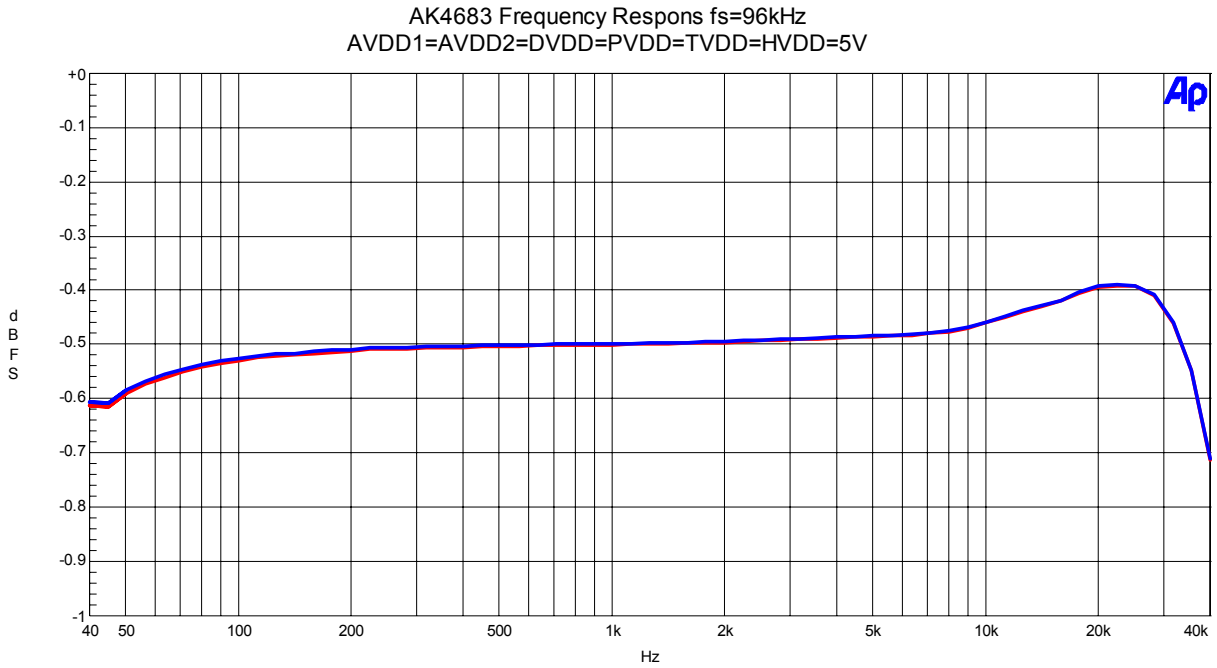


Figure 24. Frequency Response (Input Level=-0.5dBFS)

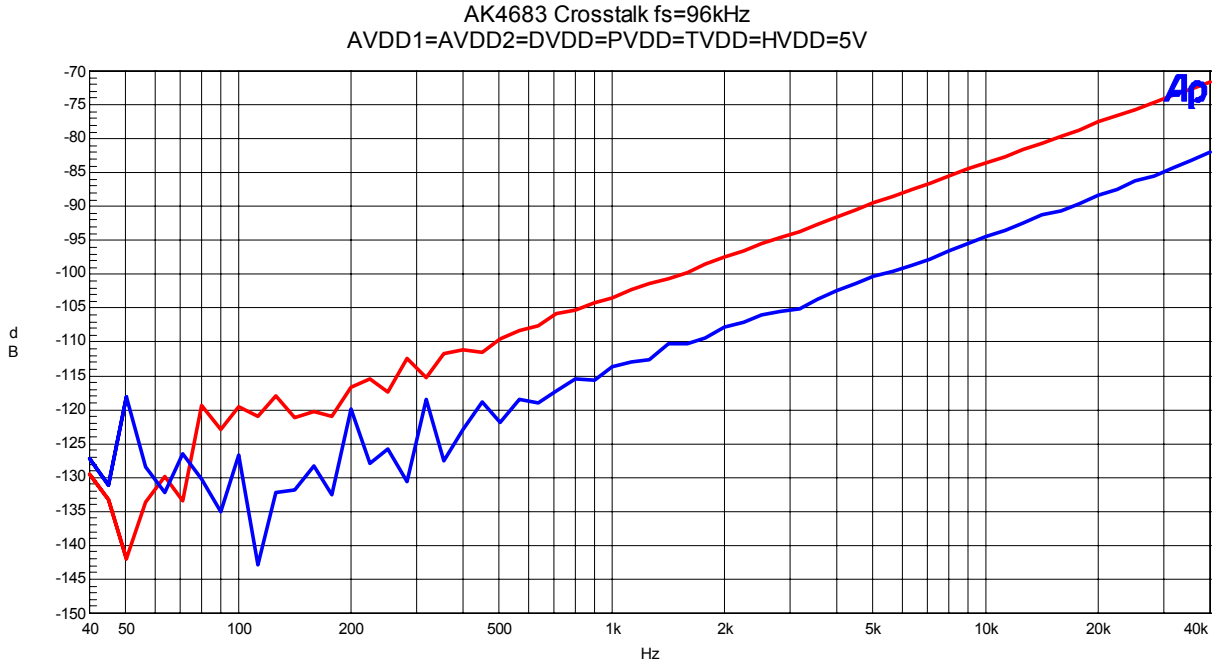


Figure 25. Crosstalk (Input Level=-0.5dBFS)

2.DAC部

(DAC fs=48kHz)

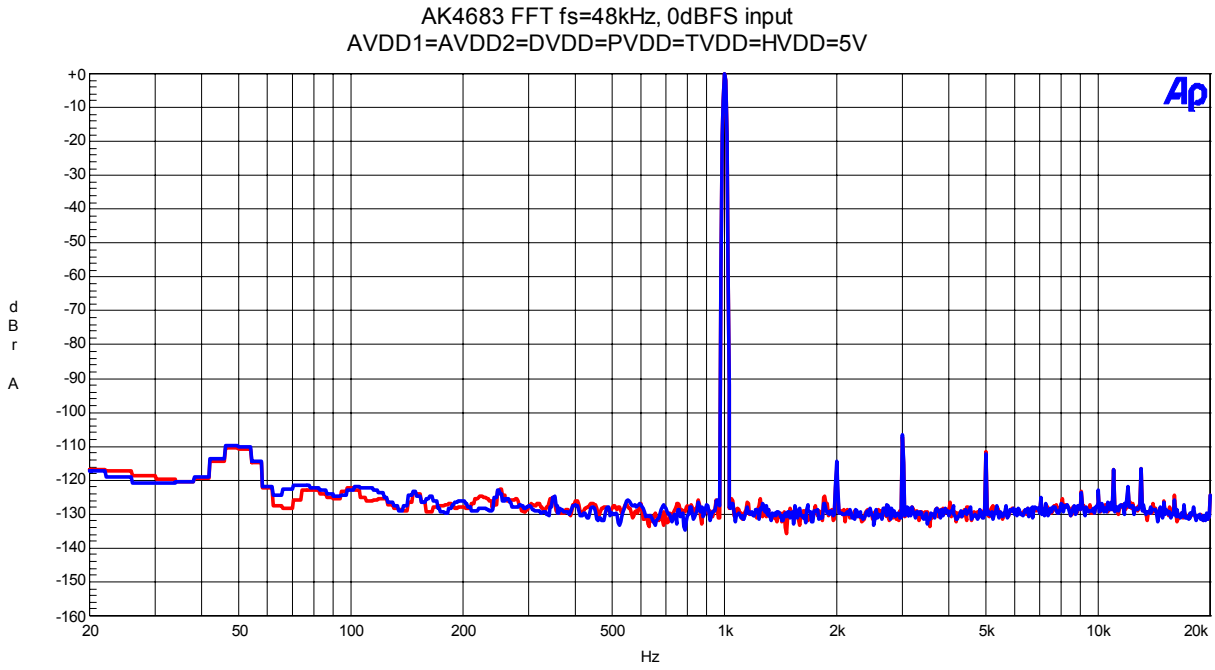


Figure 26. FFT(Input Frequency =1kHz, Input Level=0dBFS)

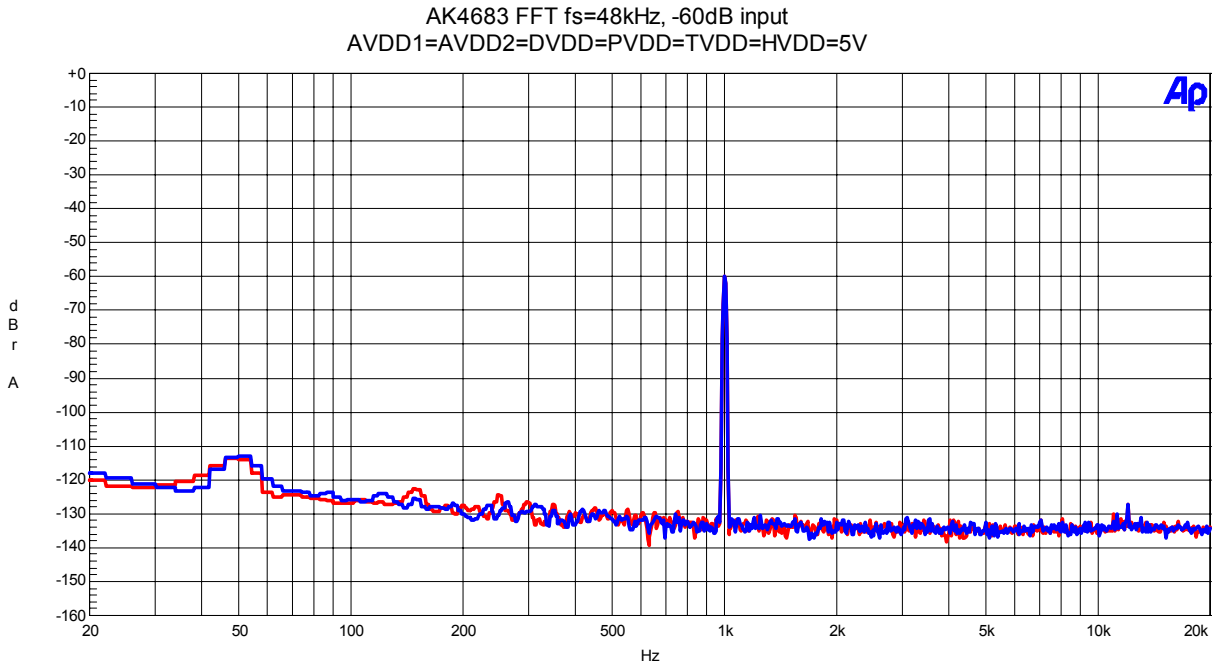


Figure 27. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

(DAC fs=48kHz)

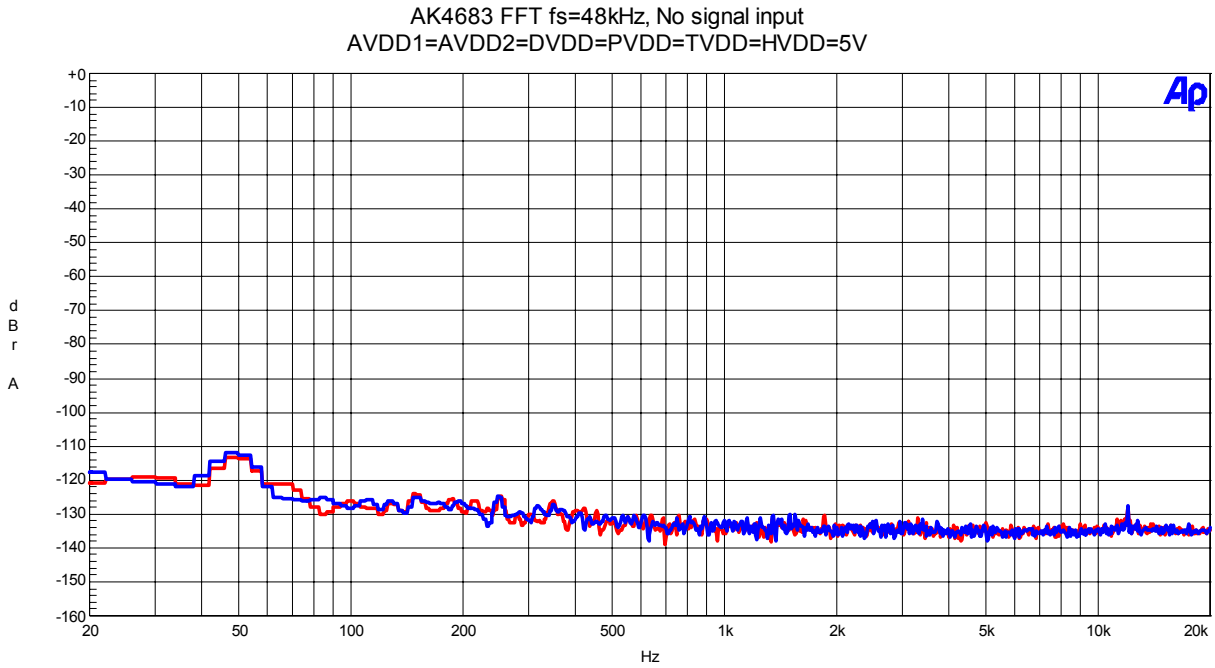


Figure 28. FFT(noise floor)

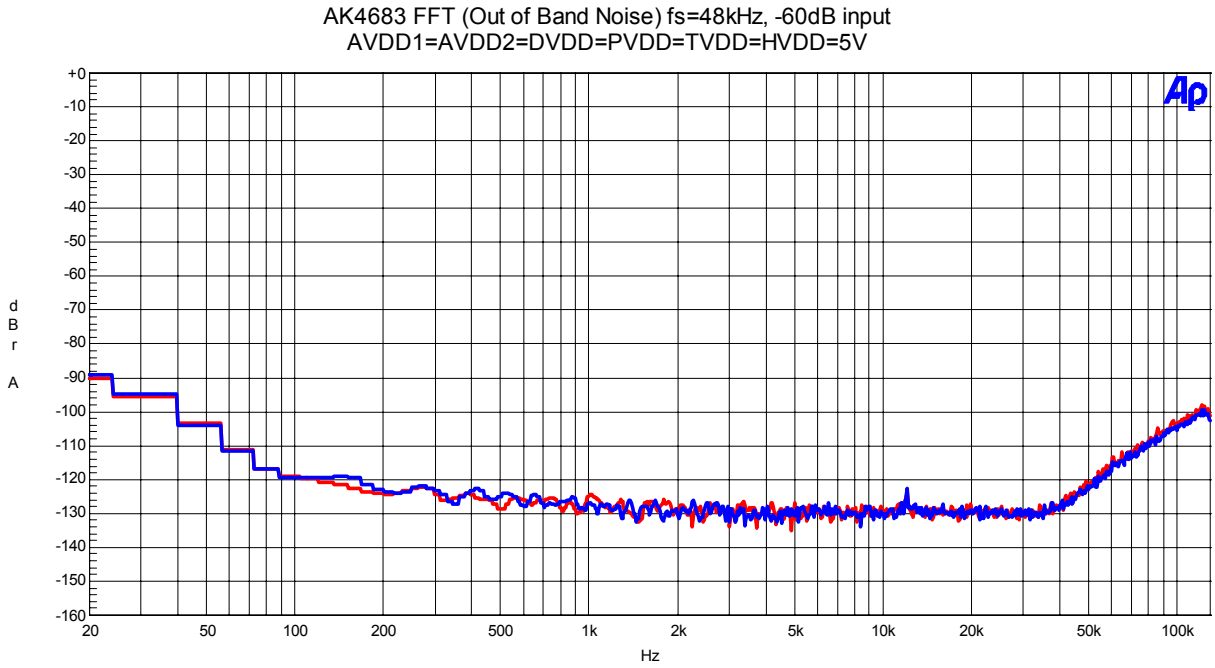


Figure 29. FFT(out-of-band noise)

(DAC fs=48kHz)

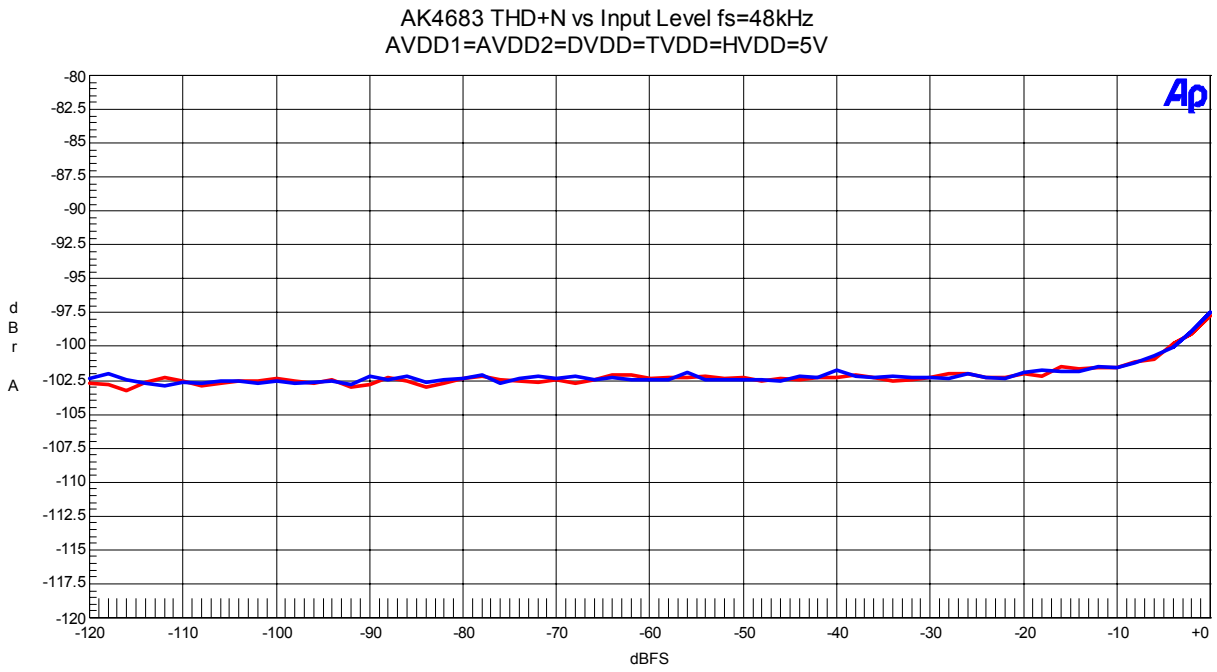


Figure 30. THD+N vs Input Level (Input Frequency =1kHz)

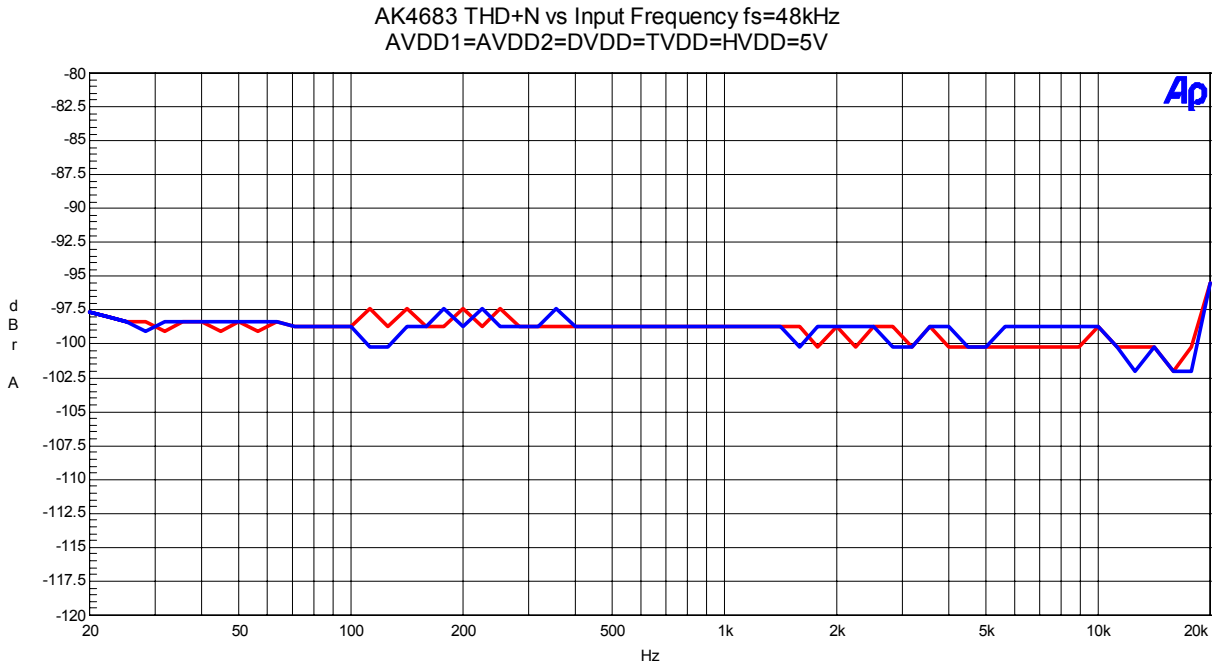


Figure 31. THD+N vs Input Frequency (Input Level=0dBFS)

(DAC fs=48kHz)

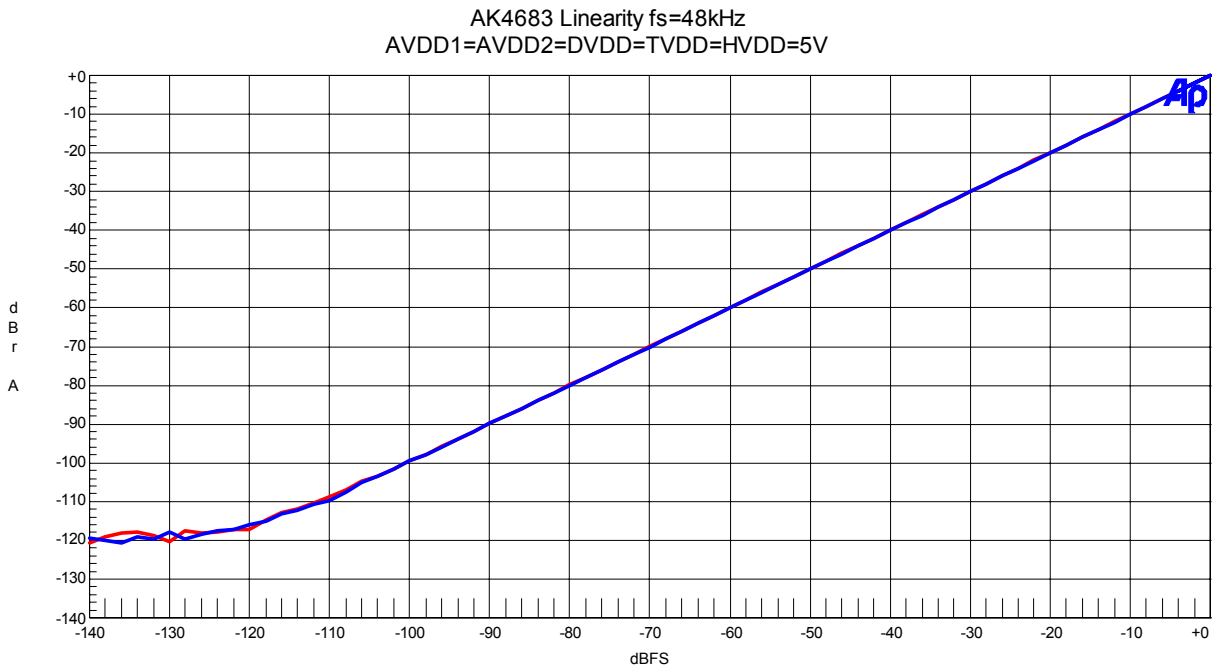


Figure 32. Linearity (Input Frequency =1kHz)

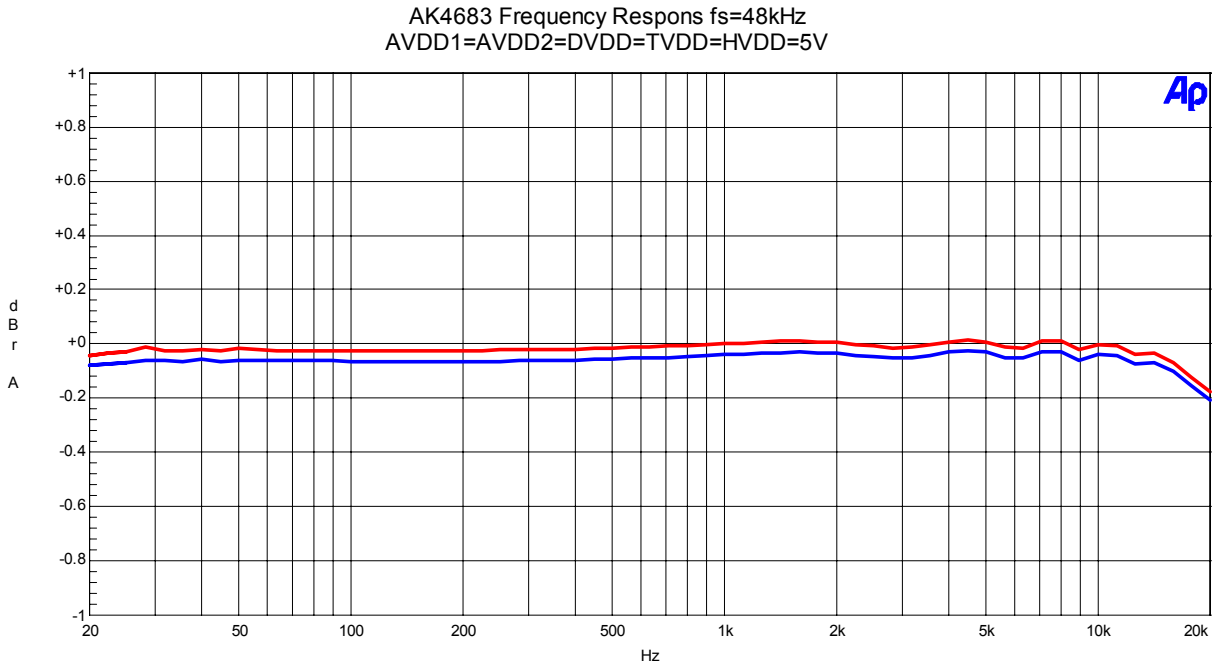


Figure 33. Frequency Response (Input Level=0dBFS)

(DAC fs=48kHz)

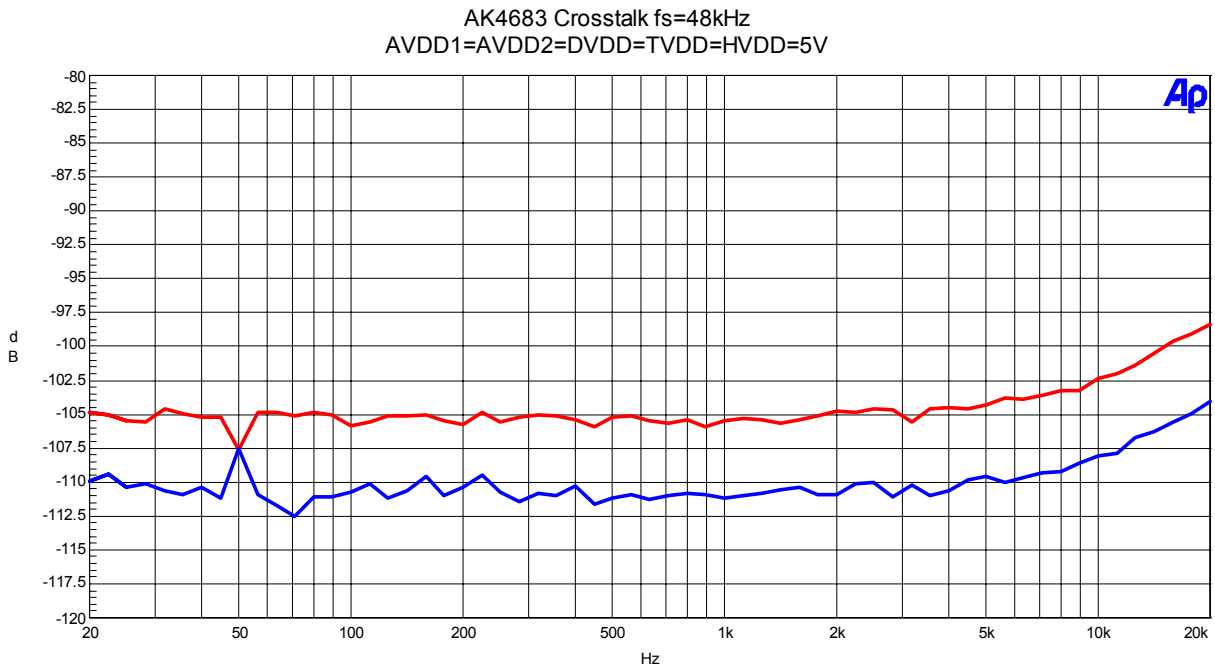


Figure 34. Cross-talk (Input Level=0dBFS)

(DAC fs=96kHz)

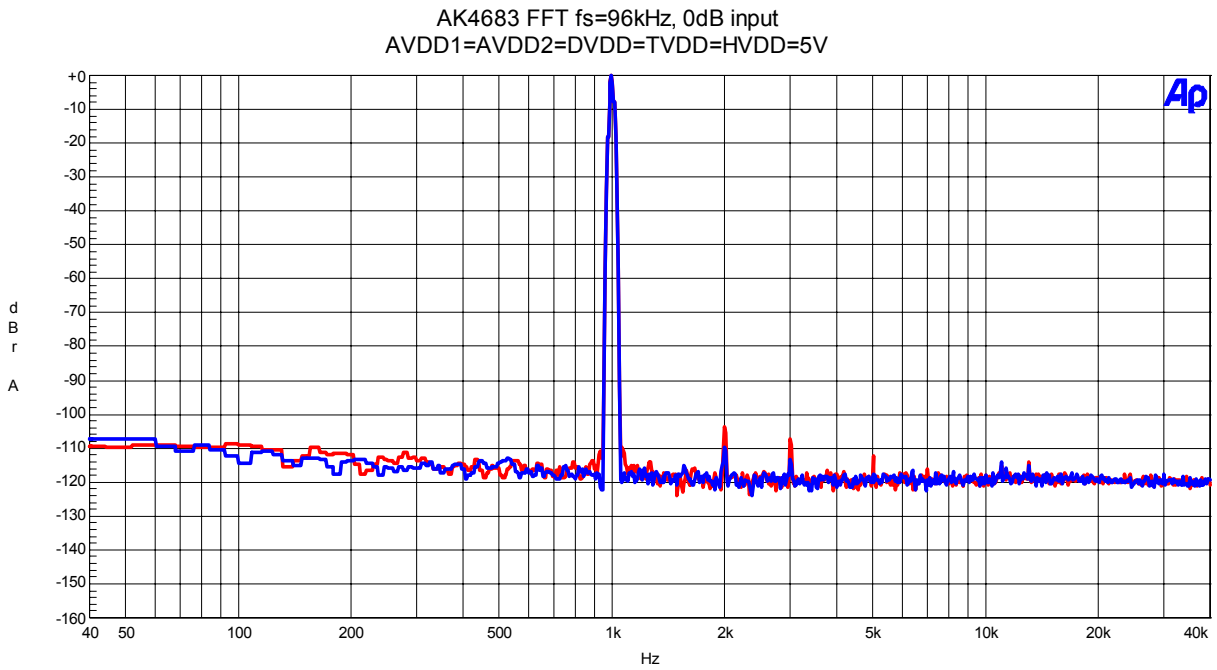


Figure 35. FFT(Input Frequency =1kHz, Input Level=0dBFS)

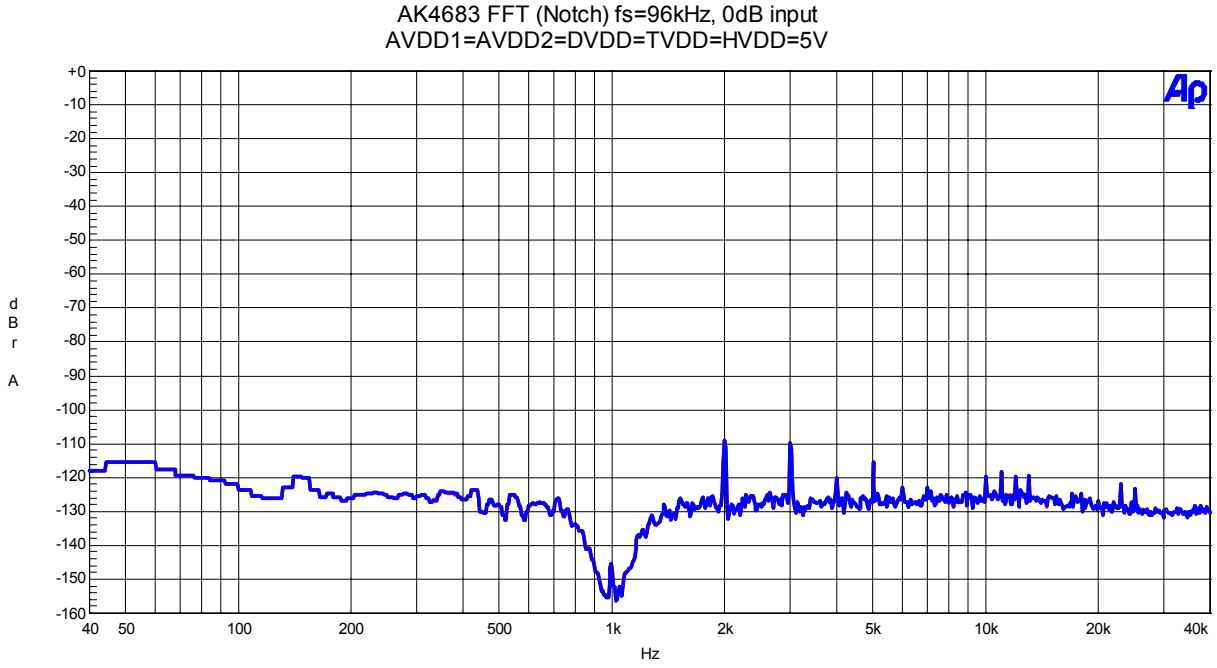


Figure 36. FFT(Input Frequency =1kHz, Input Level=0dBFS,Notch-on)

(DAC fs=96kHz)

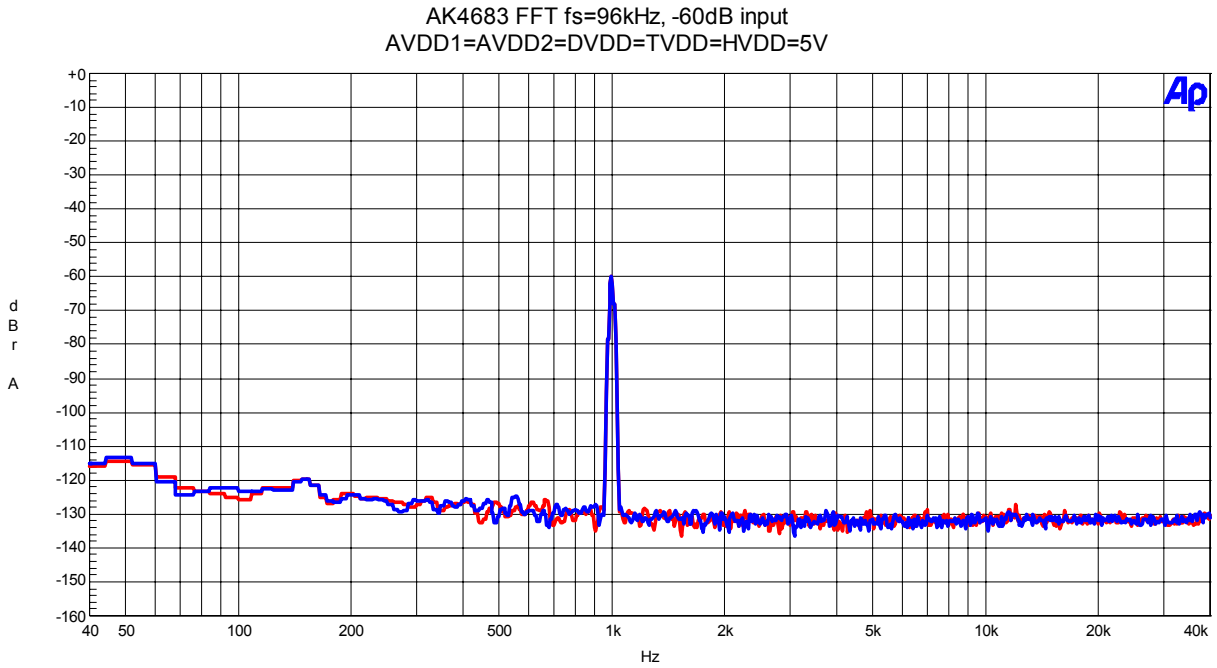


Figure 37. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

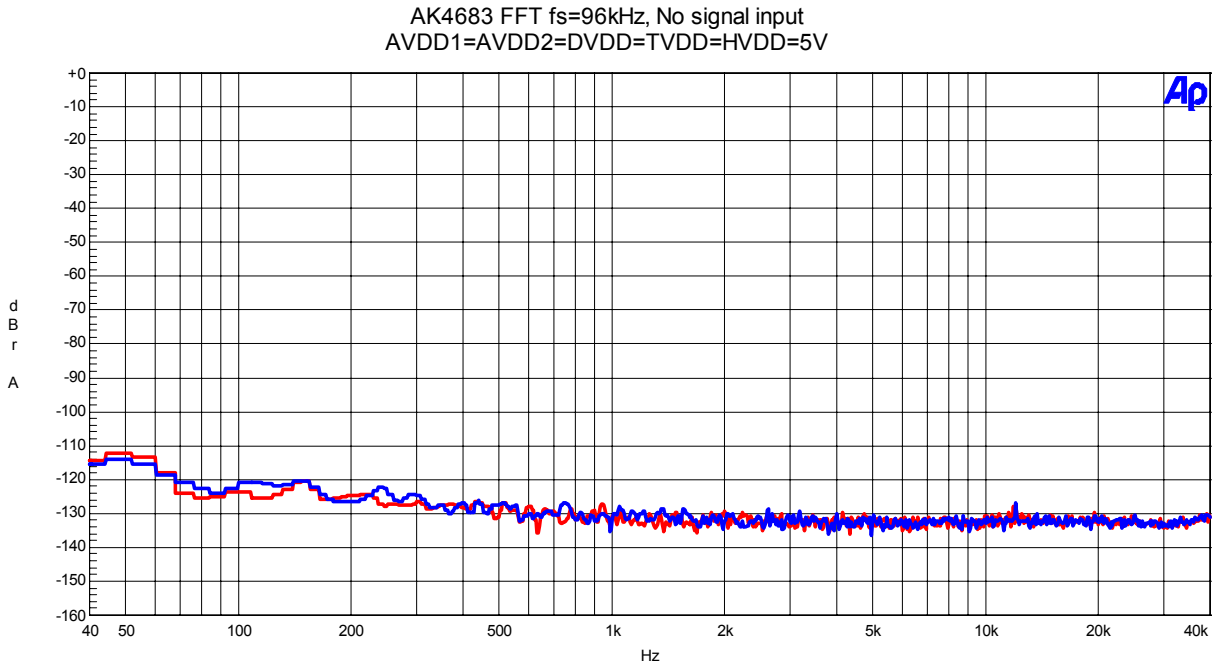
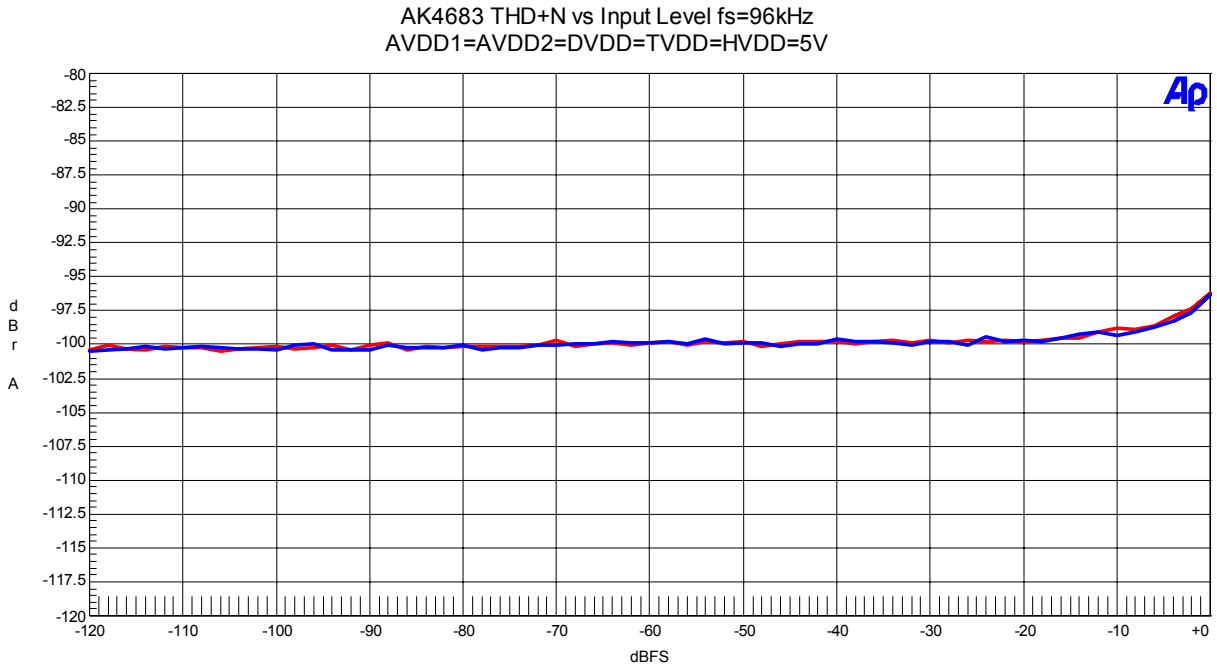


Figure 38. FFT(noise floor)

(DAC fs=96kHz)



FigureFigure 39. THD+N vs Input Level (Input Frequency =1kHz)

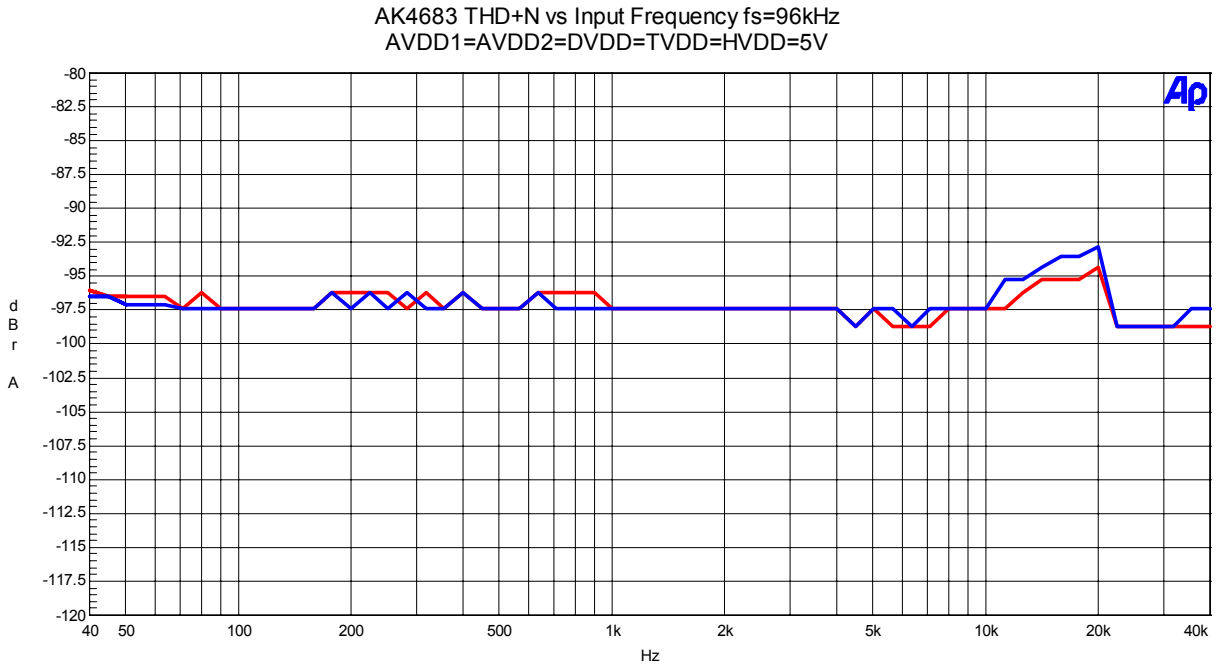


Figure 40. THD+N vs fin (Input Level=0dBFS)

(DAC fs=96kHz)

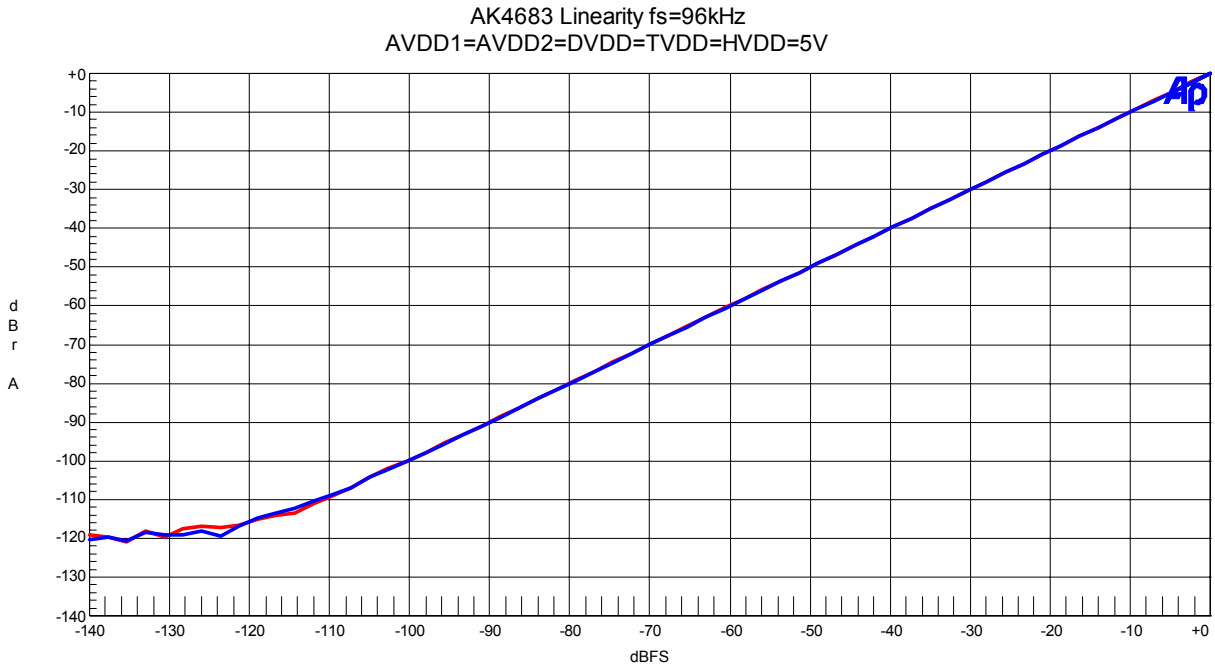


Figure 41. Linearity (Input Frequency =1kHz)

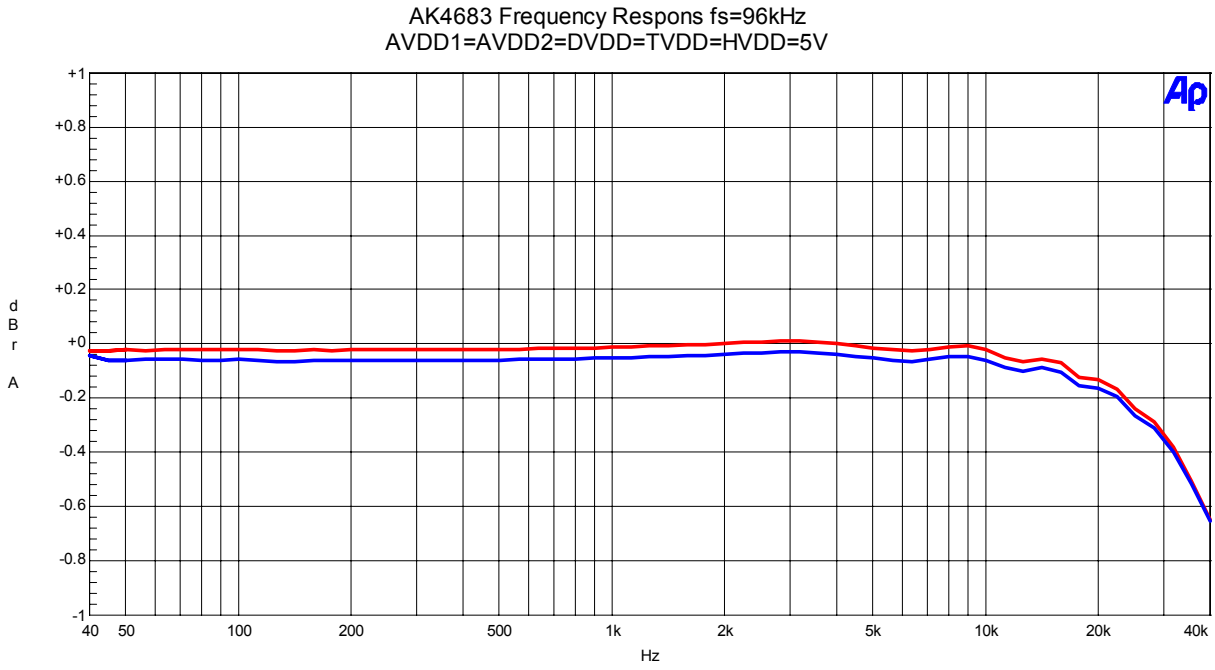


Figure 42. Frequency Response (Input Level=0dBFS)

(DAC fs=96kHz)

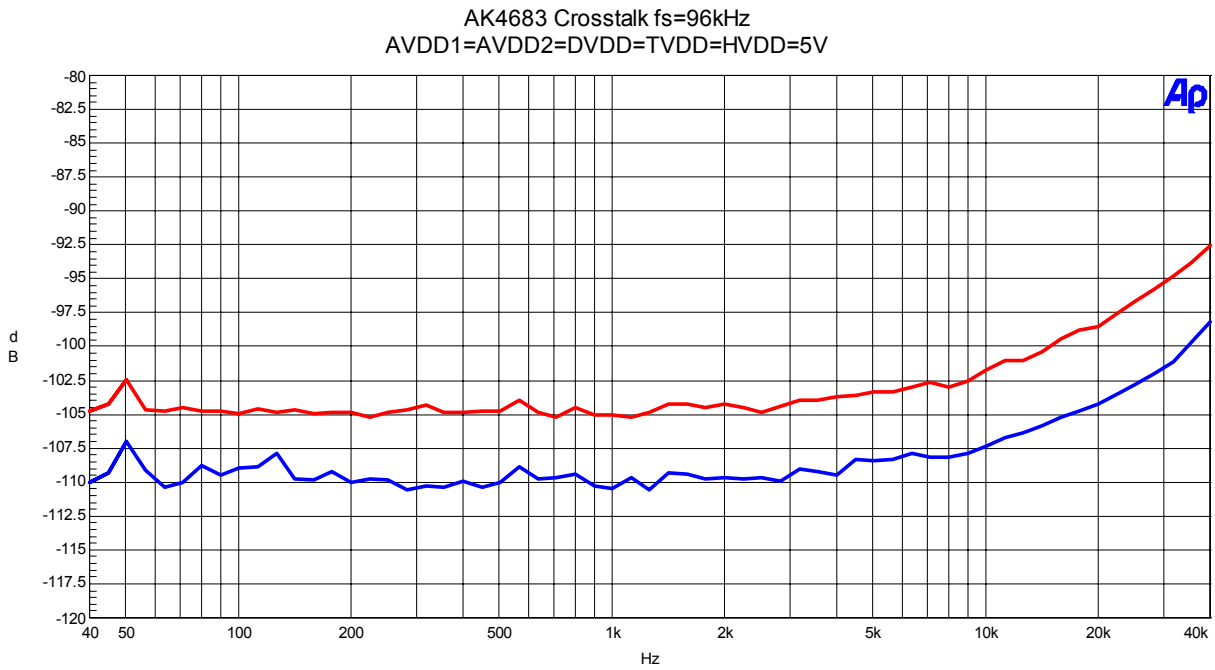


Figure 43. Cross-talk (Input Level=0dBFS)

(DAC fs=192kHz)

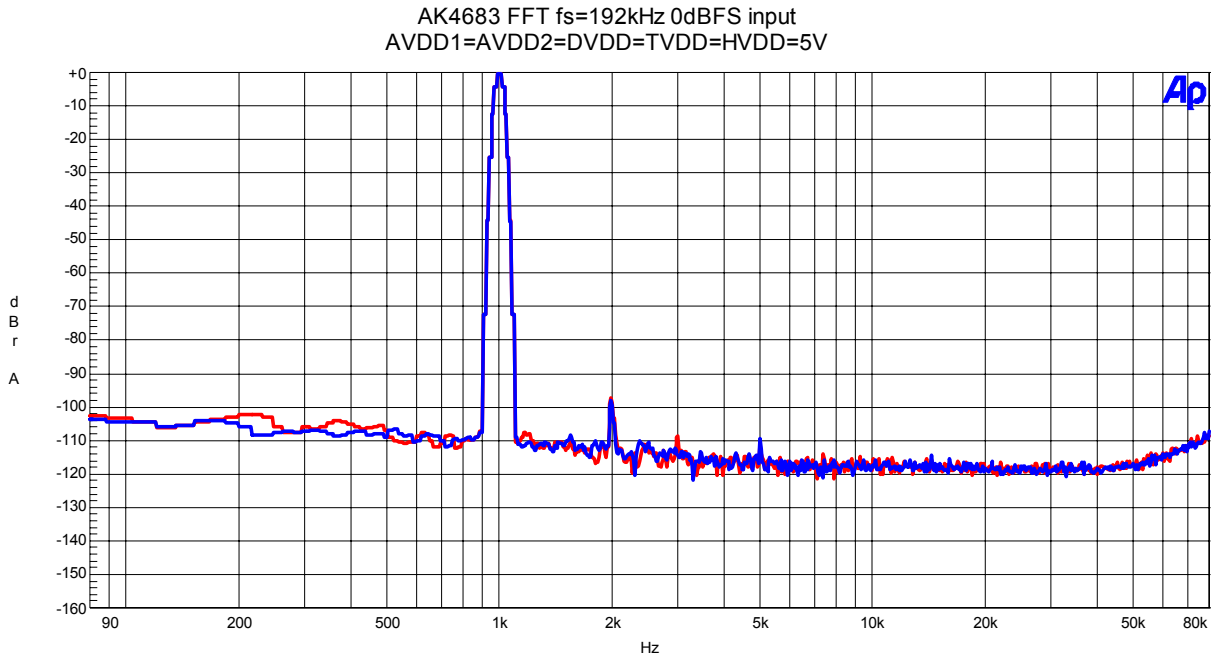


Figure 44. FFT(Input Frequency =1kHz, Input Level=0dBFS)

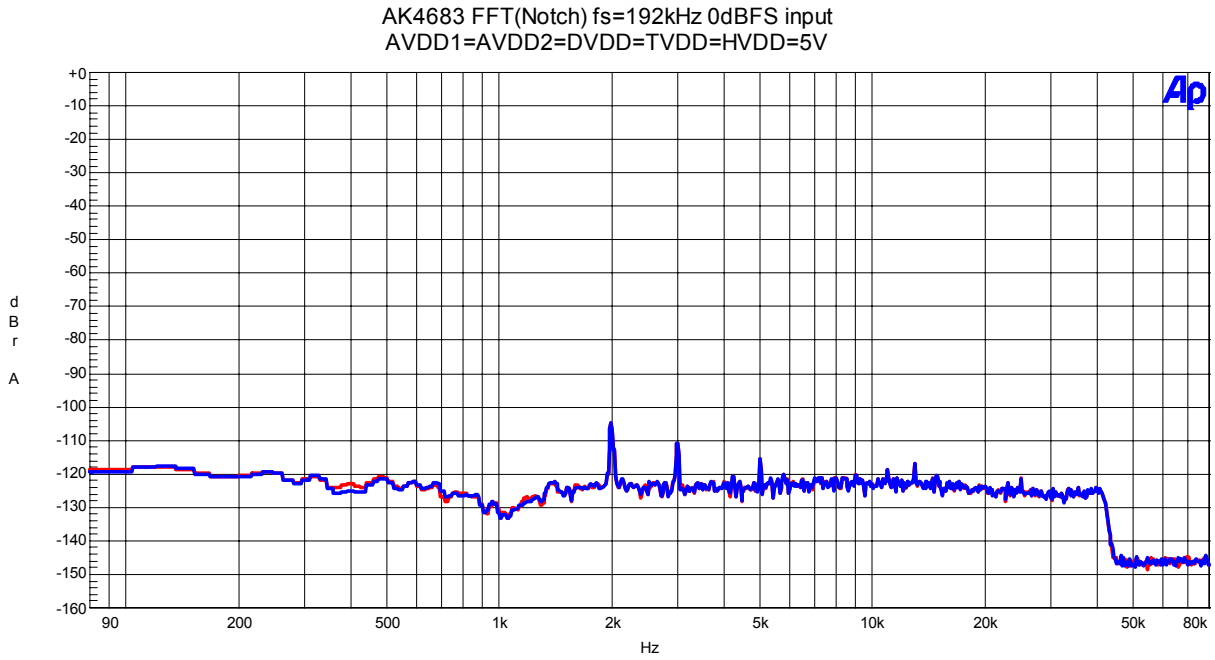


Figure 45. FFT(Input Frequency =1kHz, Input Level=0dBFS,Notch-on)

(DAC fs=192kHz)

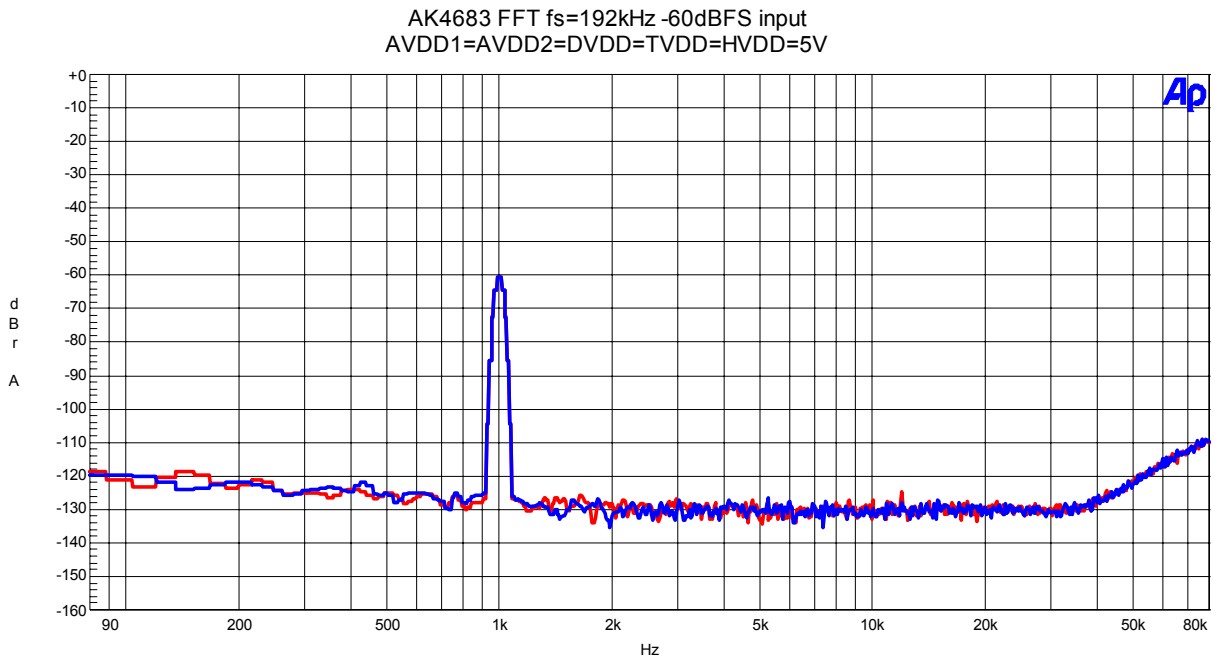


Figure 46. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

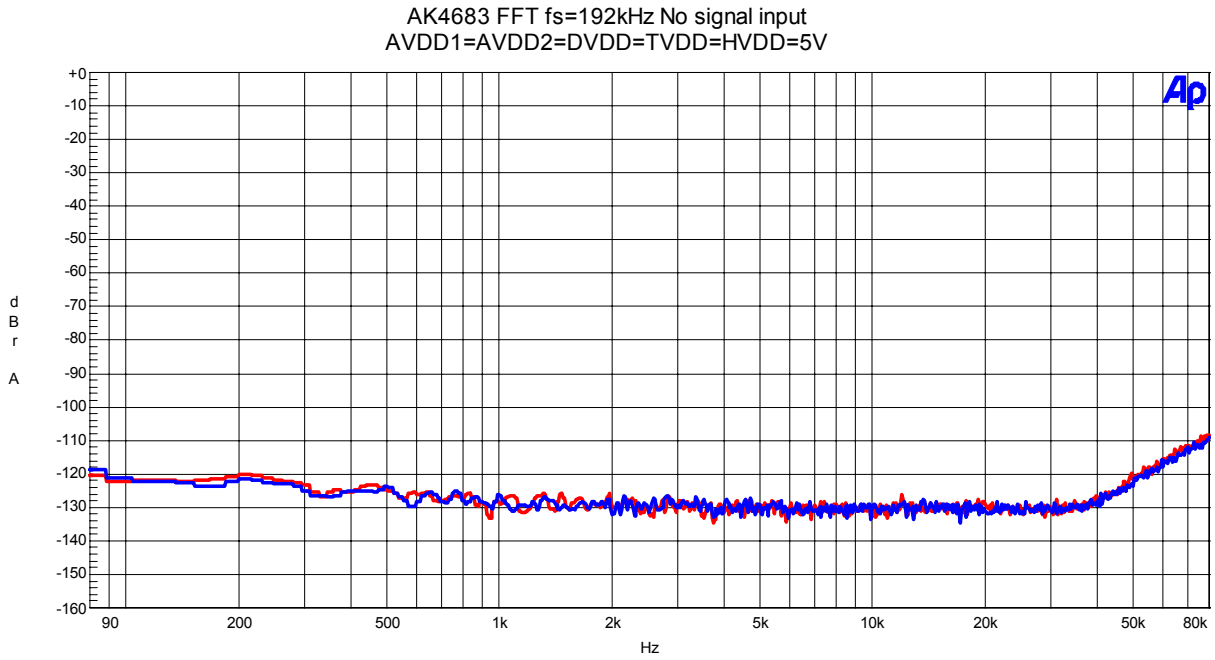


Figure 47. FFT(noise floor)

(DAC fs=192kHz)

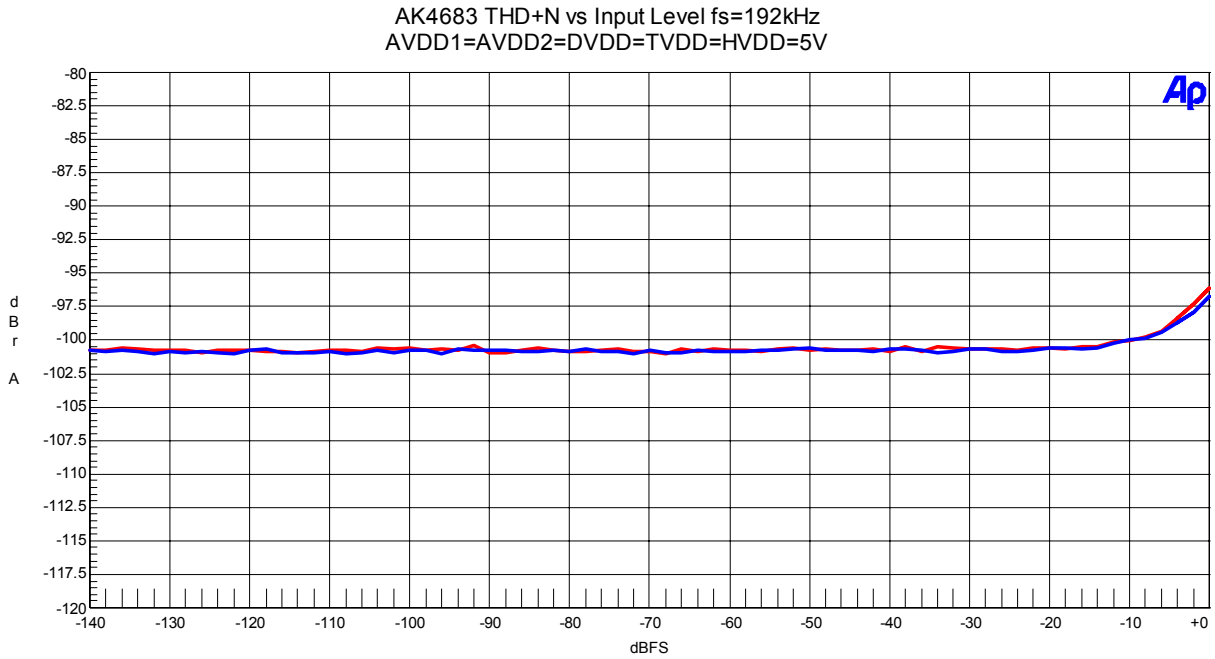


Figure 48. THD+N vs Input Level (Input Frequency =1kHz)

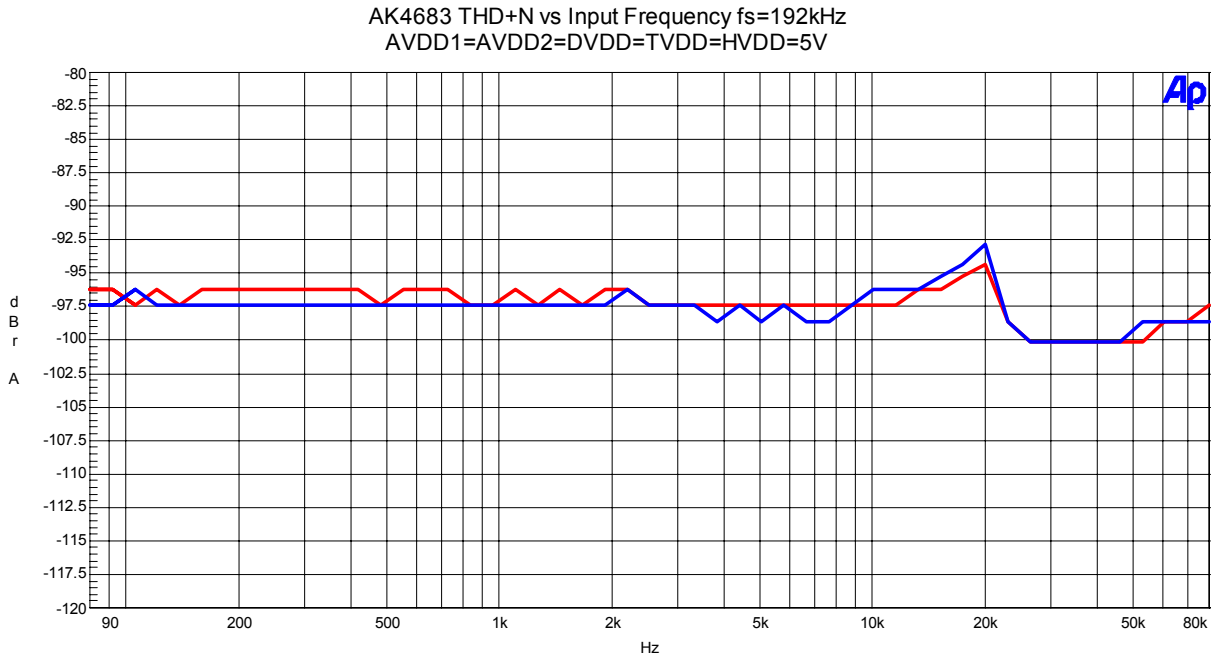


Figure 49. THD+N vs Input Frequency (Input Level=0dBFS)

(DAC fs=192kHz)

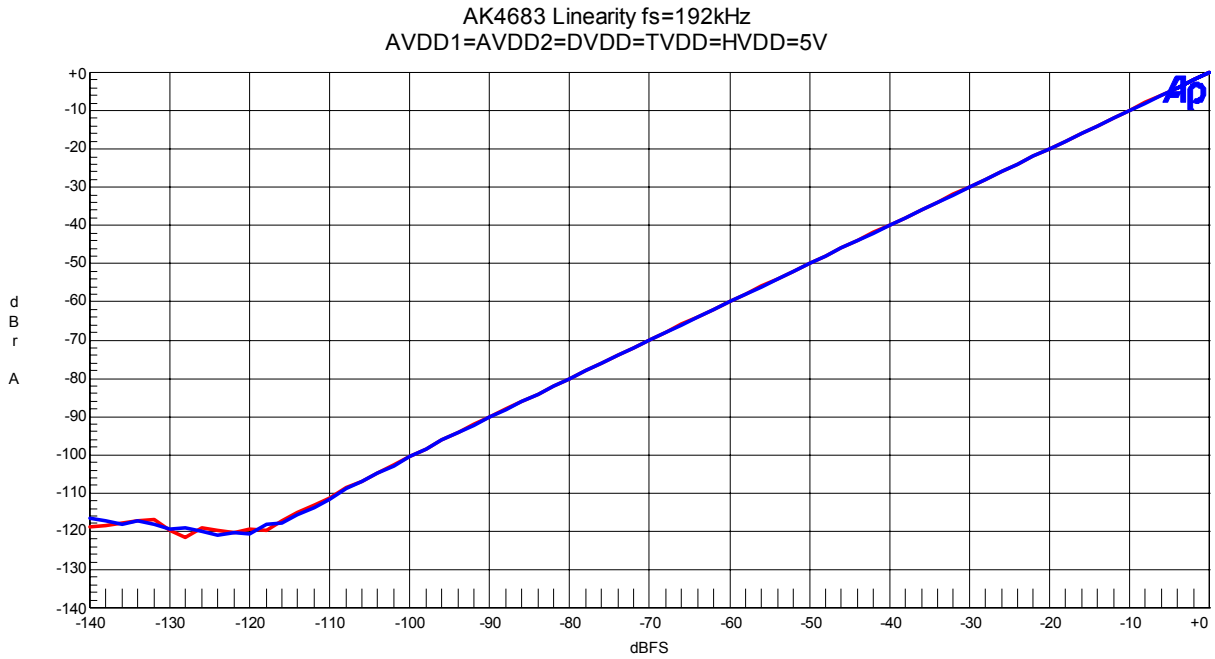


Figure 50. Linearity (f Input Frequency =1kHz)

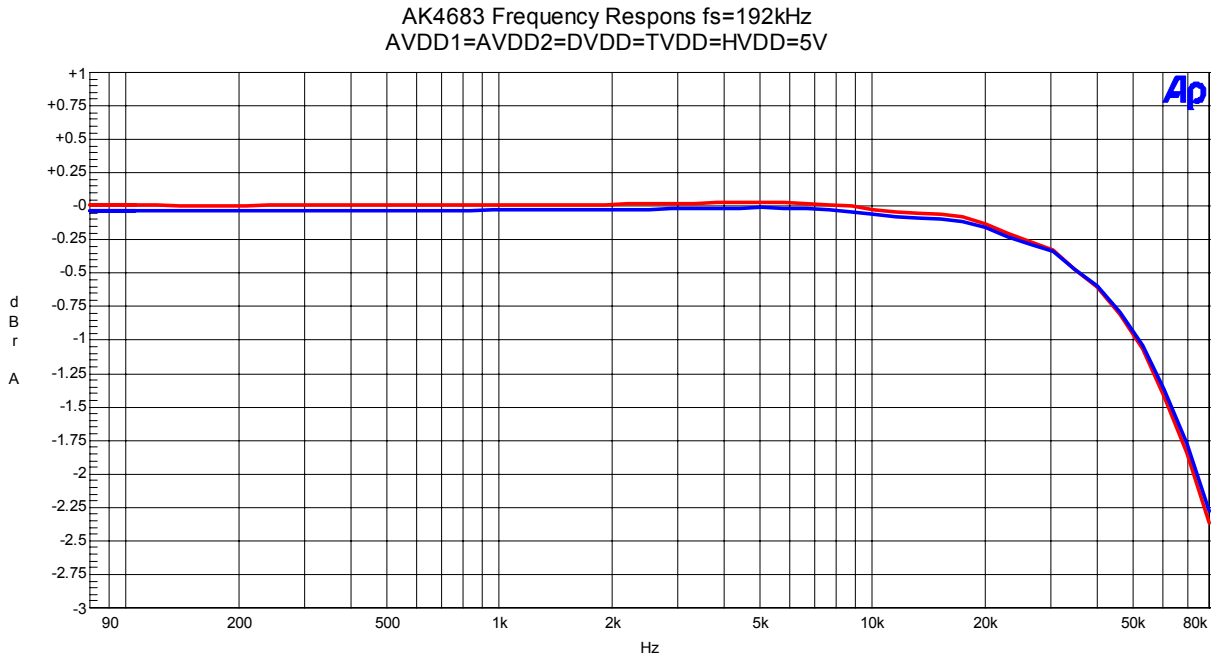


Figure 51. Frequency Response (Input Level=0dBFS)

(DAC fs=192kHz)

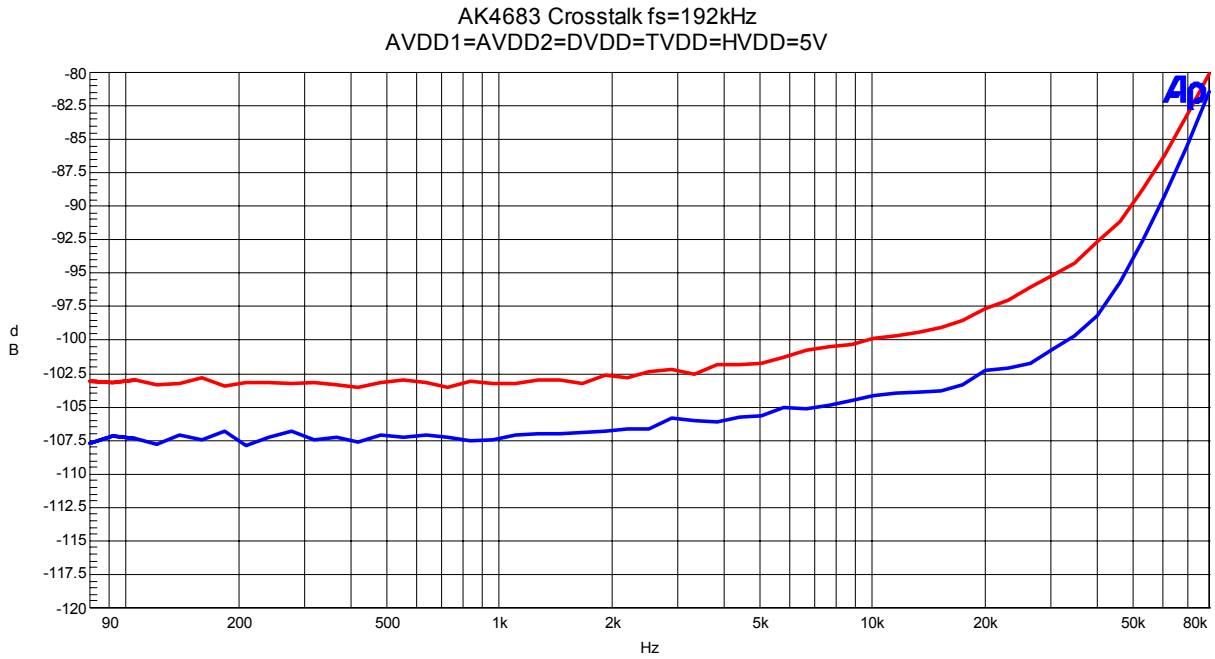


Figure 52. Cross-talk (Input Level=0dBFS)

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
06/05/12	KM080900	0	First Edition	
06/05/25	KM080901	0	Error Correct	P.3. (3) DAC with external DIR 2. Setting of jumper pin Add (Default input of PORTA is SDTIA1.) JP16 (ILRCK)→JP16 (ILRCKA) JP19(SDTIA2)： PORTA: DIR→GND JP20(SDTIA3)： PORTA: DIR→GND Add column of JP23 (SDTO) 4. Setting of DIP switch P.4. (4) ADC with external DIT 2. Setting of jumper pin JP16 (ILRCK)→JP16 (ILRCKA) Add column of JP23 (SDTO) 4. Setting of DIP switch SW2 (PORT-DIR/4683)→SW2 (PORTA-DIR/4683) P.7. Set up Jumper pins JP15 (XTIA)：Evaluation Mode 4：Open→Short JP16 (ILRCKA)：Evaluation Mode 4：Short → Open JP19(SDTIA2)： Evaluation Mode 3: DIR→GND JP20(SDTIA3)： Evaluation Mode 3: DIR→GND JP21(MCLK-SEL)： Evaluation Mode 1, 2, 4, 5：MCKO1→Open JP24 (OLRCK)→JP24 (OLRCKA) JP24 (OLRCKA)：Evaluation Mode 4：Open → Short JP25 (SDTIB)：Evaluation Mode 3：DIR → GND JP27 (BICKB)：Evaluation Mode 1, 2, 3, 4, 5：Short → Open JP28 (LRCKB)：Evaluation Mode 1, 2, 3, 4, 5：Short → Open JP29(MCLK)： Evaluation Mode 1, 2, 3, 4, 5：MCKI→Open

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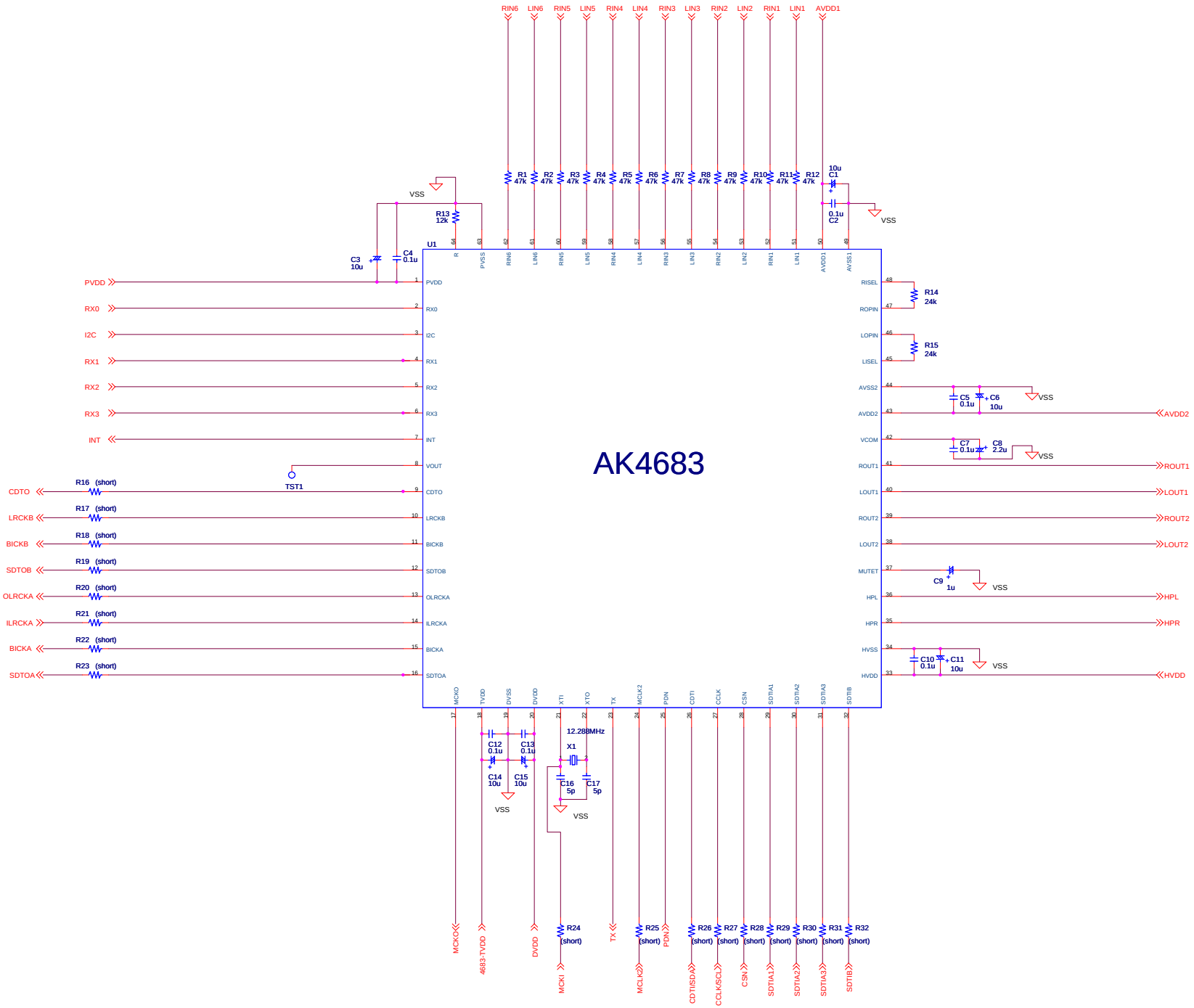

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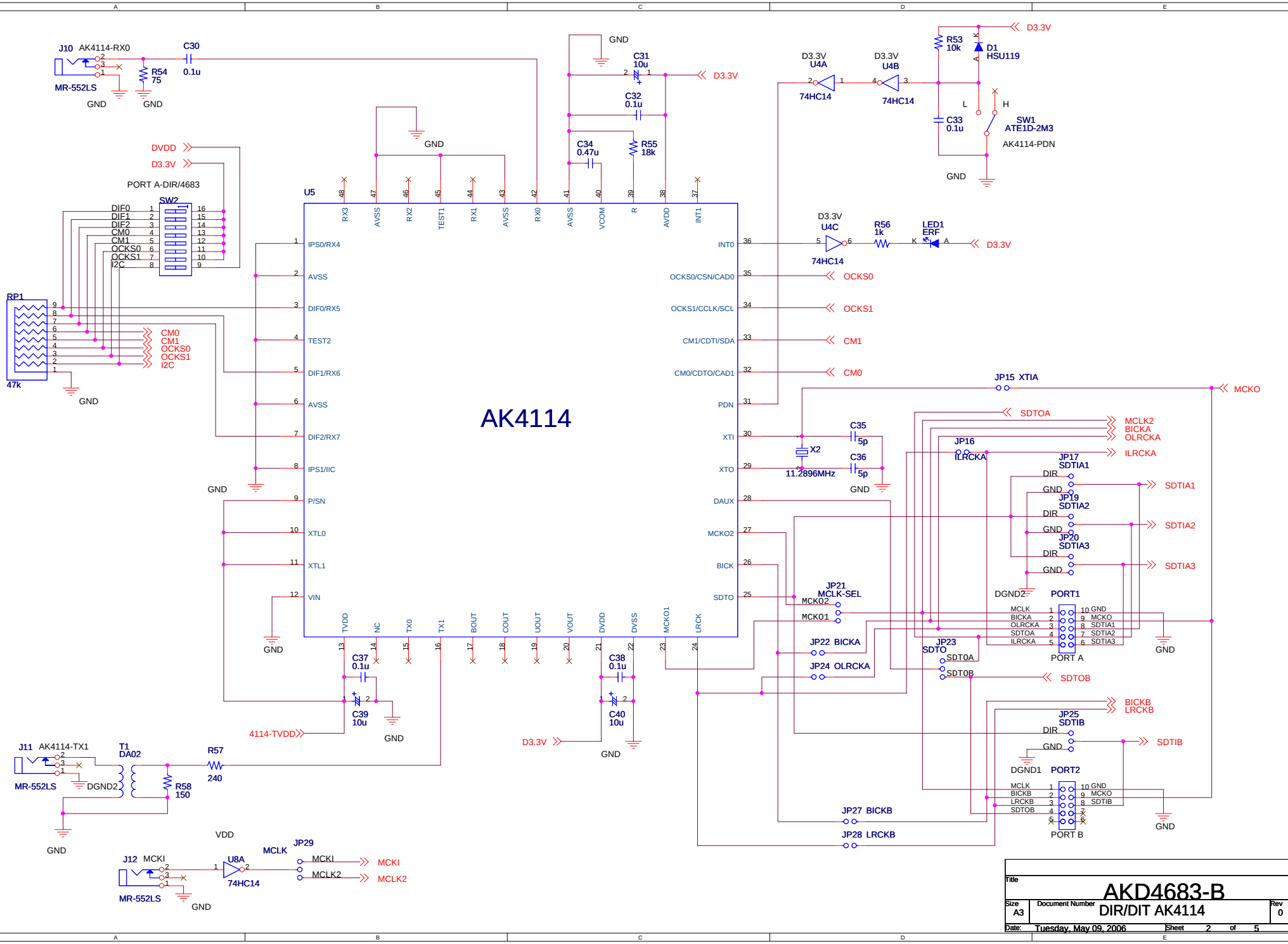
AK4114
U5
J10 AK4114-RX0
MR-552LS
R54 75
C30 0.1u
C31 10u
C32 0.1u
C34 0.47u
R55 18k
C33 0.1u
R53 10k
D1 HSU119
SW1 ATE1D-2M3
AK4114-PDN
74HC14
U4A
U4B
U4C
R56 1k
LED1 ERF
PORT A-DIR/4683
SW2
DIF0
DIF1
DIF2
CM0
CM1
OCKS0
OCKS1
I2C
RP1
47k
C35 5p
C36 5p
X2
11.2896MHz
JP15 XTIA
JP16 ILRCKA
JP17 SDTIA1
JP19 SDTIA2
JP20 SDTIA3
JP21 MCLK-SEL
JP22 BICKA
JP24 OLRCKA
JP23 SDTO
JP25 SDTIB
JP27 BICKB
JP28 LRCKB
PORT1
PORT2
PORT A
PORT B
DGND1
DGND2
C37 0.1u
C38 0.1u
C39 10u
C40 10u
4114-TVDD
J11 AK4114-TX1
T1 DA02
R57 240
R58 150
J12 MCKI
JP29 MCLK
MCKI
MCLK2
VDD
GND
D3.3V
DVDD
SDTOA
SDTOB
ILRCKA
SDTIA1
SDTIA2
SDTIA3
SDTIB
MCKO
MCLK2
BICKA
OLRCKA
BICKB
LRCKB
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DIR/DIT AK4114
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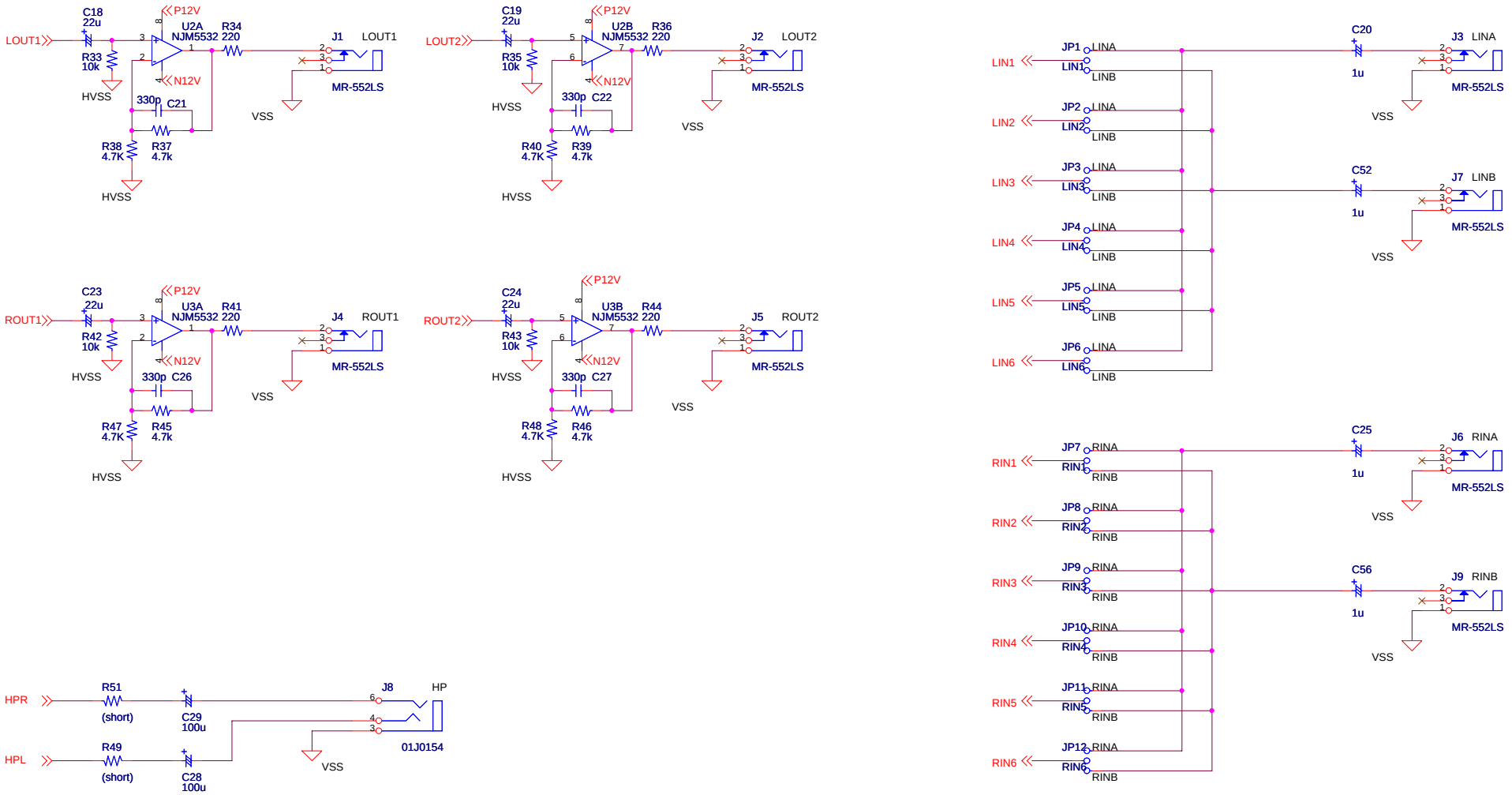

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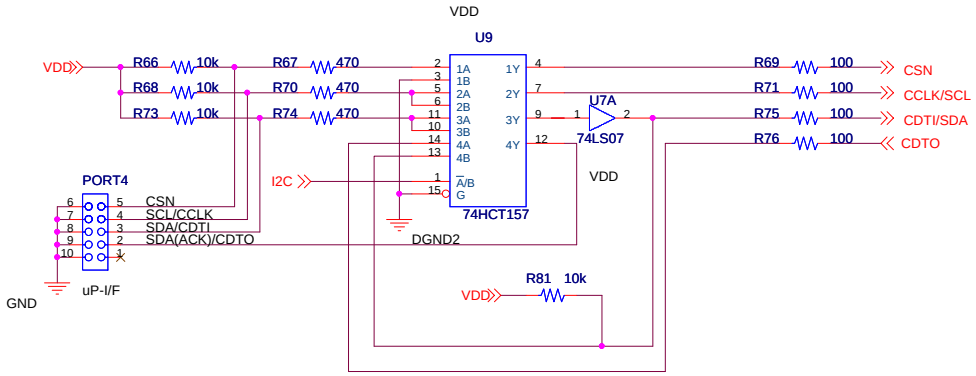

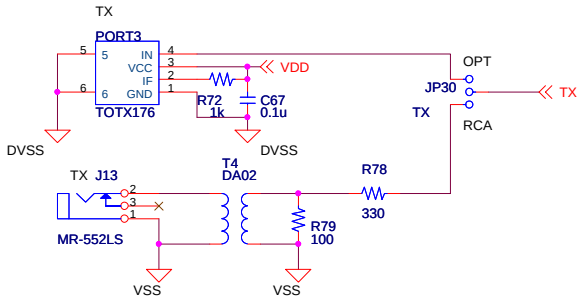

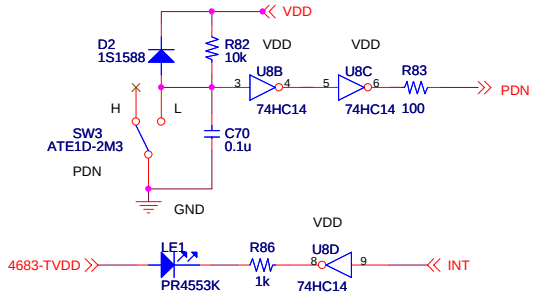

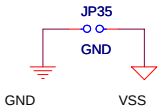

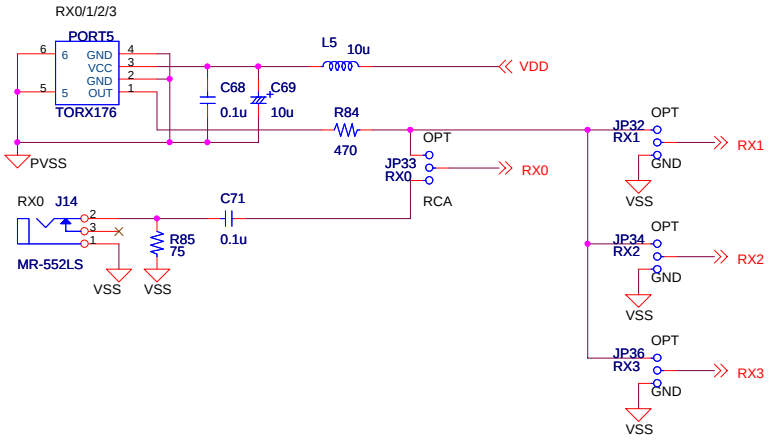

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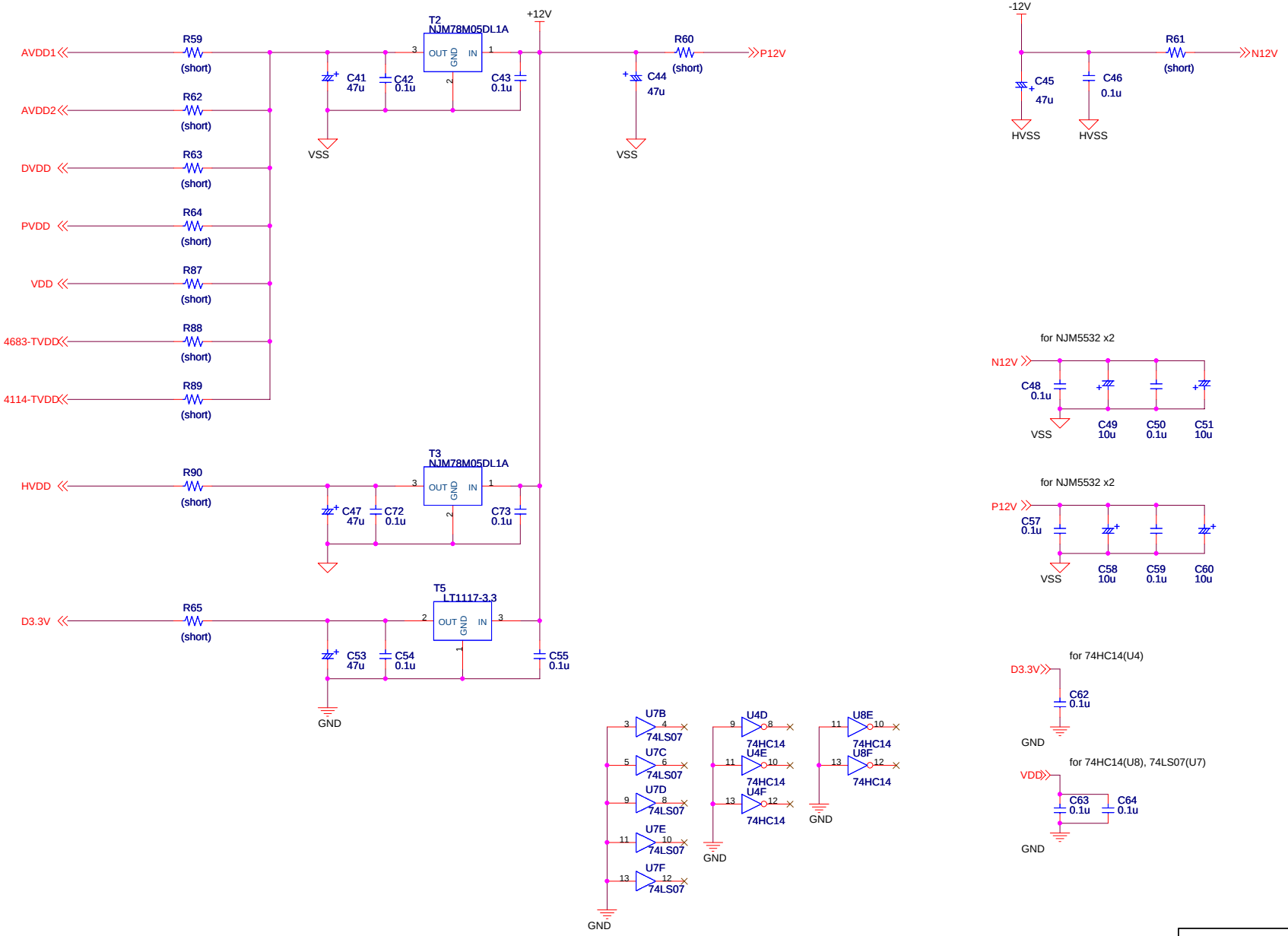

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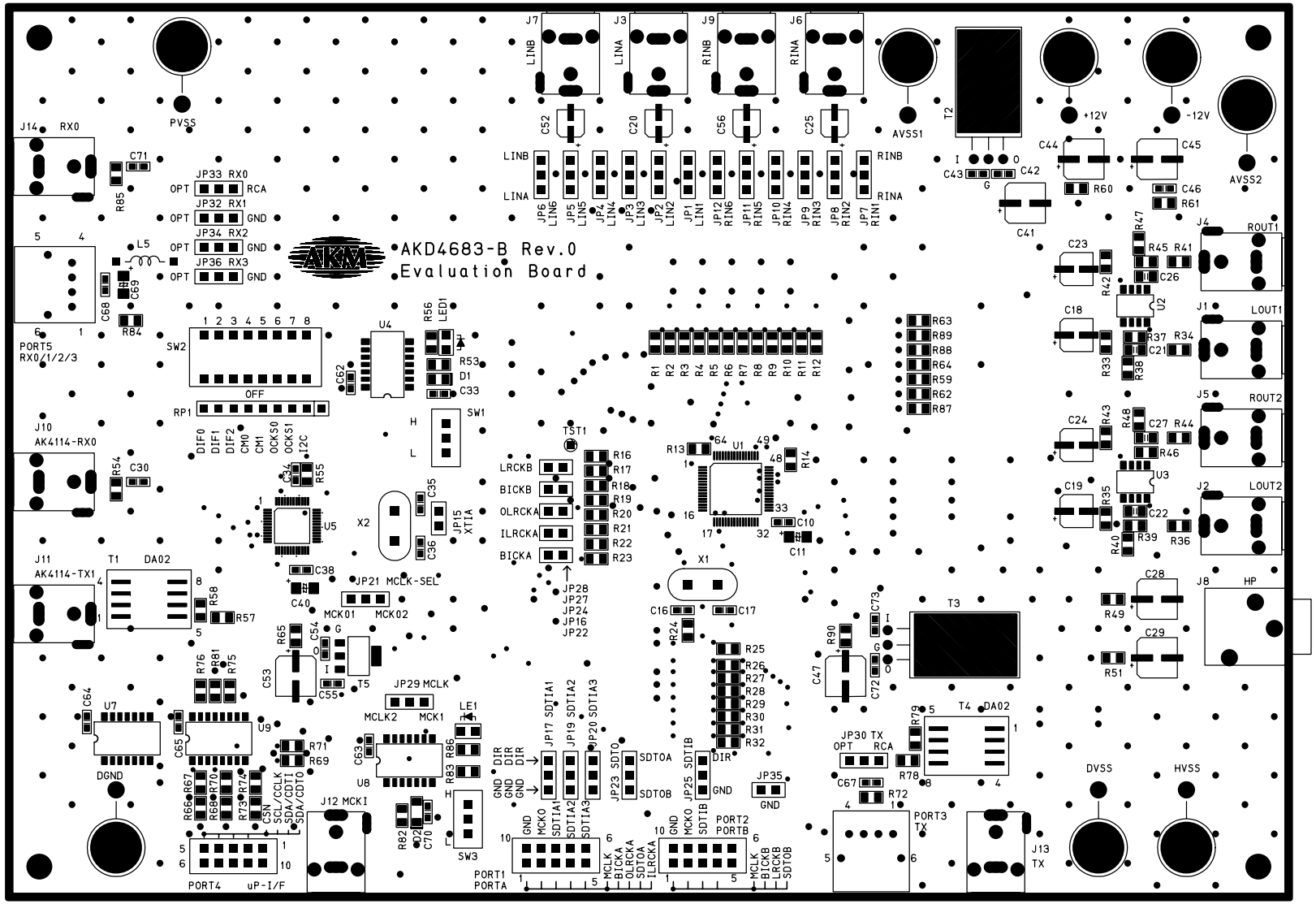
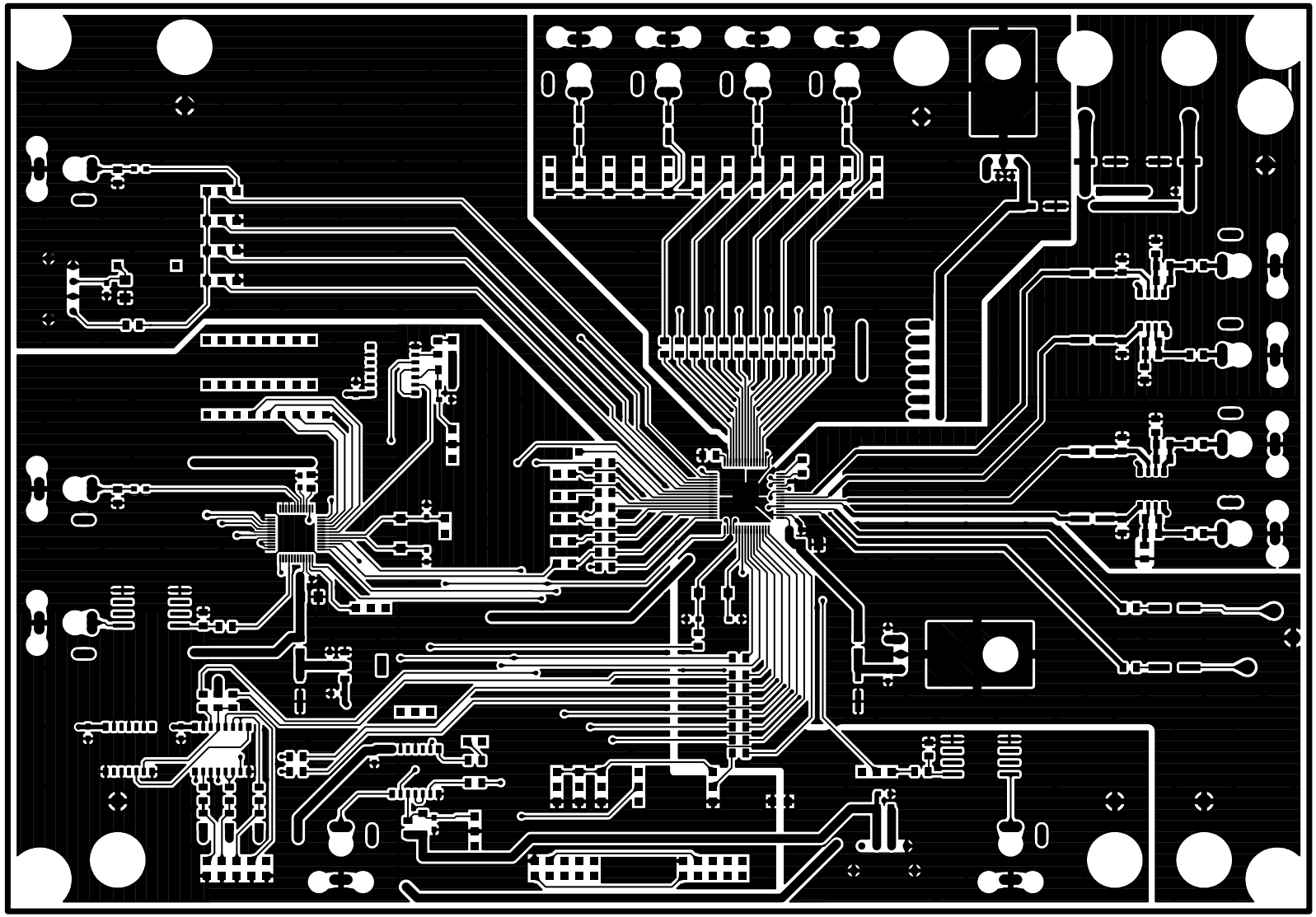


AKD4683-B L1 SILK

AKD4683-B L2 SILK



AKD4683-B L1

AKD4683-B L2