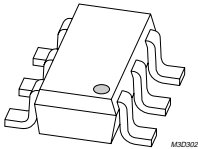


PMN34LN



1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMN34LN in SOT457 (TSOP6).

1.2 Features

- Low on-state resistance in small surface mount package.

1.3 Applications

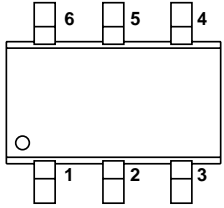
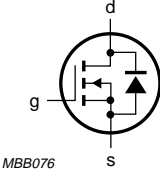
- DC-to-DC primary side.

1.4 Quick reference data

- $V_{DS} \leq 20\text{ V}$
- $I_D \leq 5.7\text{ A}$
- $P_{tot} \leq 1.75\text{ W}$
- $R_{DSon} \leq 34\text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT457 (TSOP6), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,5,6	drain (d)	 <p>Top view MBK092</p>	 <p>MBB076</p>
3	gate (g)		
4	source (s)		

SOT457 (TSOP6)

3. Limiting values

Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage (DC)		-	± 15	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	5.7	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	3.6	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	22.9	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	1.75	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	1.45	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	5.95	A