FAIRCHILD
SEMICONDUCTOR TM

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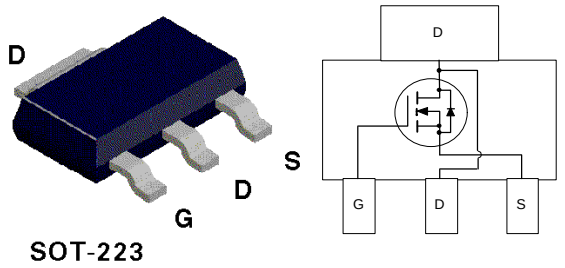
# NDT451AN
# N-Channel Enhancement Mode Field Effect Transistor

## General Description

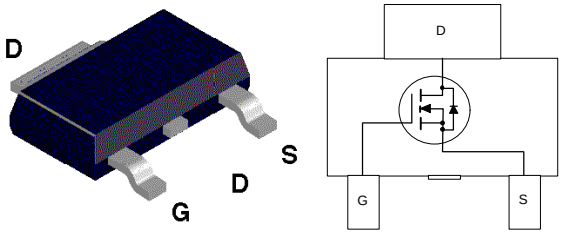
Power SOT N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

## Features

- 7.2A, 30V. $R_{DS(ON)}$ = 0.035Ω @ $V_{GS}$ = 10V
  $R_{DS(ON)}$ = 0.05Ω @ $V_{GS}$ = 4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.




SOT-223




SOT-223*
(J23Z)

## Absolute Maximum Ratings

$T_A$= 25°C unless otherwise noted

| Symbol | Parameter | | NDT451AN | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ± 20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | ± 7.2 | A |
| | - Pulsed | | ± 25 | |
| $P_D$ | Maximum Power Dissipation | (Note 1a) | 3 | W |
| | | (Note 1b) | 1.3 | |
| | | (Note 1c) | 1.1 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | | -65 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 42 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 12 | °C/W |

* Order option J23Z for cropped center drain lead.

## Electrical Characteristics ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $T_J$ = 55°C | | | 10 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.6 | 3 | V |
| | | $T_J$ = 125°C | 0.7 | 1.2 | 2.2 | |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 7.2 A | | 0.03 | 0.035 | Ω |
| | | $T_J$ = 125°C | | 0.042 | 0.063 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 6.0 A | | 0.042 | 0.05 | |
| | | $T_J$ = 125°C | | 0.058 | 0.09 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 25 | | | A |
| | | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | 15 | | | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 7.2 A | | 11 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 720 | | pF |
| $C_{oss}$ | Output Capacitance | | | 370 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 250 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 1 A, $V_{GEN}$ = 10 V, $R_{GEN}$ = 6 Ω | | 12 | 20 | ns |
| $t_r$ | Turn - On Rise Time | | | 13 | 30 | ns |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 29 | 50 | ns |
| $t_f$ | Turn - Off Fall Time | | | 10 | 20 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 10 V, $I_D$ = 7.2 A, $V_{GS}$ = 10 V | | 19 | 30 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 2.3 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 5.5 | | nC |

## Electrical Characteristics ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.3 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 7.2A (Note 2) | | 0.9 | 1.3 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_F$ = 1.25 A, $dI_F/dt$ = 100 A/µs | | | 100 | ns |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

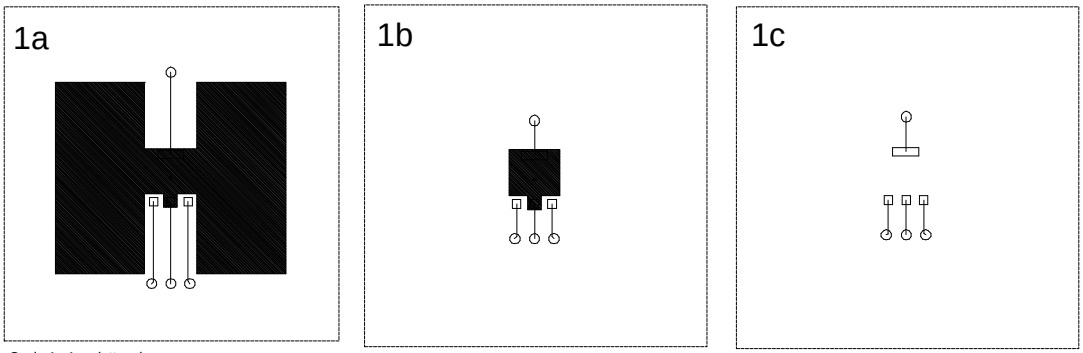
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 42°C/W when mounted on a 1 $in^2$ pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 $in^2$ pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 $in^2$ pad of 2oz copper.




Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

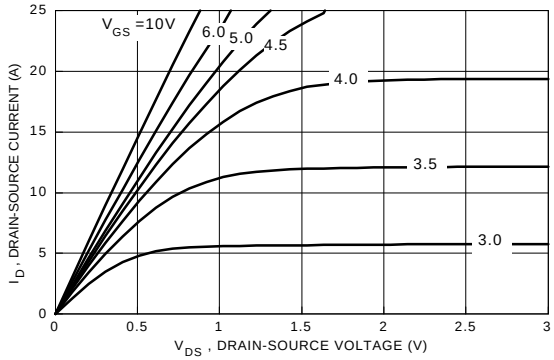



**Figure 1. On-Region Characteristics.**

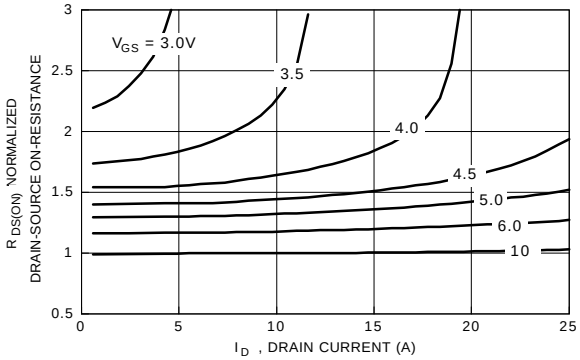



**Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.**

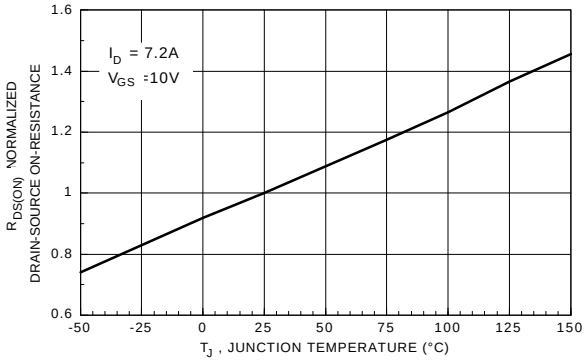



**Figure 3. On-Resistance Variation with Temperature.**

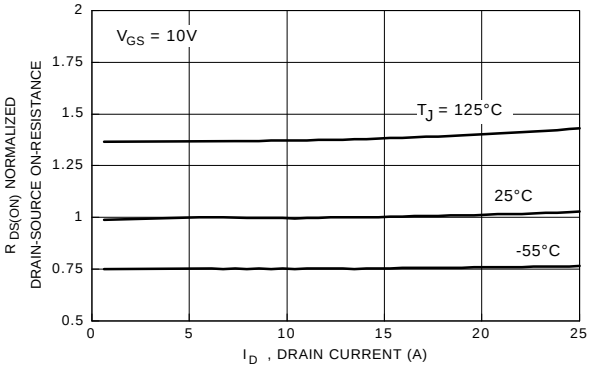



**Figure 4. On-Resistance Variation with Drain Current and Temperature.**

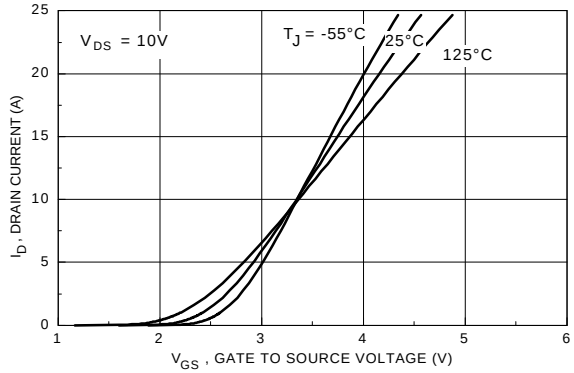



**Figure 5. Transfer Characteristics.**

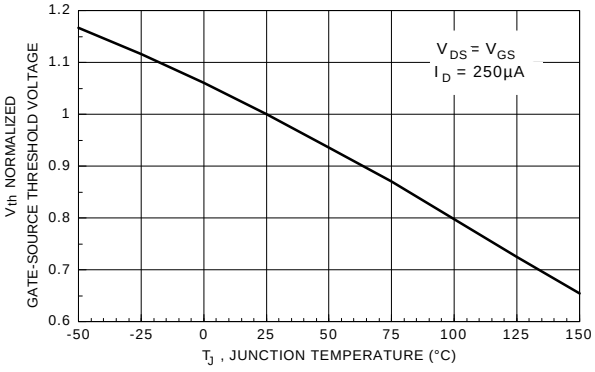



**Figure 6. Gate Threshold Variation with Temperature.**

## Typical Electrical Characteristics

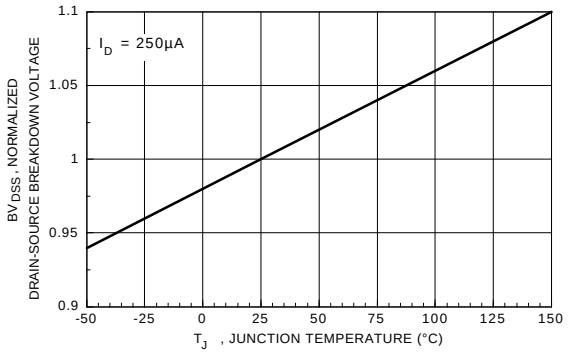



**Figure 7. Breakdown Voltage Variation with Temperature.**

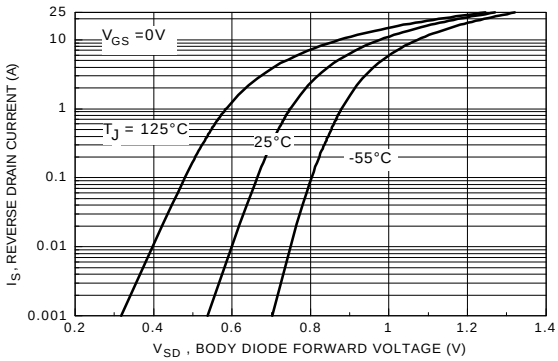



**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.**

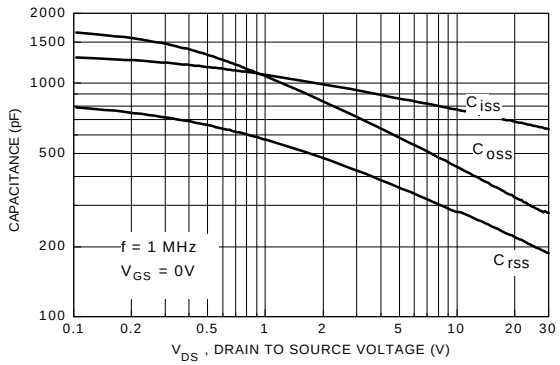



**Figure 9. Capacitance Characteristics.**

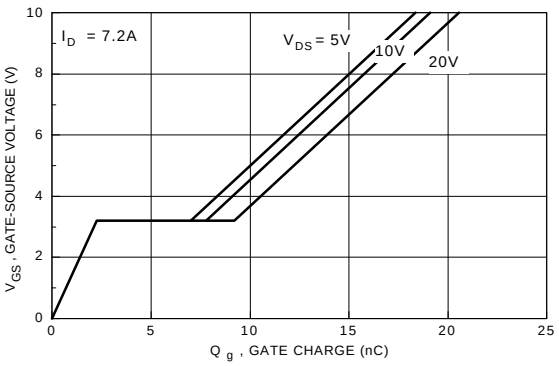



**Figure 10. Gate Charge Characteristics.**

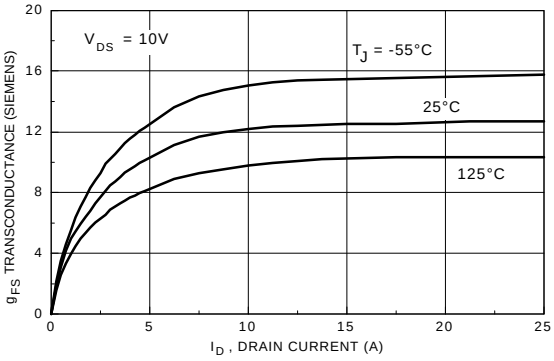



**Figure 11. Transconductance Variation with Drain Current and Temperature.**

## Typical Thermal Characteristics

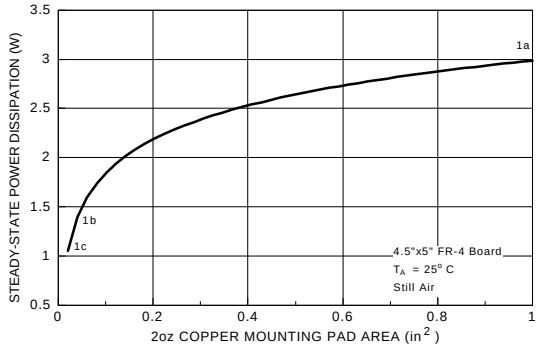



**Figure 12. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**

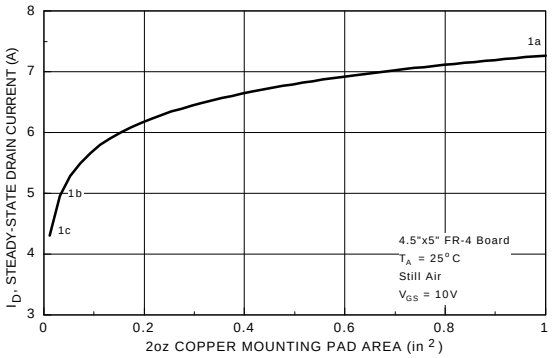



**Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**

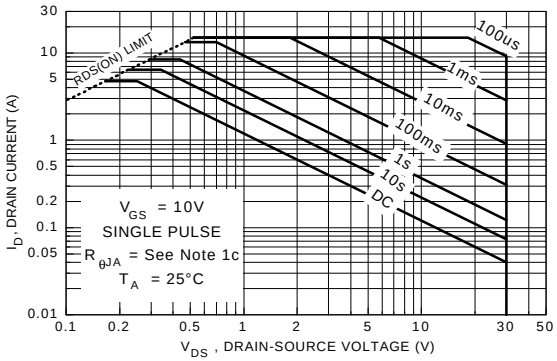



**Figure 14. Maximum Safe Operating Area.**

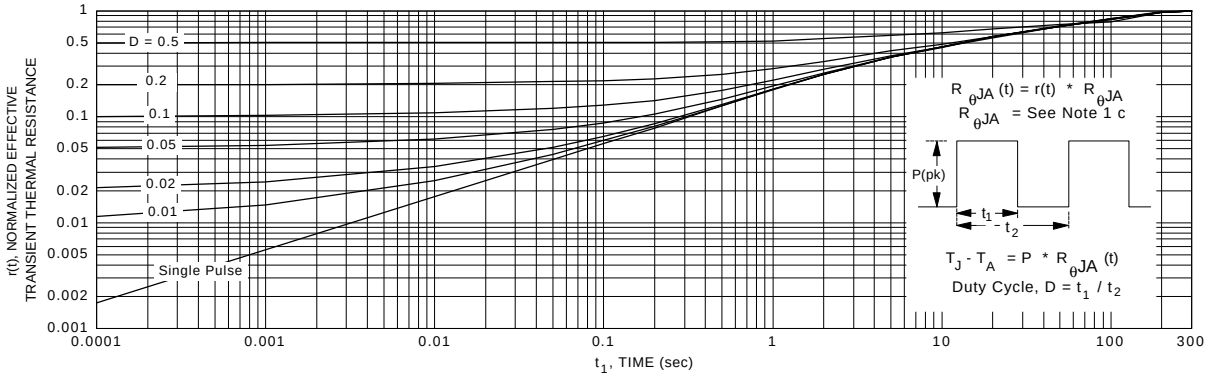



**Figure 15. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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