# Mobile SDRAM

## MT48LC8M32LF, MT48V8M32LF, MT48H8M32LF - 2 Meg x 32 x 4 banks

For the latest data sheet, refer to Micron's Web site: www.micron.com/products/dram/mobile

## Features

- Low voltage power supply
- Partial array self refresh power-saving mode
- Temperature Compensated Self Refresh (TCSR)
- Deep power-down mode
- Programmable output drive strength
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge, and auto refresh modes
- Self-refresh mode; standard and low power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Commercial and industrial temperature ranges
- Supports CAS latency of 1, 2, 3

| Options | Marking |
|---|---|
| • VDD/VDDQ | |
| • 3.3V/3.3V | LC |
| • 2.5V/2.5V | V |
| • 1.8V/1.8V | H |
| • Configurations | |
| • 8 Meg x 32 (2 Meg x 32 x 4 banks) | 8M32 |
| • Package/Ballout | |
| • 90-ball VFBGA (8mm x 13mm) (Standard) | F5 |
| • 90-ball VFBGA (8mm x 13mm) (Lead-free) | B5 |
| • Timing (Cycle Time) | |
| • 7.5ns @ CL = 3 (133 MHz) | -75 |
| • 7.5ns @ CL = 2 (104 MHz) | -75 |
| • 8ns @ CL = 3 (125 MHz) | -8 |
| • 8ns @ CL = 2 (104 Mhz) | -8 |
| • 10ns @ CL = 3 (100 MHz) | -10 |
| • 10ns @ CL = 2 (83 Mhz) | -10 |
| • Operating Temperature Range | |
| • Commercial (0° to +70°C) | None |
| • Industrial (-40°C to +85°C) | IT |

### Table 1: Addressing

| | 8 Meg x 32 |
|---|---|
| Configuration | 2 Meg x 32 x 4 banks |
| Refresh Count | 4K |
| Row Addressing | 4K (A0–A11) |
| Bank Addressing | 4 (BA0, BA1) |
| Column Addressing | 512 (A0–A8) |

### Table 2: Key Timing Parameters

CL = CAS (READ) latency

| Speed Grade | Clock Frequency | Access Time | | Setup Time | Hold Time |
|---|---|---|---|---|---|
| | | CL = 2 | CL = 3 | | |
| -75 | 133 MHz | – | 6ns | 2.5ns | 1ns |
| -8 | 125 MHz | – | 7ns | 2.5ns | 1ns |
| -10 | 100 MHz | – | 7ns | 2.5ns | 1ns |
| -75 | 133 MHz | 7ns | – | 2.5ns | 1ns |
| -8 | 104 MHz | 8ns | – | 2.5ns | 1ns |
| -10 | 83 MHz | 8ns | - | 2.5ns | 1ns |

## Table of Contents

## List of Figures

## List of Tables

### Table 3: Cross Reference For VFBGA Device Marking

| Part Number | $V_{DD}/V_{DD}Q$ | Architecture | VFBGA | Production Marking |
|---|---|---|---|---|
| MT48LC8M32LFF5-75 | 3.3V/3.3V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9FMQ |
| MT48LC8M32LFF5-8 | 3.3V/3.3V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CCH |
| MT48LC8M32LFF5-10 | 3.3V/3.3V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CCK |
| MT48LC8M32LFB5-75 | 3.3V/3.3V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9FMX |
| MT48LC8M32LFB5-8 | 3.3V/3.3V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CCW |
| MT48LC8M32LFB5-10 | 3.3V/3.3V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CCZ |
| MT48V8M32LFF5-75 | 2.5V/2.5V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9FMS |
| MT48V8M32LFF5-8 | 2.5V/2.5V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CCM |
| MT48V8M32LFF5-10 | 2.5V/2.5V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CCP |
| MT48V8M32LFB5-75 | 2.5V/2.5V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9FMZ |
| MT48V8M32LFB5-8 | 2.5V/2.5V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CDC |
| MT48V8M32LFB5-10 | 2.5V/2.5V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CDF |
| MT48H8M32LFF5-75 | 1.8V/1.8V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9FMV |
| MT48H8M32LFF5-8 | 1.8V/1.8V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CCR |
| MT48H8M32LFF5-10 | 1.8V/1.8V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CCT |
| MT48H8M32LFB5-75 | 1.8V/1.8V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9FNB |
| MT48H8M32LFB5-8 | 1.8V/1.8V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CDJ |
| MT48H8M32LFB5-10 | 1.8V/1.8V | 8 Meg x 32 | 90-ball, 8 x 13mm | D9CDL |

## FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA part marking decoder on Micron's Web site, www.micron.com/decoder.

## General Description

The Micron® 256Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 67,108,864-bit banks is organized as 4,096 rows by 512 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

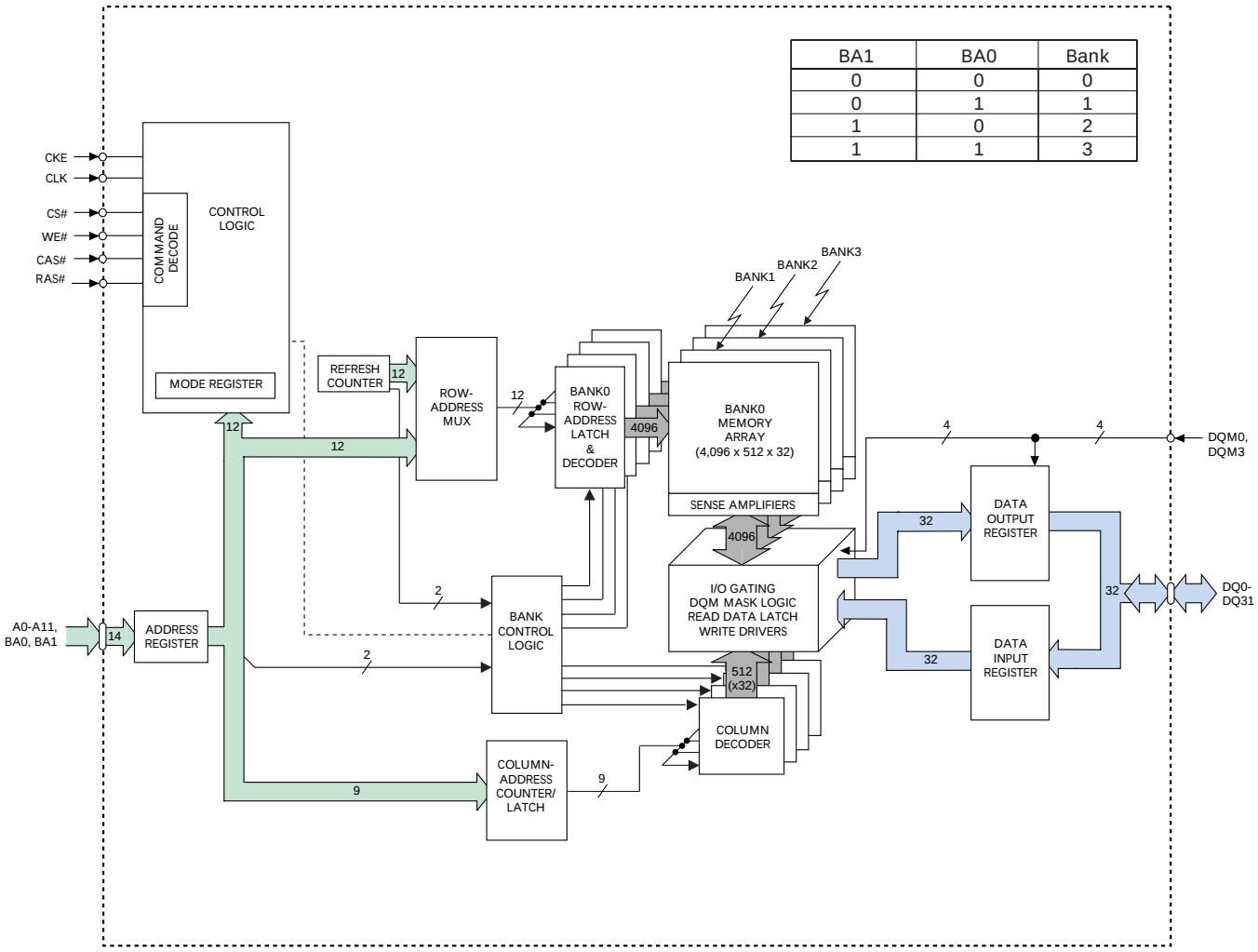
The 256Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-

speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 256Mb SDRAM is designed to operate in 3.3V, 2.5V, and 1.8V low-power memory systems. An auto refresh mode is provided, along with a power-saving, deep power-down mode. All inputs and outputs are LVTTL-compatible.

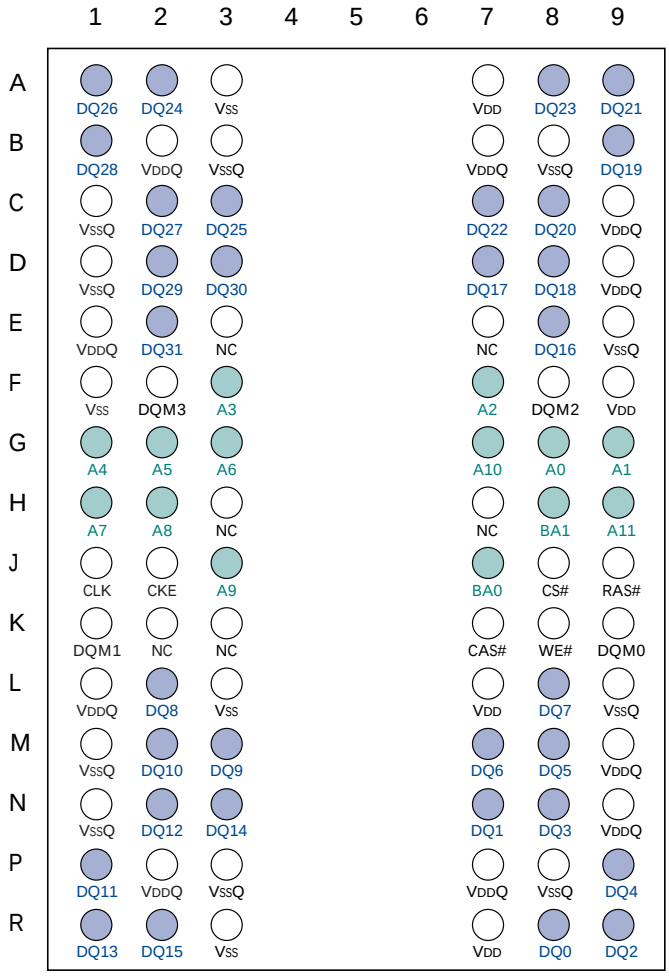
SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

## Figure 1: Functional Block Diagram 8 Meg x 32 SDRAM



# Ball Assignment

## Figure 2: 90-Ball VFBGA (Top View)



# Ball Descriptions

## Table 4: Ball Descriptions

| 90-Ball VFBGA | Symbol | Type | Description |
|---|---|---|---|
| J1 | CLK | Input | Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers. |
| J2 | CKE | Input | Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank), DEEP POWER DOWN (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. |
| J8 | CS# | Input | Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. |
| J9, K7, K8 | RAS#,CAS#, WE# | Input | Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered. |
| K9, K1, F8, F2 | DQM0-3 | Input | Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. DQM0 corresponds to DQ0-DQ7, DQM1 corresponds to DQ8-DQ15, DQM2 corresponds to DQ16-DQ23, and DQM3 corresponds to DQ24-DQ31. DQM0-3 are considered same state when referenced as DQM. |
| J7, H8 | BA0, BA1 | Input | Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. These balls also provide the op-code during a LOAD MODE REGISTER command |
| G8, G9, F7, F3, G1, G2, G3, H1, H2, J3, G7,H9 | A0–A11 | Input | Address Inputs: A0–A11 are sampled during the ACTIVE command (row-address A0–A11) and READ/WRITE command (column-address A0–A8; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command. |
| R8, N7, R9, N8, P9, M8, M7, L8, L2, M3, M2, P1, N2, R1, N3, R2, E8, D7, D8, B9, C8, A9, C7, A8, A2, C3, A1, C2, B1, D2, D3, E2 | DQ0–DQ31 | I/O | Data Input/Output: Data bus. |
| E3, E7, H3, H7, K2, K3 | NC | – | Internally Not Connected: These could be left unconnected, but it is recommended they be connected to $V_{SS}$. H3 is a no connect for this part, but may be used as A12 in future designs. |
| B2, B7, C9, D9, E1, L1, M9, N9, P2, P7 | $V_{DD}Q$ | Supply | DQ Power: Provide isolated power to DQs for improved noise immunity. |
| B3, B8, C1, D1, E9, L9, M1, N1, P3, P8 | $V_{SS}Q$ | Supply | DQ Ground: Provide isolated ground to DQs for improved noise immunity. |
| A7, F9, L7, R7 | $V_{DD}$ | Supply | Core Power Supply. |
| A3, F1, L3, R3 | $V_{SS}$ | Supply | Ground. |

# Functional Description

In general, the 256Mb SDRAMs (2 Meg x 32 x 4 banks) are quad-bank DRAMs that operate at 3.3V, 2.5V, and 1.8V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 67,108,864-bit banks is organized as 4,096 rows by 512 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0–A11 select the row). The address bits (A0–A8) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

# Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once the power is applied to $V_{DD}$ and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

# Register Definition

## Mode Register

In order to achieve low power consumption, there are two mode registers in the component: mode register and extended mode register. Extended mode register is illustrated in Figure 5. The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 3. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 should be set to zero. M12 and M13 should be set to zero to prevent the extended mode register from being programmed.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

## Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 3. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

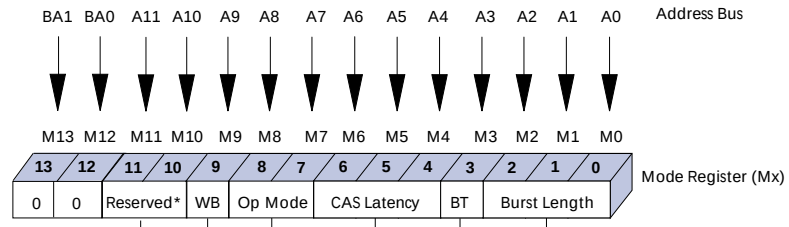
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A8 when BL = 2, A2–A8 when BL = 4, and A3–A8 when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

## Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 4.

## Figure 3: Mode Register Definition




*Should program
M10 = "0, 0"
to ensure compatibility
with future devices.

| | Burst Length | |
|---|---|---|
| M2 M1 M0 | M3 = 0 | M3 = 1 |
| 0 0 0 | 1 | 1 |
| 0 0 1 | 2 | 2 |
| 0 1 0 | 4 | 4 |
| 0 1 1 | 8 | 8 |
| 1 0 0 | Reserved | Reserved |
| 1 0 1 | Reserved | Reserved |
| 1 1 0 | Reserved | Reserved |
| 1 1 1 | Full Page | Reserved |

| M3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleaved |

| M6 M5 M4 | CAS Latency |
|---|---|
| 0 0 0 | Reserved |
| 0 0 1 | 1 |
| 0 1 0 | 2 |
| 0 1 1 | 3 |
| 1 0 0 | Reserved |
| 1 0 1 | Reserved |
| 1 1 0 | Reserved |
| 1 1 1 | Reserved |

| M8 | M7 | M6-M0 | Operating Mode |
|---|---|---|---|
| 0 | 0 | Defined | Standard Operation |
| - | - | - | All other states reserved |

| M9 | Write Burst Mode |
|---|---|
| 0 | Programmed Burst Length |
| 1 | Single Location Access |

## Table 5: Burst Definition Table

| Burst Length | Starting Column Address | | | Order of Accesses Within a Burst | |
|---|---|---|---|---|---|
| | | | | Type = Sequential | Type = Interleaved |
| 2 | | | A0 | | |
| | | | 0 | 0-1 | 0-1 |
| | | | 1 | 1-0 | 1-0 |
| 4 | | A1 | A0 | | |
| | | 0 | 0 | 0-1-2-3 | 0-1-2-3 |
| | | 0 | 1 | 1-2-3-0 | 1-0-3-2 |
| | | 1 | 0 | 2-3-0-1 | 2-3-0-1 |
| | | 1 | 1 | 3-0-1-2 | 3-2-1-0 |
| 8 | A2 | A1 | A0 | | |
| | 0 | 0 | 0 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 |
| | 0 | 0 | 1 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 |
| | 0 | 1 | 0 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 |
| | 0 | 1 | 1 | 3-4-5-6-7-0-1-2 | 3-2-1-0-7-6-5-4 |
| | 1 | 0 | 0 | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 |
| | 1 | 0 | 1 | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 |
| | 1 | 1 | 0 | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 |
| | 1 | 1 | 1 | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 |
| Full Page (y) | n = A0-A11/9/8 (location 0-y) | | | Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn... | Not Supported |

Notes:
1. For full-page accesses: y = 512.
2. For BL = 2, A1–A8 select the block-of-two burst; A0 selects the starting column within the block.
3. For BL = 4, A2–A8 select the block-of-four burst; A0-A1 select the starting column within the block.
4. For BL = 8, A3–A8 select the block-of-eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A8 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For BL = 1, A0–A8 select the unique column to be accessed, and mode register bit M3 is ignored.

## CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to one, two, or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a read command is registered at T0

and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 4. Table 5 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

### Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both read and write bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

### Write Burst Mode

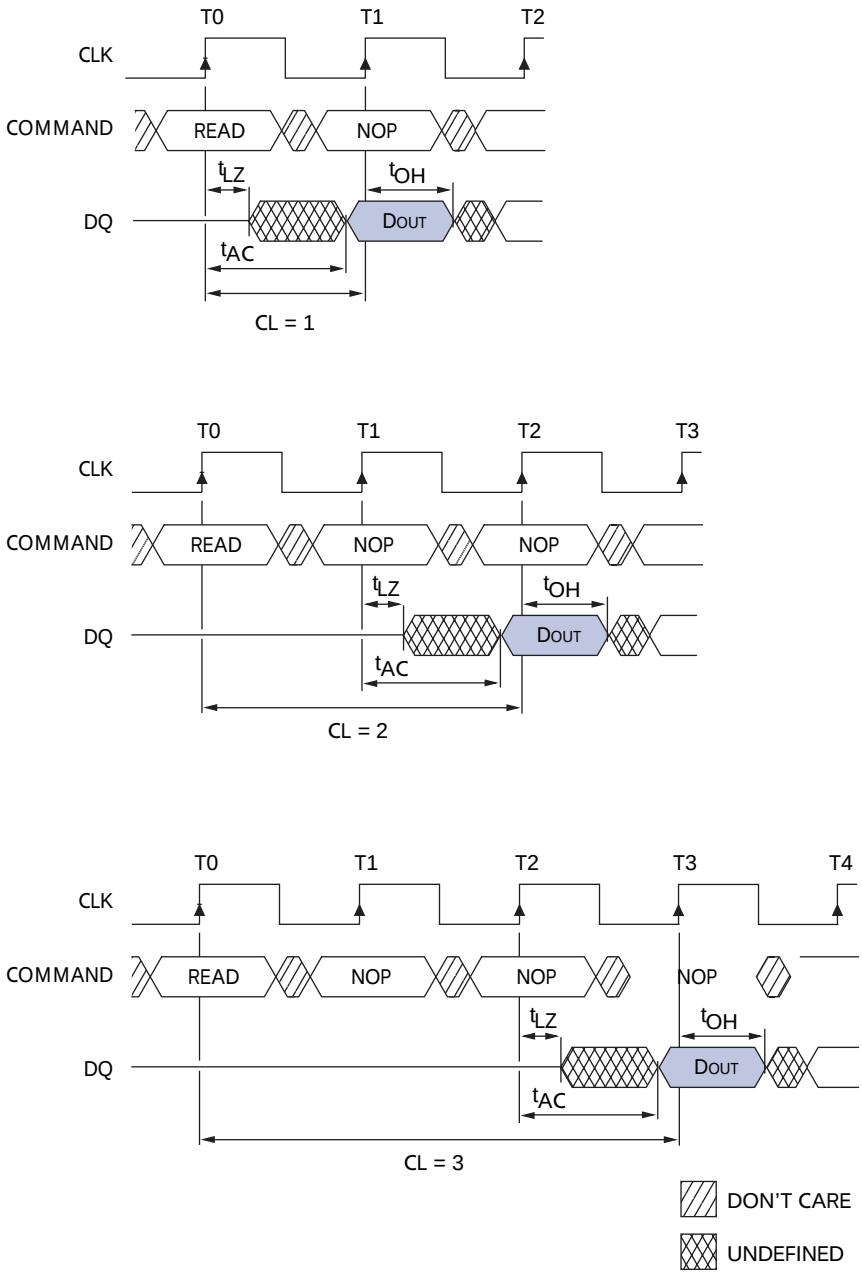
When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9= 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

## Low-Power Extended Mode Register Definition

The low-power extended mode register controls the functions beyond those controlled by the mode register. These additional functions are special features of the mobile device. They include temperature compensated self refresh (TCSR) control, partial array self refresh (PASR), and output drive strength. Not programming the extended mode register upon initialization will result in default settings for the low-power features. The extended mode will default with the temperature sensor enabled, full drive strength, and full array refresh.

The low-power extended mode register is programmed via the MODE REGISTER SET command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

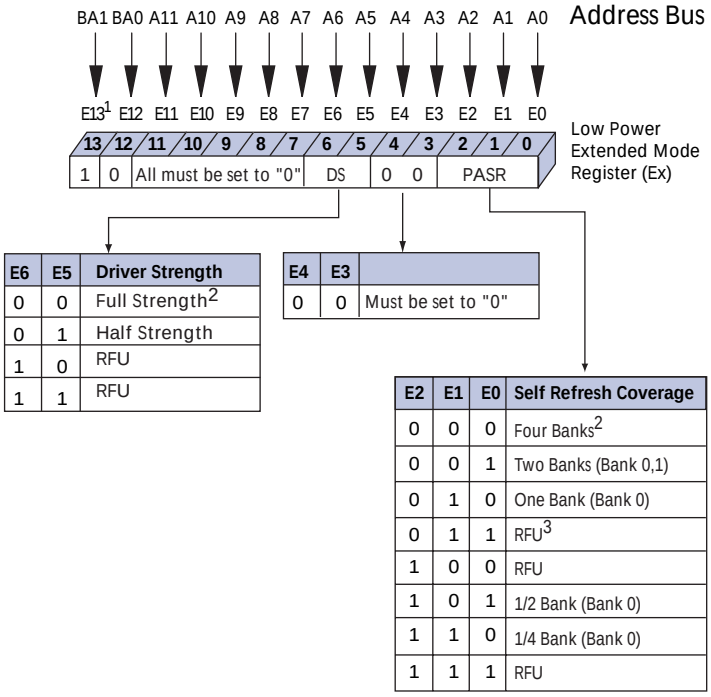
## Figure 4: CAS Latency




## Table 6: CAS Latency

| Speed | Allowable Operating Frequency (MHz) | | |
|---|---|---|---|
| | CL = 1 | CL = 2 | CL = 3 |
| -75 | – | ≤104 | ≤133 |
| - 8 | ≤50 | ≤104 | ≤125 |
| -10 | ≤50 | ≤83.3 | ≤100 |

## Figure 5: Low Power Extended Mode Register Table




| E6 | E5 | Driver Strength |
|---|---|---|
| 0 | 0 | Full Strength[2] |
| 0 | 1 | Half Strength |
| 1 | 0 | RFU |
| 1 | 1 | RFU |

| E4 | E3 | |
|---|---|---|
| 0 | 0 | Must be set to "0" |

| E2 | E1 | E0 | Self Refresh Coverage |
|---|---|---|---|
| 0 | 0 | 0 | Four Banks[2] |
| 0 | 0 | 1 | Two Banks (Bank 0,1) |
| 0 | 1 | 0 | One Bank (Bank 0) |
| 0 | 1 | 1 | RFU[3] |
| 1 | 0 | 0 | RFU |
| 1 | 0 | 1 | 1/2 Bank (Bank 0) |
| 1 | 1 | 0 | 1/4 Bank (Bank 0) |
| 1 | 1 | 1 | RFU |

Notes: 1. E13 and E12 (BA1 and BA0) must be “1, 0” to select the extended mode register (vs. the base mode register).
2. Default EMR values are full array for PASR, full drive strength.
3. RFU: reserved for future use.
4. E4 and E3 are “Don’t Care.”

The low-power extended mode register must be programmed with E7 through E11 set to “0”. It must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. Once the values are entered, the extended mode register settings will be retained even after exiting deep power-down mode.

### Temperature Compensated Self Refresh

Temperature compensated self refresh (TCSR) allows the controller to program the refresh interval during self refresh mode, according to the case temperature of the Mobile device. This allows great power savings during self refresh during most operating temperature ranges. Only during extreme temperatures would the controller have to select the maximum TCSR level. This would guarantee data during self refresh.

Every cell in the DRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. Historically, during self refresh, the refresh rate has been set to accommodate the worst case, or highest temperature range expected.

Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high because the refresh rate was set to accommodate the higher temperatures. This SDRAM has an on-chip temperature sensor that automatically adjusts refresh rate according to die temperature. The default setting for the TCSR is with the temperature sensor enabled.

### Partial Array Self Refresh

For further power savings during self refresh, the partial array self refresh (PASR) feature allows the controller to select the amount of memory that will be refreshed during self refresh. The refresh options are all banks (banks 0, 1, 2, and 3), two banks (banks 0 and 1), and one bank (bank 0). Also included in the refresh options are the half-bank and quarter-bank partial array self refresh (bank 0). WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during self refresh. It is important to note that data in banks 2 and 3 will be lost when the two bank option is used. Data will be lost in banks 1, 2, and 3 when the one bank option is used.

### Driver Strength

Bits E5 and E6 of the extended mode register can be used to select the driver strength of the DQ outputs. This value should be set according to the application's requirements. Full drive strength was carried over from standard SDRAM and is suitable to drive higher load systems.

# Commands

Table 7 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following "Operation" on page 21; these tables provide current state/next state information.

## Table 7: Truth Table – Commands and DQM Operation

CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER DOWN

| Name (Function) | CS# | RAS# | CAS# | WE# | DQM | ADDR | DQs | Notes |
|---|---|---|---|---|---|---|---|---|
| COMMAND INHIBIT (NOP) | H | X | X | X | X | X | X | |
| NO OPERATION (NOP) | L | H | H | H | X | X | X | |
| ACTIVE (Select bank and activate row) | L | L | H | H | X | Bank/Row | X | 1 |
| READ (Select bank and column, and start READ burst) | L | H | L | H | L/H[8] | Bank/Col | X | 2 |
| WRITE (Select bank and column, and start WRITE burst) | L | H | L | L | L/H[8] | Bank/Col | Valid | 2 |
| BURST TERMINATE or DEEP POWER DOWN (Enter deep power-down mode) | L | H | H | L | X | X | X | 3, 4 |
| PRECHARGE (Deactivate row in bank or banks) | L | L | H | L | X | Code | X | 5 |
| AUTO REFRESH or SELF REFRESH (Enter self refresh mode) | L | L | L | H | X | X | X | 6, 7 |
| LOAD MODE REGISTER | L | L | L | L | X | Op-Code | X | 8 |
| Write Enable/Output Enable | X | X | X | X | L | X | Active | 9 |
| Write Inhibit/Output High-Z | X | X | X | X | H | X | High-Z | 9 |

Notes:
1. A0–A11 provide row address, and BA0, BA1 determine which bank is made active.
2. A0–A8 provide column address; A10 HIGH enables the auto precharge feature (non persistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
3. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER DOWN when CKE is LOW.
4. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However the DQs column reads a don't care state to illustrate that the BURST TERMINATE command can occur when there is no data present.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. A0–A11 define the op-code written to the mode and extended mode register.
9. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay). DQM0 controls DQ0–DQ7; DQM1 controls DQ8–DQ15; DQM2 controls DQ16–DQ23; and DQM3 control DQ24–DQ31.

### COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected and the DQ balls tri-state. Operations already in progress are not affected.

### NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

### LOAD MODE REGISTER

The mode register is loaded via inputs A0, BA0, and BA1. (See "Mode Register" on page 9.) The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until $^{t}$MRD is met.

The values of the load mode register and extended mode register will be retained even when exiting deep power-down mode.

### ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

### READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

### WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

### PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time ($^{t}$RP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

### Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE com-

mand is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where auto precharge does not apply. Auto precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time ($^{t}$RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in "Operation" on page 21.

### BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in "Operation" on page 21.

### AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAMs. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum $^{t}$RP has been met after the PRECHARGE command, as shown in "Operation" on page 21.

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The 256Mb SDRAM requires 4,096 AUTO REFRESH cycles every 64ms ($^{t}$REF). Providing a distributed AUTO REFRESH command every 15.625µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate ($^{t}$RFC), once every 64ms.

### SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to $^{t}$RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for $^{t}$XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued every 15.625µs or less as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

## DEEP POWER-DOWN

DEEP POWER-DOWN is an operating mode to achieve maximum power reduction by eliminating the power of the whole memory array of the devices. Array data will not be retained once the device enters deep power-down mode. The settings in the mode and extended mode register will be retained during deep power-down.

This mode is entered by having all banks idle then CS# and WE# held LOW with RAS# and CAS# held HIGH at the rising edge of the clock, while CKE is LOW. This mode is exited by asserting CKE HIGH.

# Operation

## Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 5 on page 15).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the $^{t}$RCD specification. $^{t}$RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a $^{t}$RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 6 on page 21, which covers any case where $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by $^{t}$RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by $^{t}$RRD.

**Figure 6: Activating a Specific Row in a Specific Bank**

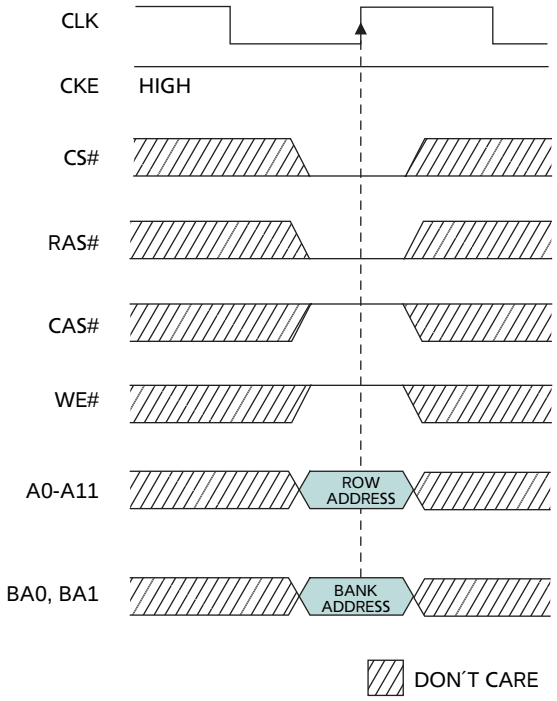
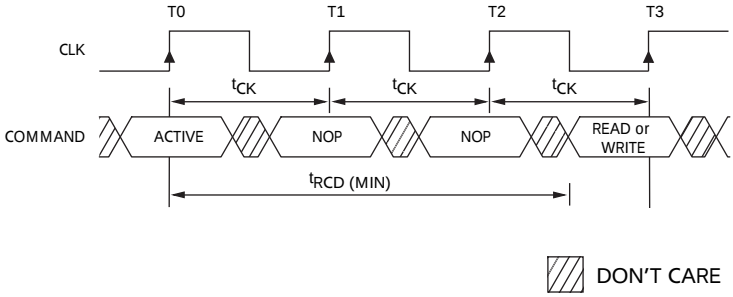


**Figure 7: Example: Meeting $^{t}$RCD (MIN) When 2 < $^{t}$RCD (MIN)/$^{t}$CK ≤ 3**



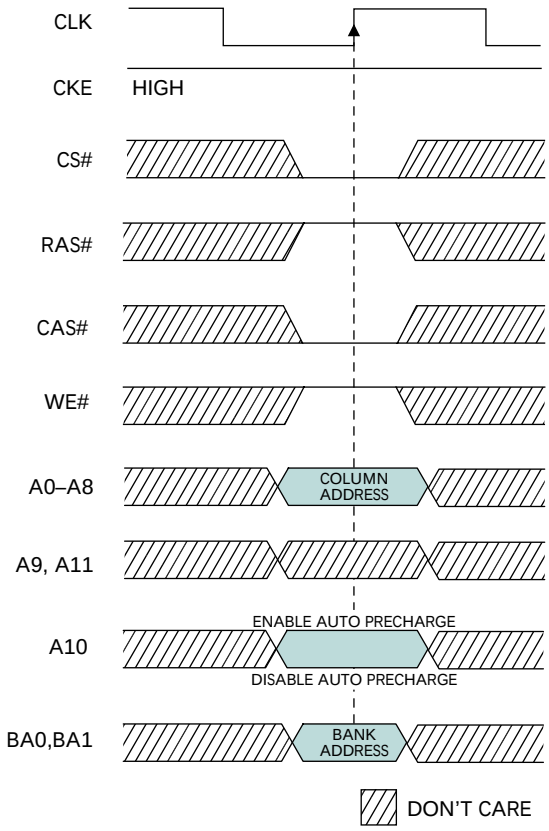

## READs

READ bursts are initiated with a READ command, as shown in Figure 8.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 9 shows general timing for each possible CAS latency setting.

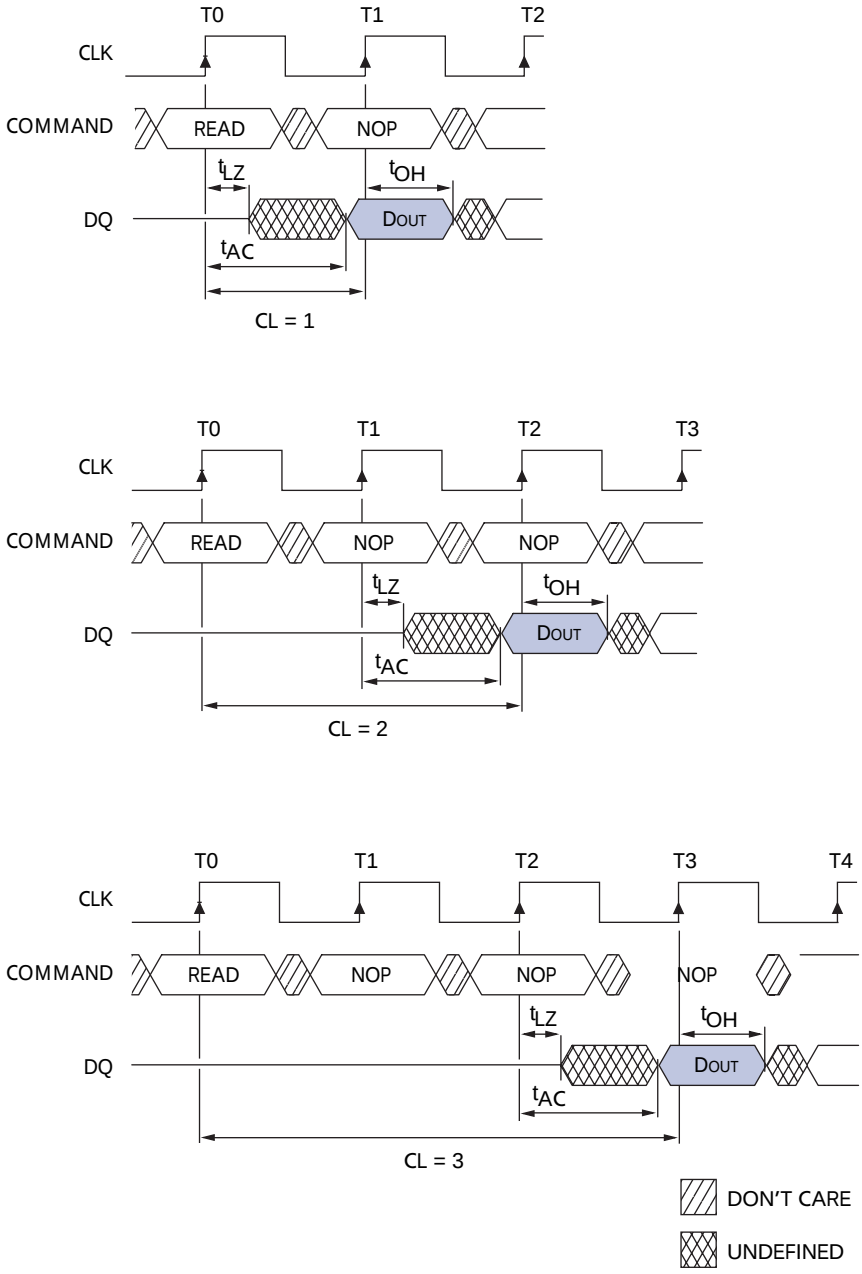
## Figure 8: READ Command




Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

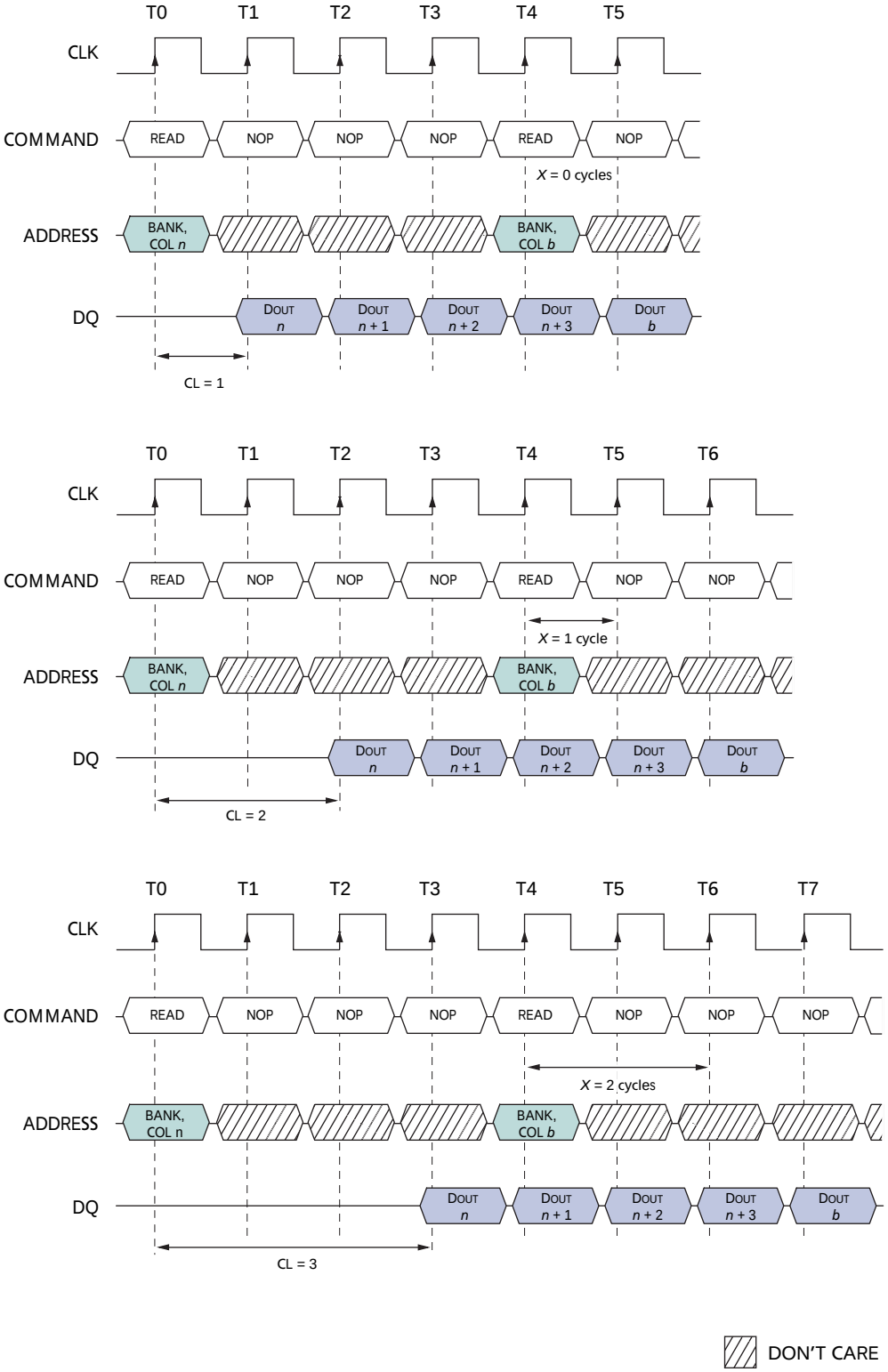
Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one.

## Figure 9: CAS Latency



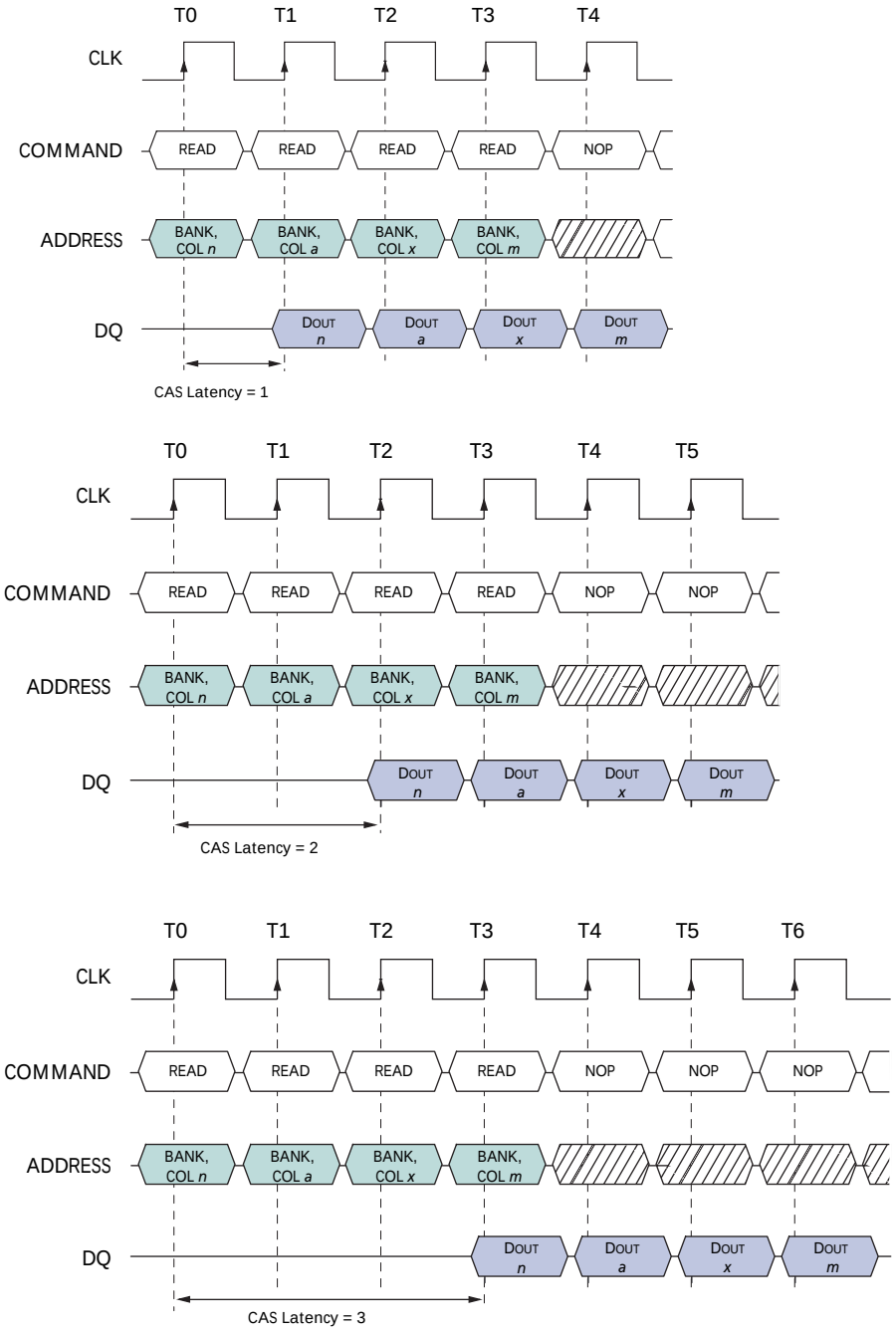

This is shown in Figure 10 for CAS latencies of one, two, and three; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. The 256Mb SDRAM uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 10 on page 25, or each subsequent READ may be performed to a different bank.

## Figure 10: Consecutive READ Bursts




Note: Each READ command may be to either bank. DQM is LOW.

## Figure 11: Random READ Accesses




**NOTE:** Each READ command may be to either bank. DQM is LOW.

Note: Each READ command may be to either bank. DQM is LOW.

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be

initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

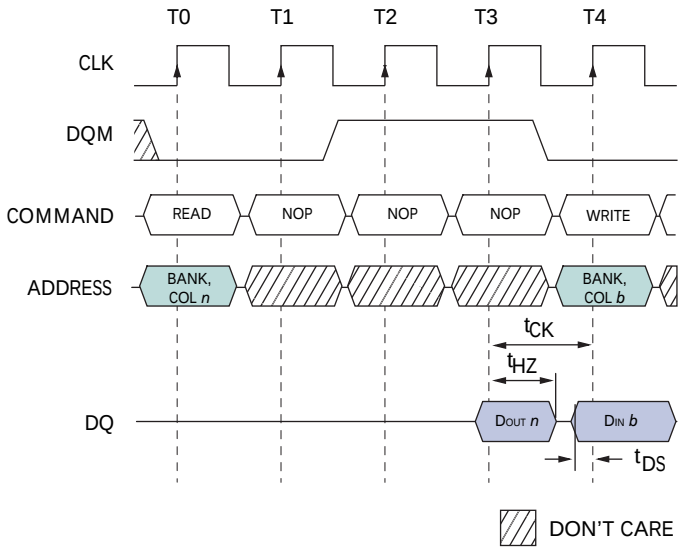
The DQM input is used to avoid I/O contention, as shown in Figure 11 on page 26 and Figure 12 on page 28. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 (in Figure 13) then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 12 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 13 shows the case where the additional NOP is needed.

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 13 on page 28 for each possible CAS latency; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until $^{t}$RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

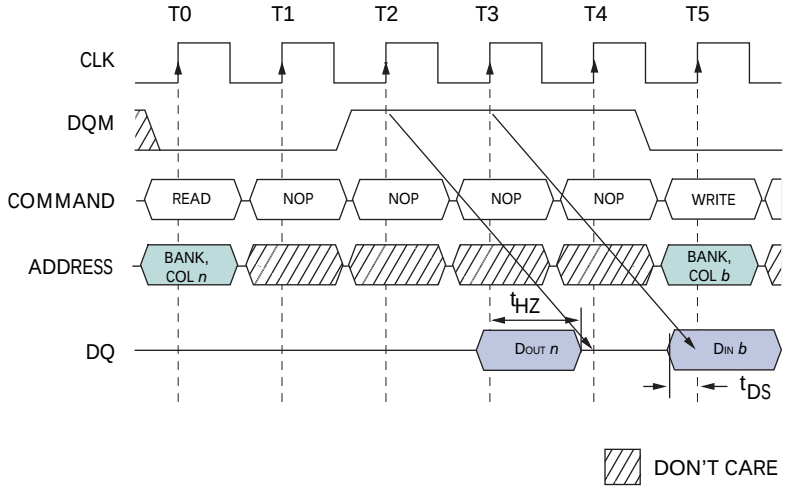
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

## Figure 12: READ to WRITE



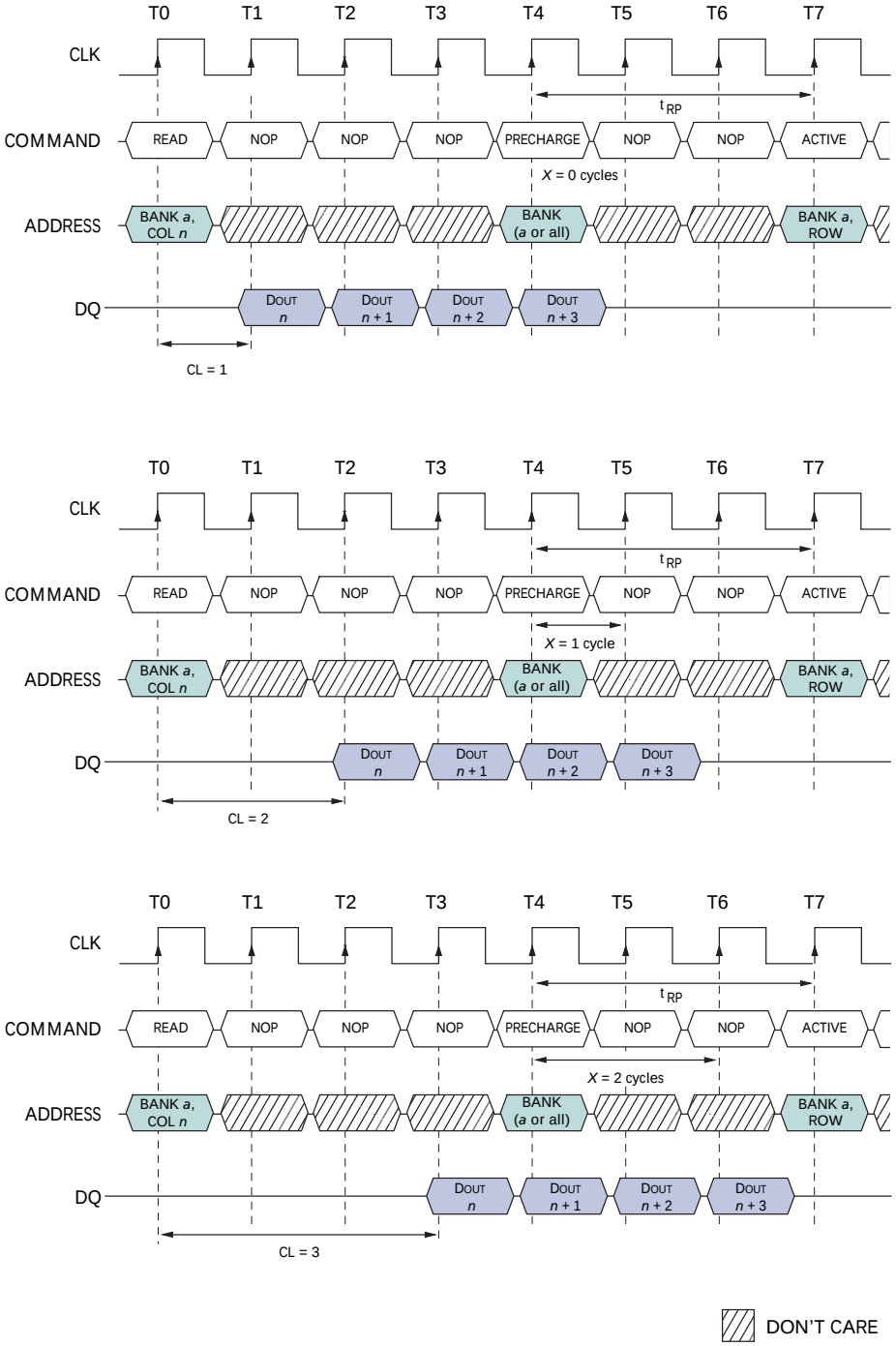

Note: CL = 3. The READ command may be to any bank, and the WRITE command may be to any bank. If a burst of one is used, then DQM is not required.

## Figure 13: READ to WRITE with Extra Clock Cycle




Note: CL = 3. The READ command may be to any bank, and the WRITE command may be to any bank.

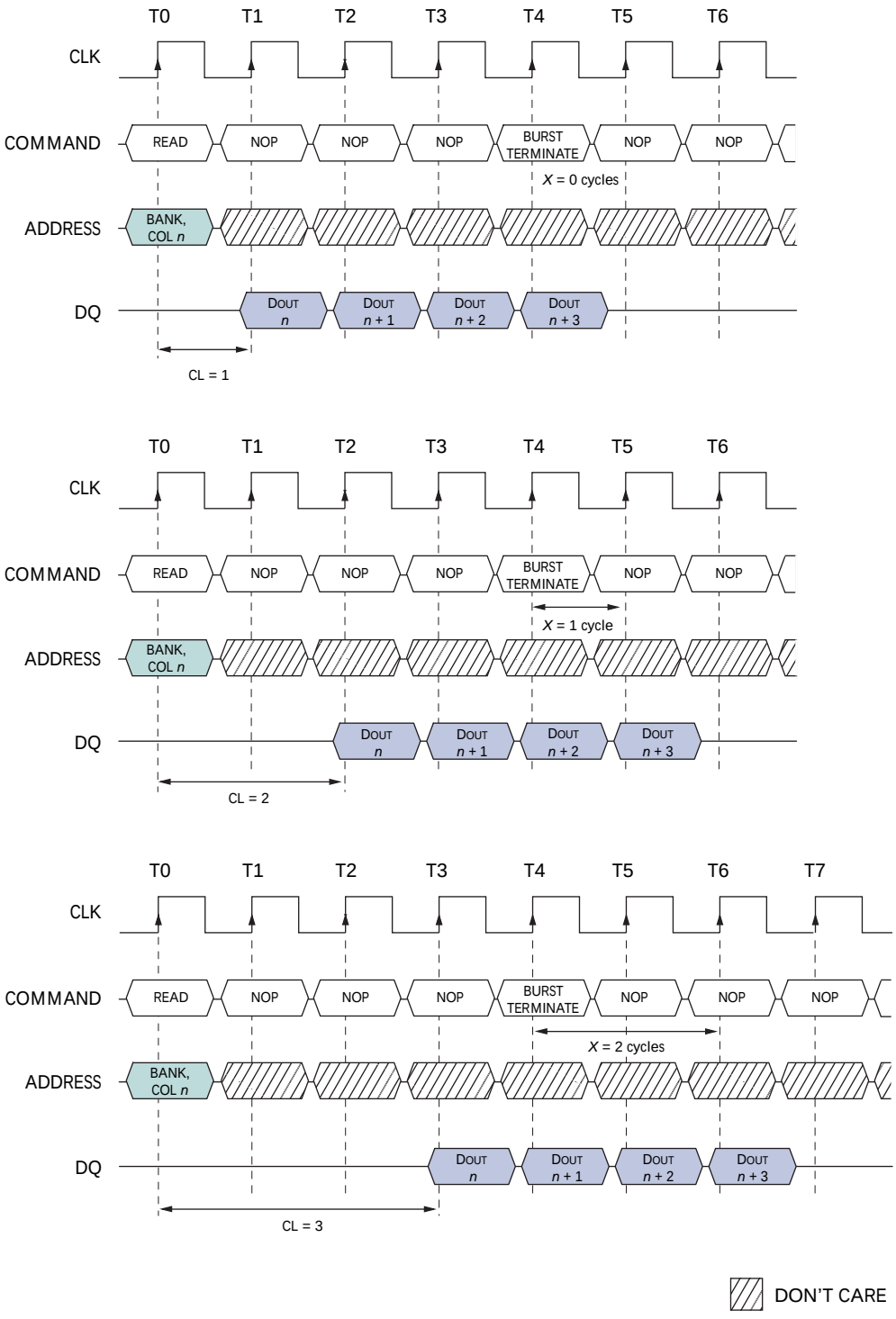
## Figure 14: READ to PRECHARGE




Note: DQM is LOW.

Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 15 for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

## Figure 15: Terminating a READ Burst




Note: DQM is LOW.

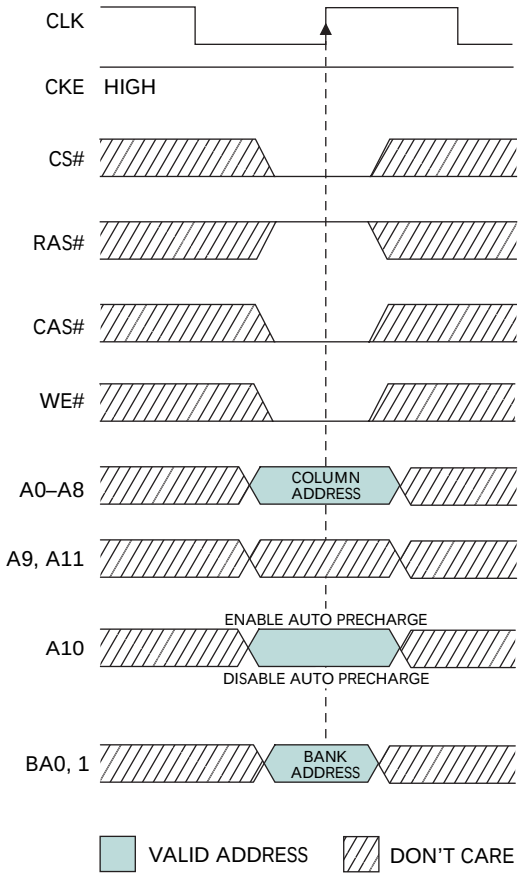
## WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 15 on page 30.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see Figure 17). A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

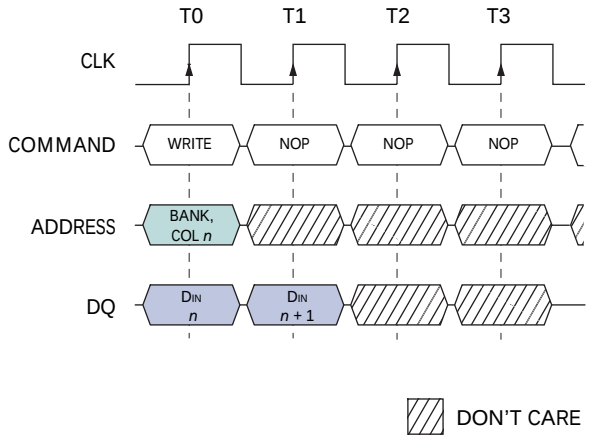
**Figure 16: WRITE Command**




Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 17 on page 32. Data $n + 1$ is either the last of a burst of two or the last desired of a longer burst. The 256Mb SDRAM uses a pipelined architecture and therefore does not require the 2n rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous

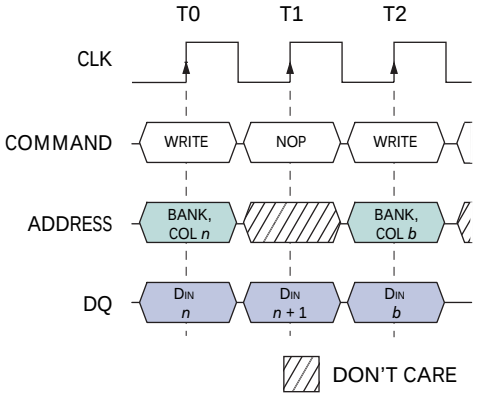
WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 19, or each subsequent WRITE may be performed to a different bank.

## Figure 17: WRITE Burst




Note: BL = 2. DQM is LOW.

## Figure 18: WRITE to WRITE




Note: DQM is LOW. Each WRITE command may be to any bank.

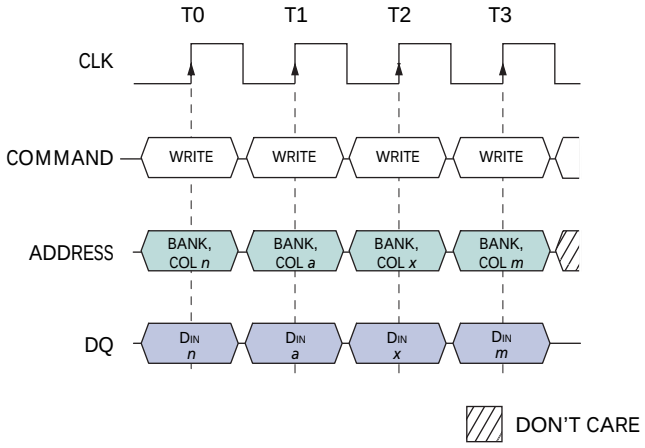
Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is registered, the data inputs will be ignored, and WRITEs will not be executed. An example is shown in Figure 19 on page 33. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued $^{t}$WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a $^{t}$WR of at least one clock plus time, regardless of frequency.

In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 21. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until $^{t}$RP is met.

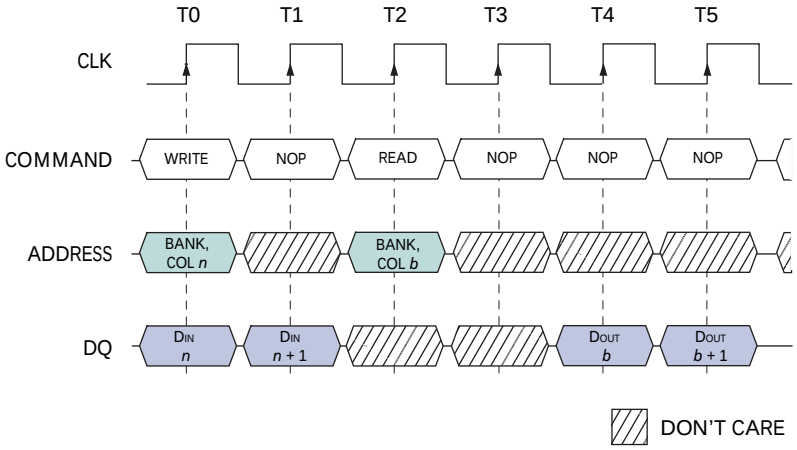
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

## Figure 19: Random WRITE Cycles



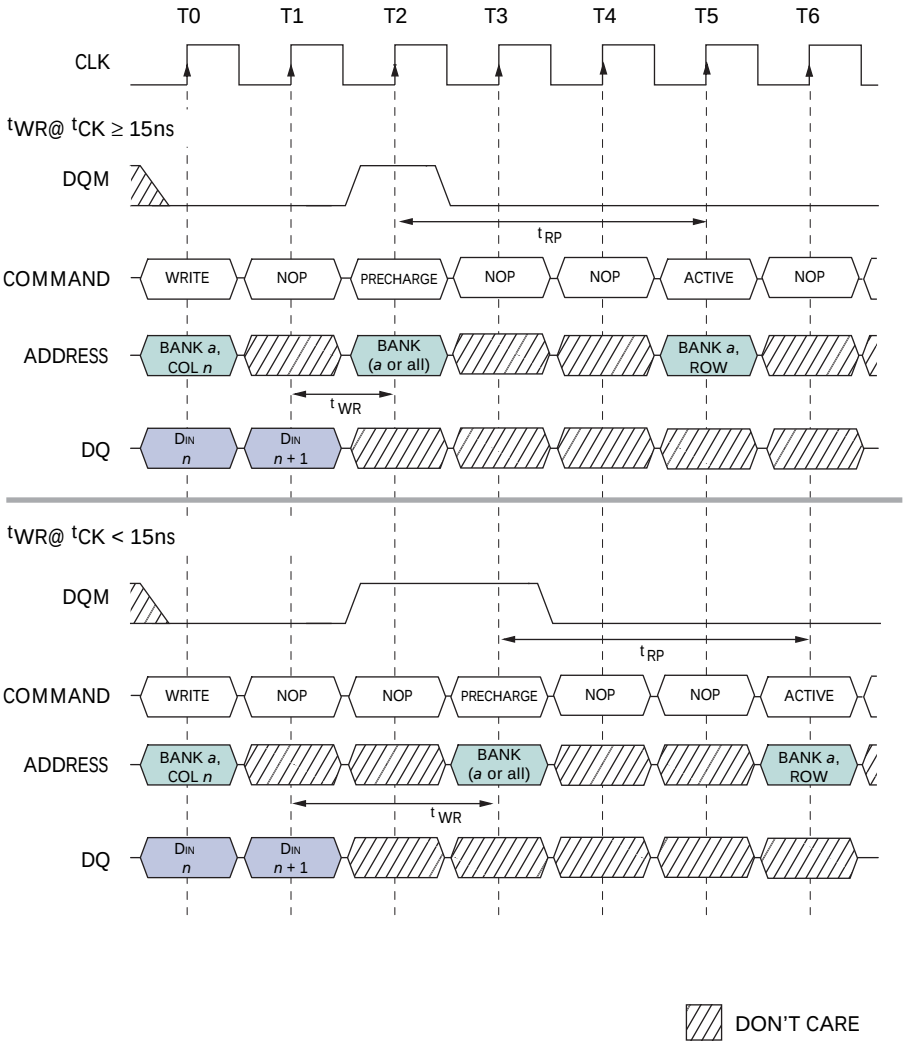

Note: Each WRITE command may be to any bank. DQM is LOW.

## Figure 20: WRITE to READ




Note: The WRITE command may be to any bank, and the READ command may be to any bank. DQM is LOW. CL = 2 for illustration.

## Figure 21: WRITE to PRECHARGE




Note: DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 22, where data *n* is the last desired data element of a longer burst.

### PRECHARGE

The PRECHARGE command (see Figure 23) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time ($^{t}$RP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

## POWER-DOWN

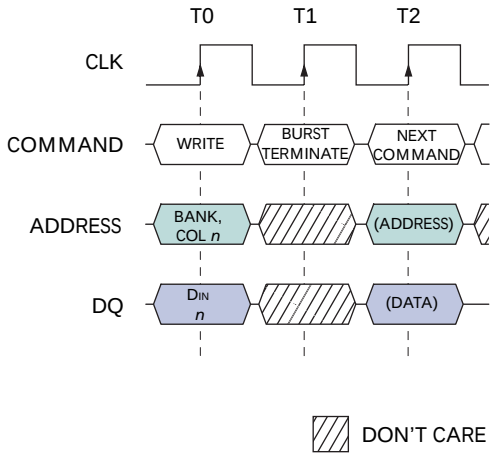
Power-down occurs if CKE is registered low coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no REFRESH operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting $^{t}$CKS). See Figure 24.

## DEEP POWER-DOWN

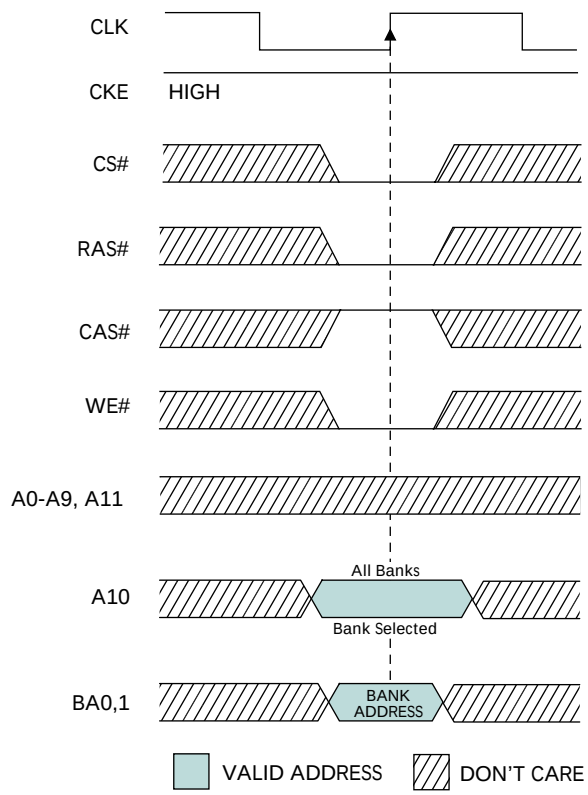
Deep power-down mode is a maximum power savings feature achieved by shutting off the power to the entire memory array of the device. Data on the memory array will not be retained once deep power-down mode is executed. Deep power-down mode is entered by having all banks idle then CS# and WE# held LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during deep power down.

## Figure 22: Terminating a WRITE Burst

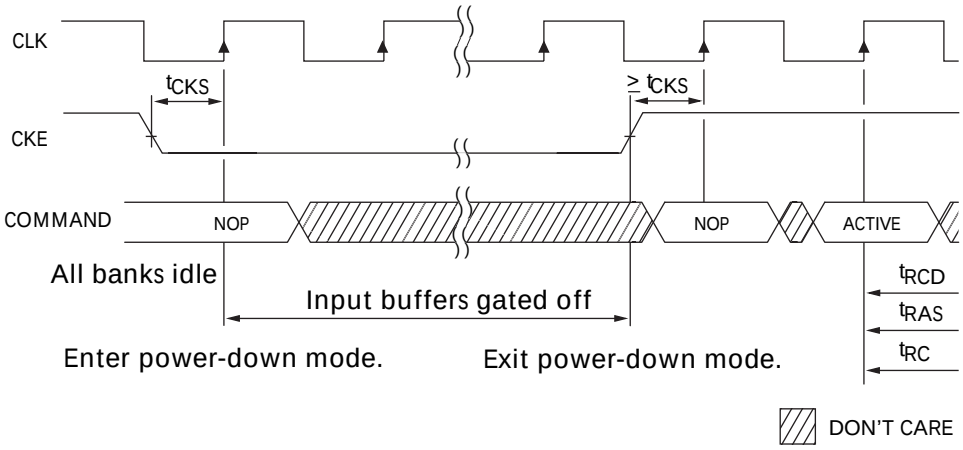



Note: DQMs are LOW.

## Figure 23: PRECHARGE Command




## Figure 24: Power-Down




In order to exit deep power-down mode, CKE must be asserted high. After exiting, the following sequence is needed in order to enter a new command:

1. Maintain NOP input conditions for a minimum of 100us.
2. Issue PRECHARGE commands for all banks.
3. Issue two or more AUTO REFRESH commands.

The values of the MODE REGISTER and EXTENDED MODE REGISTER will be retained upon exit deep power down.

## CLOCK SUSPEND

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls at the time of a suspended internal clock edge is ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended. (See examples in Figure 25 and Figure 26.)

Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

## BURST READ/SINGLE WRITE

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

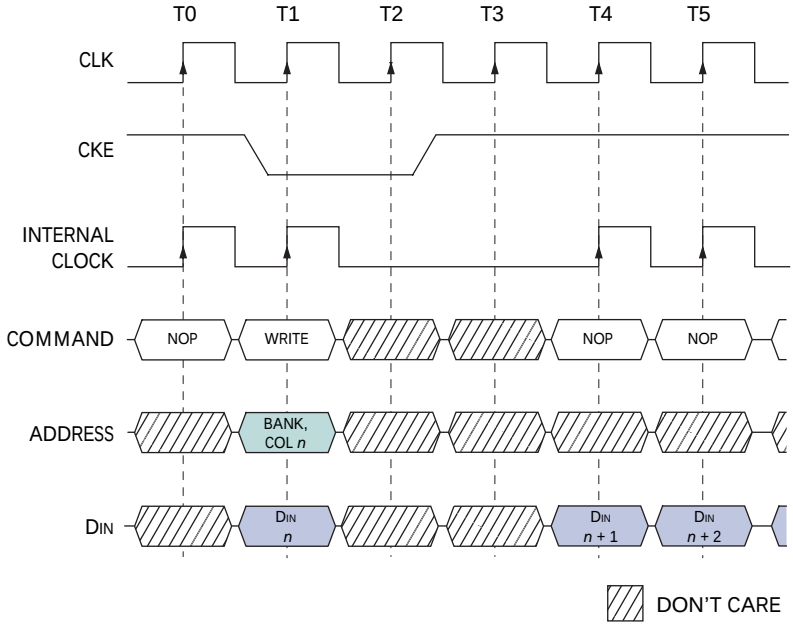
## Concurrent Auto Precharge

An access command (READ or WRITE) to a second bank while an access command with auto precharge enabled on a first bank is executing is not allowed by SDRAMs, unless the SDRAM supports concurrent auto precharge. Micron SDRAMs support concurrent auto precharge. Four cases where concurrent auto precharge occurs are defined below.

## READ with Auto Precharge

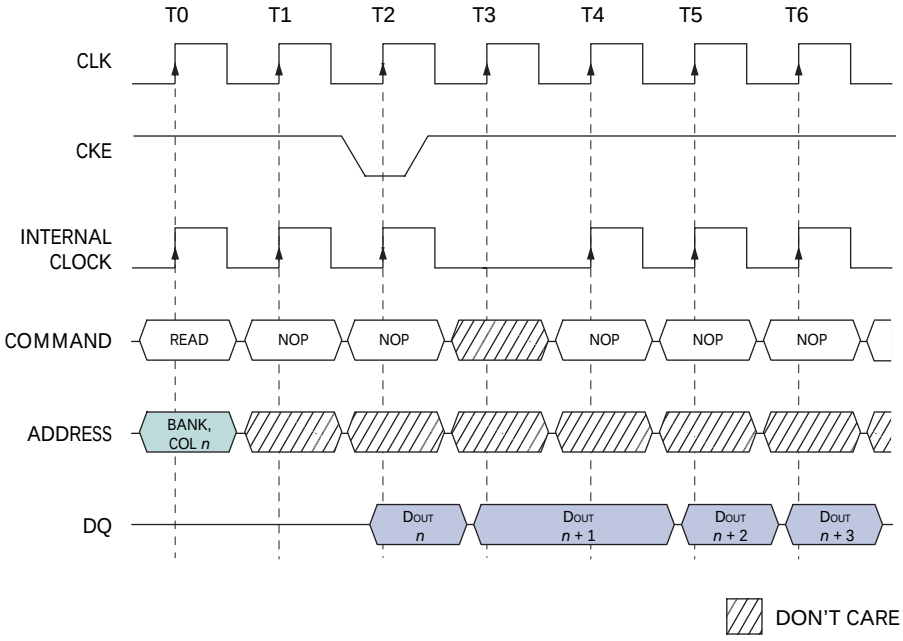
1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ on bank *n*, CAS latency later. The precharge to bank *n* will begin when the READ to bank *m* is registered (Figure 27).
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank *n* will begin when the WRITE to bank *m* is registered (Figure 28).

## Figure 25: Clock Suspend During WRITE Burst



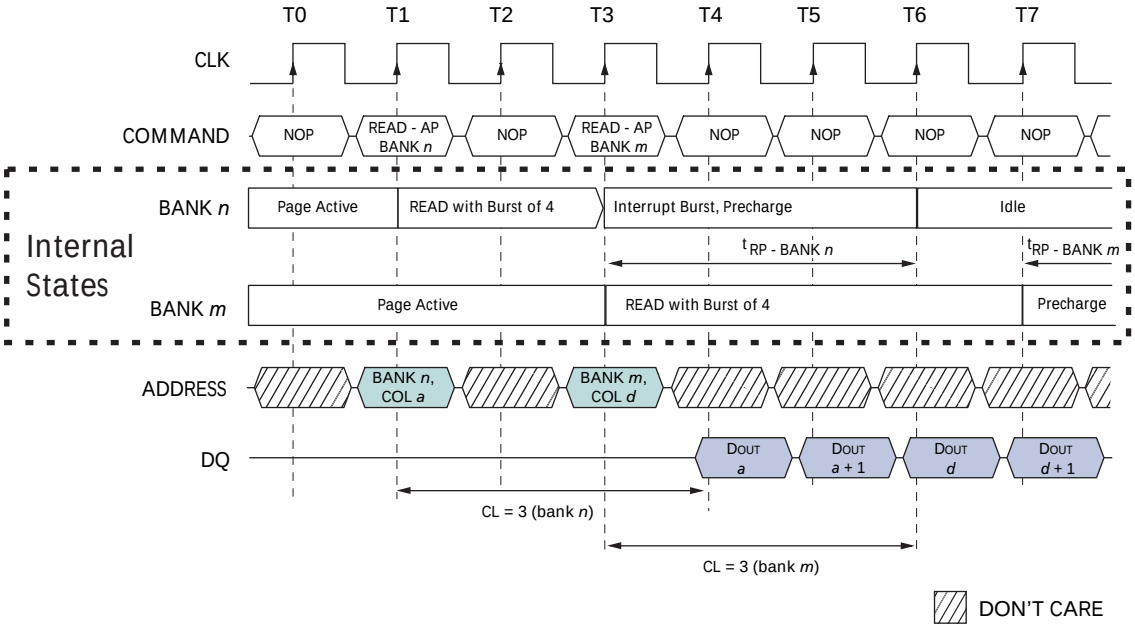

Note: For this example, BL = 4 or greater, and DM is LOW.

## Figure 26: Clock Suspend During READ Burst



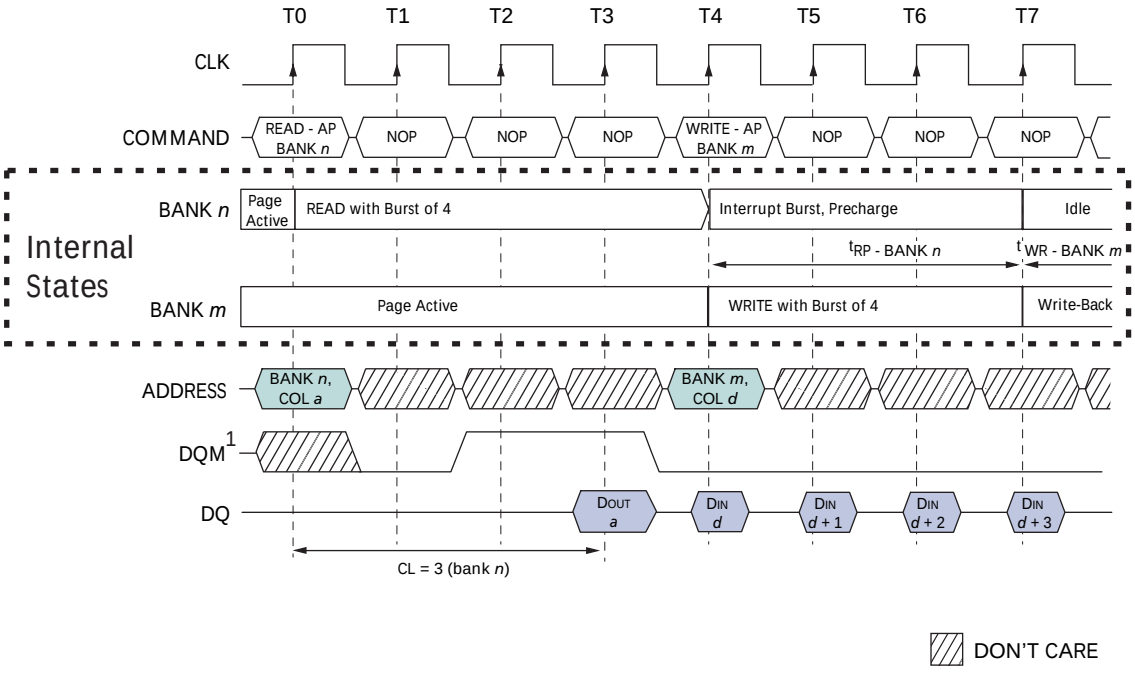

Note: For this example, CL = 2, BL = 4 or greater, and DQM is LOW.

## Figure 27: READ With Auto Precharge Interrupted by a READ




Note: DQM is LOW.

## Figure 28: READ With Auto Precharge Interrupted by a WRITE

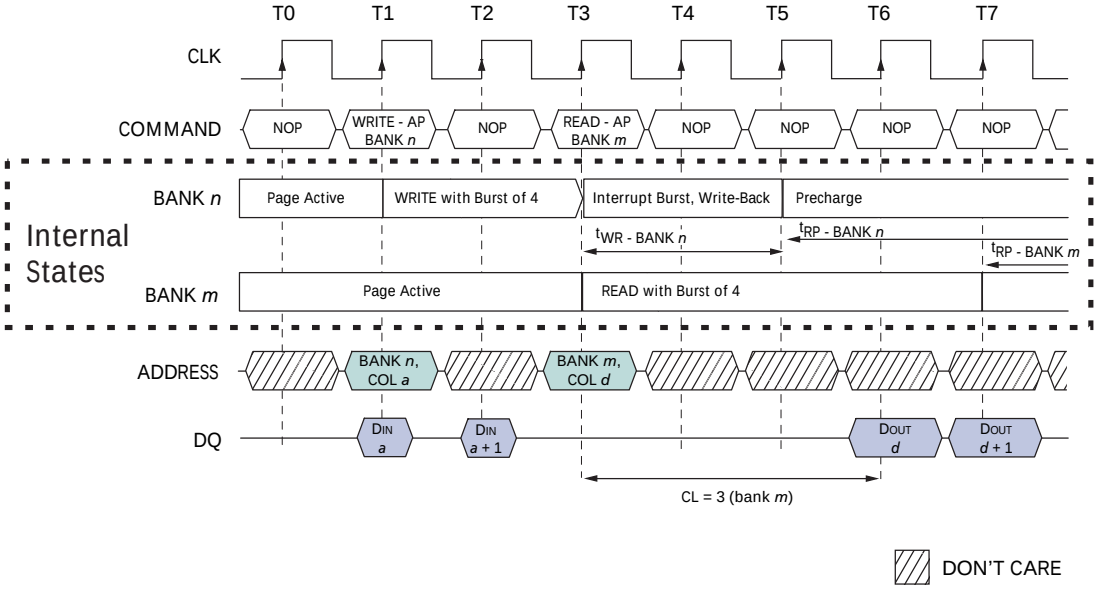



Note: DQM is HIGH at T2 to prevent DOUT-*a* +1 from contending with DIN-*d* at T4.

### WRITE with Auto Precharge

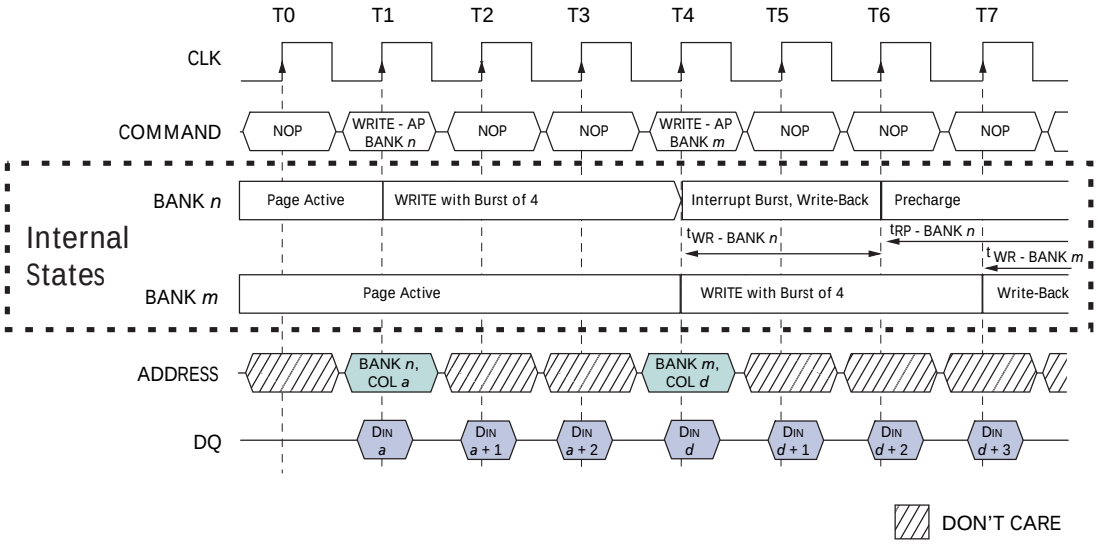
3. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CAS latency later. The precharge to bank *n* will begin after $^{t}$WR is met, where $^{t}$WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 29).
4. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The precharge to bank *n* will begin after $^{t}$WR is met, where $^{t}$WR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (Figure 30).

## Figure 29: WRITE With Auto Precharge Interrupted by a READ




Note: DQM is LOW.

## Figure 30: WRITE With Auto Precharge Interrupted by a WRITE




Note: DQM is LOW.

# Truth Tables

## Table 8: Truth Table – CKE

Notes: 1–4

| $CKE_{n-1}$ | $CKE_n$ | Current State | $COMMAND_n$ | $ACTION_n$ | Notes |
|---|---|---|---|---|---|
| L | L | Power-Down | X | Maintain Power-Down | |
| | | Self Refresh | X | Maintain Self Refresh | |
| | | Clock Suspend | X | Maintain Clock Suspend | |
| | | Deep Power-Down | X | Maintain Deep Power-Down | 8 |
| L | H | Power-Down | COMMAND INHIBIT or NOP | Exit Power-Down | 5 |
| | | Deep Power-Down | X | Exit Deep Power-Down | 8 |
| | | Self Refresh | COMMAND INHIBIT or NOP | Exit Self Refresh | 6 |
| | | Clock Suspend | X | Exit Clock Suspend | 7 |
| H | L | All Banks Idle | COMMAND INHIBIT or NOP | Power-Down Entry | |
| | | All Banks Idle | BURST TERMINATE | Deep Power-Down Entry | 8 |
| | | All Banks Idle | AUTO REFRESH | Self Refresh Entry | |
| | | Reading or Writing | VALID | Clock Suspend Entry | |
| H | H | | See Truth Table 3 | | |

Notes:
1. $CKE_n$ is the logic state of CKE at clock edge n; $CKE_{n-1}$ was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that $^tCKS$ is met).
6. Exiting self refresh at clock edge *n* will put the device in the all banks idle state once $^tXSR$ is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the $^tXSR$ period. A minimum of two NOP commands must be provided during $^tXSR$ period.
7. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n* + 1.
8. Deep Power-Down is power savings feature of this Mobile SDRAM device. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER DOWN when CKE is LOW.

## Table 9: Truth Table – Current State Bank *n*, Command To Bank *n*

Notes: 1–6; notes appear below table

| Current State | CS# | RAS# | CAS# | WE# | COMMAND (ACTION) | Notes |
|---|---|---|---|---|---|---|
| Any | H | X | X | X | COMMAND INHIBIT (NOP/Continue previous operation) | |
| | L | H | H | H | NO OPERATION (NOP/Continue previous operation) | |
| Idle | L | L | H | H | ACTIVE (Select and activate row) | |
| | L | L | L | H | AUTO REFRESH | 7 |
| | L | L | L | L | LOAD MODE REGISTER | 7 |
| | L | L | H | L | PRECHARGE | 11 |
| Row Active | L | H | L | H | READ (Select column and start READ burst) | 10 |
| | L | H | L | L | WRITE (Select column and start WRITE burst) | 10 |
| | L | L | H | L | PRECHARGE (Deactivate row in bank or banks) | 8 |
| Read (Auto Precharge Disabled) | L | H | L | H | READ (Select column and start new READ burst) | 10 |
| | L | H | L | L | WRITE (Select column and start WRITE burst) | 10 |
| | L | L | H | L | PRECHARGE (Truncate READ burst, start PRECHARGE) | 8 |
| | L | H | H | L | BURST TERMINATE | 9 |
| | L | H | H | L | DEEP POWER DOWN | 9 |
| Write (Auto Precharge Disabled) | L | H | L | H | READ (Select column and start READ burst) | 10 |
| | L | H | L | L | WRITE (Select column and start new WRITE burst) | 10 |
| | L | L | H | L | PRECHARGE (Truncate WRITE burst, start PRECHARGE) | 8 |
| | L | H | H | L | BURST TERMINATE | 9 |
| | L | H | H | L | DEEP POWER-DOWN | 9 |

Notes:
1. This table applies when $CKE_{n-1}$ was HIGH and $CKE_n$ is HIGH (see Truth Table 2) and after $^tXSR$ has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   **Idle**: The bank has been precharged, and $^tRP$ has been met.
   **Row active**: A row in the bank has been activated, and $^tRCD$ has been met. No data bursts/accesses and no register accesses are in progress.
   **Read**: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   **Write**: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
   **Precharging**: Starts with registration of a PRECHARGE command and ends when $^tRP$ is met. Once $^tRP$ is met, the bank will be in the idle state.
   **Row activating**: Starts with registration of an ACTIVE command and ends when $^tRCD$ is met. Once $^tRCD$ is met, the bank will be in the row active state
   **Read w/auto precharge enabled**: Starts with registration of a READ command with auto precharge enabled and ends when $^tRP$ has been met. Once $^tRP$ is met, the bank will be in the idle state.
   **Write w/auto precharge enabled**: Starts with registration of a WRITE command with auto precharge enabled and ends when $^tRP$ has been met. Once $^tRP$ is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when $^{t}$RC is met. Once $^{t}$RC is met, the SDRAM will be in the all banks idle state.
   Accessing mode register: Starts with registration of a LOAD MODE REGISTER command and ends when $^{t}$MRD has been met. Once $^{t}$MRD is met, the SDRAM will be in the all banks idle state.
   Precharging all: Starts with registration of a PRECHARGE ALL command and ends when $^{t}$RP is met. Once $^{t}$RP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER DOWN when CKE is LOW.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

## Table 10: Truth Table – Current State Bank *n*, Command To Bank *m*

Notes: 1–6; notes appear below and on next page

| Current State | CS# | RAS# | CAS# | WE# | COMMAND (ACTION) | Notes |
|---|---|---|---|---|---|---|
| Any | H | X | X | X | COMMAND INHIBIT (NOP/Continue previous operation) | |
| | L | H | H | H | NO OPERATION (NOP/Continue previous operation) | |
| Idle | X | X | X | X | Any Command Otherwise Allowed to Bank m | |
| Row Activating, Active, or Precharging | L | L | H | H | ACTIVE (Select and activate row) | |
| | L | H | L | H | READ (Select column and start READ burst) | 7 |
| | L | H | L | L | WRITE (Select column and start WRITE burst) | 7 |
| | L | L | H | L | PRECHARGE | |
| Read (Auto Precharge Disabled) | L | L | H | H | ACTIVE (Select and activate row) | |
| | L | H | L | H | READ (Select column and start new READ burst) | 7, 10 |
| | L | H | L | L | WRITE (Select column and start WRITE burst) | 7, 11 |
| | L | L | H | L | PRECHARGE | 9 |
| Write (Auto Precharge Disabled) | L | L | H | H | ACTIVE (Select and activate row) | |
| | L | H | L | H | READ (Select column and start READ burst) | 7, 12 |
| | L | H | L | L | WRITE (Select column and start new WRITE burst) | 7, 13 |
| | L | L | H | L | PRECHARGE | 9 |
| Read (With Auto Precharge) | L | L | H | H | ACTIVE (Select and activate row) | |
| | L | H | L | H | READ (Select column and start new READ burst) | 7, 8, 14 |
| | L | H | L | L | WRITE (Select column and start WRITE burst) | 7,8, 15 |
| | L | L | H | L | PRECHARGE | 9 |
| Write (With Auto Precharge) | L | L | H | H | ACTIVE (Select and activate row) | |
| | L | H | L | H | READ (Select column and start READ burst) | 7,8, 16 |
| | L | H | L | L | WRITE (Select column and start new WRITE burst) | 7,8, 17 |
| | L | L | H | L | PRECHARGE | 9 |

Notes:
1. This table applies when $CKE_{n-1}$ was HIGH and $CKE_n$ is HIGH (see Truth Table 2) and after $^tXSR$ has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   **Idle**: The bank has been precharged, and $^tRP$ has been met.
   **Row Active**: A row in the bank has been activated, and $^tRCD$ has been met. No data bursts/accesses and no register accesses are in progress.
   **Read**: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   **Write**: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   **Read w/Auto Precharge Enabled**: Starts with registration of a READ command with auto precharge enabled, and ends when $^tRP$ has been met. Once $^tRP$ is met, the bank will be in the idle state.
   **Write w/Auto Precharge Enabled**: Starts with registration of a WRITE command with auto precharge enabled, and ends when $^tRP$ has been met. Once $^tRP$ is met, the bank will be in the idle state.
4. AUTO REFRESH, SELF REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.

7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. CONCURRENT AUTO PRECHARGE: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m* burst.
9. Burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency later (Figure 10 consecutive read bursts).
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m will interrupt the READ on bank *n* when registered (Figures 12 and 13). DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 20), with the data-out appearing CAS latency later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank will interrupt the WRITE on bank *n* when registered (Figure 18). The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered.
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered.
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CAS latency later. The PRECHARGE to bank *n* will begin after $^{t}$WR is met, where $^{t}$WR begins when the READ to bank *m* is registered. The last valid WRITE bank *n* will be data-in registered one clock prior to the READ to bank *m*.
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after $^{t}$WR is met, where $^{t}$WR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock to the WRITE to bank *m*.

# Electrical Specifications

## Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Table 11: Absolute Maximum Ratings

| Voltage/Temperature | MIN | MAX | Units |
|---|---|---|---|
| Voltage on $V_{DD}$/$V_{DD}$Q Supply | | | |
| Relative to $V_{SS}$ (3.3V) | -1 | +4.6 | V |
| Relative to $V_{SS}$ (2.5V) | -0.5 | +3.6 | V |
| Relative to $V_{SS}$ (1.8V) | -0.35 | +2.8 | V |
| Voltage on Inputs, NC or I/O Balls | | | |
| Relative to $V_{SS}$ (3.3V) | -1 | +4.6 | V |
| Relative to $V_{SS}$ (2.5V) | -0.5 | +3.6 | V |
| Relative to $V_{SS}$ (1.8V) | -0.35 | +2.8 | V |
| Operating Temperature | | | |
| $T_A$ (Commercial) | 0° | +70° | C |
| $T_A$ (Industrial) | -40° | +85° | C |
| Storage Temperature | | | |
| Plastic | -55° | +150° | C |

### Table 12: DC Electrical Characteristics and Operating Conditions (LC version)

Notes: 1, 5, 6; notes appear on page 54; $V_{DD}$ = +3.3 ±0.3V, $V_{DD}$Q = +3.3V ±0.3V

| Parameter/Condition | Symbol | MIN | MAX | Units | Notes |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 3 | 3.6 | V | |
| I/O Supply Voltage | $V_{DD}$Q | 3 | 3.6 | V | |
| Input High Voltage: Logic 1; All input | $V_{IH}$ | 0.8 x $V_{DD}$Q | $V_{DD}$Q + 0.3 | V | 22 |
| Input Low Voltage: Logic 0; All inputs | $V_{IL}$ | -0.3 | 0.3 | V | 22 |
| Output High Voltage: All inputs: Iout = -4mA | $V_{OH}$ | $V_{DD}$Q - 0.2 | - | V | |
| Output Low Voltage: All inputs: Iout = 4mA | $V_{OL}$ | - | 0.2 | V | |
| Input Leakage Current:<br>Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$ (All other balls not under test = 0V) | $I_I$ | -5 | 5 | µA | |
| Output Leakage Current: DQs are disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DD}$Q | $I_{OZ}$ | -5 | 5 | µA | |

## Table 13: DC Electrical Characteristics and Operating Conditions (V version)

Notes: 1, 5, 6; notes appear on page 54; $V_{DD}$ = +2.5 ±0.2V, $V_{DDQ}$ = +2.5V ±0.2V

| Parameter/Condition | Symbol | MIN | MAX | Units | Notes |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.3 | 2.7 | V | |
| I/O Supply Voltage | $V_{DDQ}$ | 2.3 | 2.7 | V | |
| Input High Voltage: Logic 1; All inputs | $V_{IH}$ | 0.8 x $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V | 22 |
| Input Low Voltage: Logic 0; All inputs | $V_{IL}$ | -0.3 | 0.3 | V | 22 |
| Output High Voltage: All inputs: $I_{OUT}$ = -4mA | $V_{OH}$ | 0.9 x $V_{DDQ}$ | - | V | |
| Output Low Voltage: All inputs: $I_{OUT}$ = 4mA | $V_{OL}$ | - | 0.2 | V | |
| Input Leakage Current:<br>Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$ (All other balls not under test = 0V) | $I_I$ | -1.0 | 1.0 | µA | |
| Output Leakage Current: DQs are disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DDQ}$ | $I_{OZ}$ | -1.5 | 1.5 | µA | |

## Table 14: DC Electrical Characteristics and Operating Conditions (H version)

Notes: 1, 5, 6; notes appear on page 54; $V_{DD}$ = +1.8 ±0.1V, $V_{DDQ}$ = +1.8V ±0.1V

| Parameter/Condition | Symbol | MIN | MAX | Units | Notes |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 1.7 | 1.9 | V | |
| I/O Supply Voltage | $V_{DDQ}$ | 1.7 | 1.9 | V | |
| Input High Voltage: Logic 1; All inputs | $V_{IH}$ | 0.8 x $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V | 22 |
| Input Low Voltage: Logic 0; All inputs | $V_{IL}$ | -0.3 | +0.3 | V | 22 |
| Output High Voltage: All inputs: Iout = -4mA | $V_{OH}$ | 0.9 x $V_{DDQ}$ | – | V | |
| Output Low Voltage: All inputs: Iout = 4mA | $V_{OL}$ | – | 0.2 | V | |
| Input Leakage Current:<br>Any input 0V ≤ VIN ≤ $V_{DD}$ (All other balls not under test = 0V) | $I_I$ | -1.0 | 1.0 | µA | |
| Output Leakage Current: DQs are disabled; 0V ≤ VOUT ≤ $V_{DDQ}$ | $I_{OZ}$ | -1.5 | 1.5 | µA | |

## Table 15: Electrical Characteristics and Recommended AC Operating Conditions

Notes: 5, 6, 8, 9, 11; notes appear on page 54

| AC Characteristics | | | -75 | | -8 | | -10 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **Units** | **Notes** |
| Access time from CLK (pos. edge) | CL = 3 | $^{t}$AC (3) | | 6 | | 7 | | 7 | ns | 9 |
| | CL = 2 | $^{t}$AC (2) | | 7 | | 8 | | 8 | ns | 9 |
| | CL = 1 | $^{t}$AC (1) | - | - | | 19 | | 22 | ns | 9 |
| Address hold time | | $^{t}$AH | 1 | | 1 | | 1 | | ns | |
| Address setup time | | $^{t}$AS | 1.5 | | 2.5 | | 2.5 | | ns | |
| CLK high-level width | | $^{t}$CH | 3 | | 3 | | 3 | | ns | |
| CLK low-level width | | $^{t}$CL | 3 | | 3 | | 3 | | ns | |
| Clock cycle time | CL = 3 | $^{t}$CK (3) | 7.5 | | 8 | 100 | 10 | 100 | ns | 23 |
| | CL = 2 | $^{t}$CK (2) | 9 | | 9 | 100 | 12 | 100 | ns | 23, 31 |
| | CL = 1 | $^{t}$CK (1) | - | | 20 | 100 | 25 | 100 | ns | |
| CKE hold time | | $^{t}$CKH | 1 | | 1 | | 1 | | ns | |
| CKE setup time | | $^{t}$CKS | 2.5 | | 2.5 | | 2.5 | | ns | |
| CS#, RAS#, CAS#, WE#, DQM hold time | | $^{t}$CMH | 1 | | 1 | | 1 | | ns | |
| CS#, RAS#, CAS#, WE#, DQM setup time | | $^{t}$CMS | 1.5 | | 2.5 | | 2.5 | | ns | |
| Data-in hold time | | $^{t}$DH | 1 | | 1 | | 1 | | ns | |
| Data-in setup time | | $^{t}$DS | 1.5 | | 2.5 | | 2.5 | | ns | |
| Data-out high-z time | CL = 3 | $^{t}$HZ (3) | | 6 | | 7 | | 7 | ns | 10 |
| | CL = 2 | $^{t}$HZ (2) | | 7 | | 8 | | 8 | ns | 10 |
| | CL = 1 | $^{t}$HZ (1) | | - | | 19 | | 22 | ns | 10 |
| Data-out low-z time | | $^{t}$LZ | 1 | | 1 | | 1 | | ns | |
| Data-out hold time (load) | | $^{t}$OH | 2.5 | | 2.5 | | 2.5 | | ns | |
| Data-out hold time (no load) | | $^{t}$OHN | 1.8 | | 1.8 | | 1.8 | | ns | 27 |
| ACTIVE to PRECHARGE command | | $^{t}$RAS | 44 | 120000 | 48 | 120000 | 50 | 120000 | ns | |
| ACTIVE to ACTIVE command period | | $^{t}$RC | 67.5 | | 72 | | 90 | | ns | |
| ACTIVE to READ or WRITE delay | | $^{t}$RCD | 19 | | 20 | | 20 | | ns | |
| Refresh period (4,096 rows) | | $^{t}$REF | | 64 | | 64 | | 64 | ms | |
| AUTO REFRESH period | | $^{t}$RFC | 80 | | 80 | | 100 | | ns | |
| PRECHARGE command period | | $^{t}$RP | 19 | | 19 | | 20 | | ns | |
| ACTIVE bank *a* to ACTIVE bank *b* command | | $^{t}$RRD | 15 | | 16 | | 20 | | ns | |
| Transition time | | $^{t}$T | 0.3 | 1.2 | 0.5 | 1.2 | 0.5 | 1.2 | ns | 7 |
| WRITE recovery time | | $^{t}$WR (a) | 1 CLK + 7.5ns | | 1 CLK +7ns | | 1 CLK +5ns | | – | 24 |
| | | $^{t}$WR (m) | 15 | | 15 | | 15 | | ns | 25 |
| Exit SELF REFRESH to ACTIVE command | | $^{t}$XSR | 67 | | 80 | | 100 | | ns | 20 |

## Table 16: AC Functional Characteristics

Notes: 5, 6, 7, 8, 9, 11; notes appear on page 54

| Parameter | | Symbol | -75 | -8 | -10 | Units | Notes |
|---|---|---|---|---|---|---|---|
| READ/WRITE command to READ/WRITE command | | tCCD | 1 | 1 | 1 | tCK | 17 |
| CKE to clock disable or power-down entry mode | | tCKED | 1 | 1 | 1 | tCK | 14 |
| CKE to clock enable or power-down exit setup mode | | tPED | 1 | 1 | 1 | tCK | 14 |
| DQM to input data delay | | tDQD | 0 | 0 | 0 | tCK | 17 |
| DQM to data mask during WRITEs | | tDQM | 0 | 0 | 0 | tCK | 17 |
| DQM to data high-z during READs | | tDQZ | 2 | 2 | 2 | tCK | 17 |
| WRITE command to input data delay | | tDWD | 0 | 0 | 0 | tCK | 17 |
| Data-in to ACTIVE command | | tDAL | 5 | 5 | 5 | tCK | 15, 21 |
| Data-in to PRECHARGE command | | tDPL | 2 | 2 | 2 | tCK | 16, 21 |
| Last data-in to burst STOP command | | tBDL | 1 | 1 | 1 | tCK | 17 |
| Last data-in to new READ/WRITE command | | tCDL | 1 | 1 | 1 | tCK | 17 |
| Last data-in to PRECHARGE command | | tRDL | 2 | 2 | 2 | tCK | 16, 21 |
| LOAD MODE REGISTER command to ACTIVE or REFRESH command | | tMRD | 2 | 2 | 2 | tCK | 26 |
| Data-out to high-z from PRECHARGE command | CL = 3 | tROH(3) | 3 | 3 | 3 | tCK | 17 |
| | CL = 2 | tROH(2) | 2 | 2 | 2 | tCK | 17 |
| | CL = 1 | tROH(1) | - | 1 | 1 | tCK | 17 |

## Table 17: IDD Specifications and Conditions (LC version)

Notes: 1, 5, 6, 11, 13; notes appear on page 54; VDD = +3.3V ±0.3V, VDDQ = +3.3V ±0.3V

| | | | MAX | | | | |
|---|---|---|---|---|---|---|---|
| Parameter/Condition | | Symbol | -75 | -8 | -10 | Units | Notes |
| Operating current: active mode; Burst = 2; READ or WRITE; tRC = tRC (MIN) | | IDD1 | 170 | 170 | 145 | mA | 3, 18, 19, 28 |
| Standby current: power-down mode; All banks idle; CKE = LOW | | IDD2P | 400 | 400 | 400 | µA | 28 |
| Standby current: power-down mode; All banks idle; CKE = HIGH | | IDD2N | 30 | 30 | 30 | mA | 28 |
| Standby current: active mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress | | IDD3N | 40 | 40 | 40 | mA | 3, 12, 19, 28 |
| Standby current: active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress | | IDD3P | 30 | 30 | 30 | mA | 3, 12, 19, 28 |
| Operating current: burst mode; Continuous burst; READ or WRITE; All banks active, half DQs toggling every cycle | | IDD4 | 125 | 125 | 100 | mA | 3, 18, 19, 28 |
| Auto Refresh Current CKE = HIGH; CS# = HIGH | tRFC = tRFC (MIN) | IDD5 | 255 | 255 | 205 | mA | 3, 12, 18, 19, 28, 29 |
| | tRFC = 15.625µs | IDD6 | 2.5 | 2.5 | 2.5 | mA | |
| Deep power-down | | IZZ | 10 | 10 | 10 | µA | |

## Table 18: IDD Specifications and Conditions (V version)

Notes: 1, 5, 6, 11, 13; notes appear on page 54; VDD = +2.5 ±0.2V, VDDQ = +2.5 ±0.2V

| | | | MAX | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter/Condition** | | **Symbol** | **-75** | **-8** | **-10** | **Units** | **Notes** |
| Operating current: active mode; Burst = 2; READ or WRITE; tRC = tRC (MIN) | | IDD1 | 170 | 170 | 145 | mA | 3, 18, 19, 28 |
| Standby current: power-down mode; All banks idle; CKE = LOW | | IDD2P | 400 | 400 | 400 | µA | 28 |
| Standby current: power-down mode; All banks idle; CKE = HIGH | | IDD2N | 30 | 30 | 30 | mA | 28 |
| Standby current: active mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress | | IDD3N | 40 | 40 | 40 | mA | 3, 12, 19, 28 |
| Standby current: active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress | | IDD3P | 30 | 30 | 30 | mA | 3, 12, 19, 28 |
| Operating current: burst mode; continuous burst; READ or WRITE; All banks active, half DQs toggling every cycle | | IDD4 | 125 | 125 | 100 | mA | 3, 18, 19, 28 |
| Auto Refresh Current CKE = HIGH; CS# = HIGH | tRFC = tRFC (MIN) | IDD5 | 255 | 255 | 200 | mA | 3, 12, 18, 19, 28, 29 |
| | tRFC = 15.625µs | IDD6 | 2.5 | 2.5 | 2.5 | mA | |
| Deep power-down | | IZZ | 10 | 10 | 10 | µA | |

## Table 19: IDD Specifications and Conditions (H version)

Notes: 1, 5, 6, 11, 13; notes appear on page 54; VDD = 1.8 ±0.1V, VDDQ = 1.8V ±0.1V

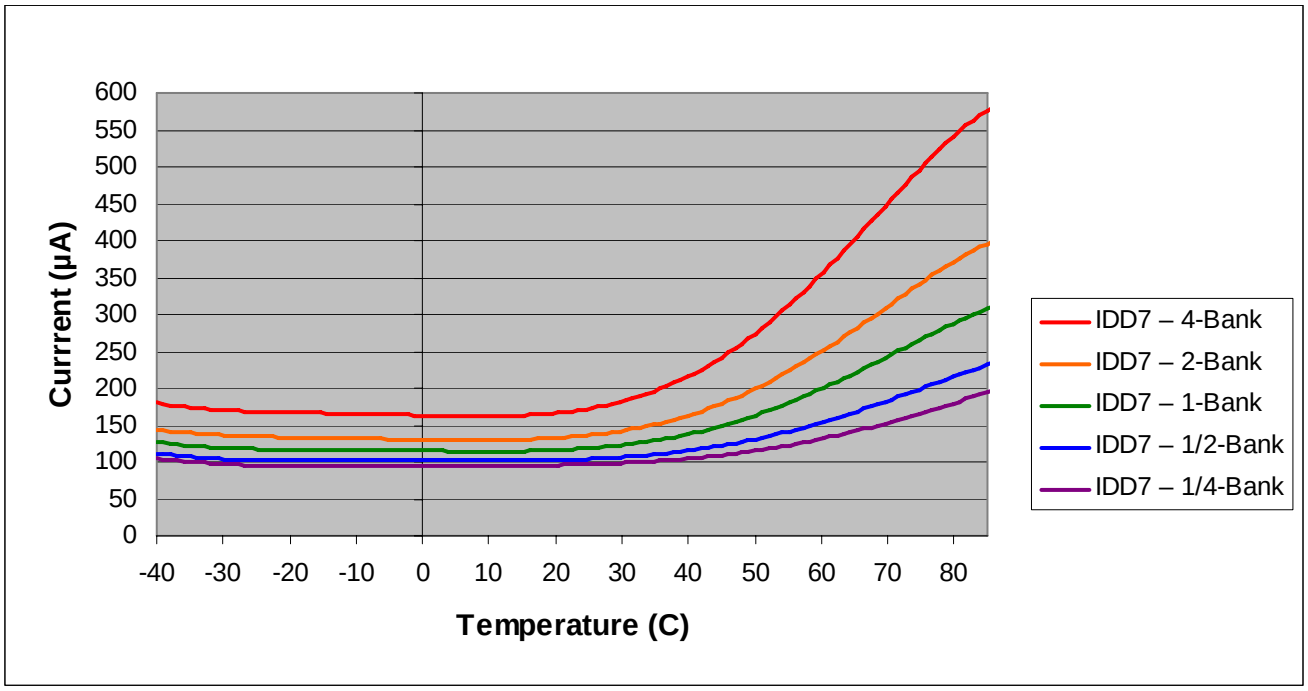
| | | | MAX | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter/Condition** | | **Symbol** | **-75** | **-8** | **-10** | **Units** | **Notes** |
| Operating current: active mode; Burst = 2; READ or WRITE; tRC = tRC (MIN) | | IDD1 | 125 | 125 | 100 | mA | 3, 18, 19, 28 |
| Standby current: power-down mode; All banks idle; CKE = LOW | | IDD2P | 300 | 300 | 300 | µA | 28 |
| Standby current: power-down mode; All banks idle; CKE = HIGH | | IDD2N | 20 | 20 | 20 | mA | 28 |
| Standby current: active mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress | | IDD3N | 30 | 30 | 30 | mA | 3, 12, 19, 28 |
| Standby current: active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress | | IDD3P | 20 | 20 | 20 | mA | 3, 12, 19, 28 |
| Operating current: burst mode; Continuous burst; READ or WRITE; All banks active, half DQs toggling every cycle | | IDD4 | 85 | 85 | 65 | mA | 3, 18, 19, 28 |
| Auto Refresh Current CKE = HIGH; CS# = HIGH | tRFC = tRFC (MIN) | IDD5 | 210 | 210 | 170 | mA | 3, 12, 18, 19, 28, 29 |
| | tRFC = 15.625µs | IDD6 | 2.5 | 2.5 | 2.5 | mA | |
| Deep power-down | | IZZ | 10 | 10 | 10 | µA | |

## Table 20: IDD7 – Self Refresh Current Options

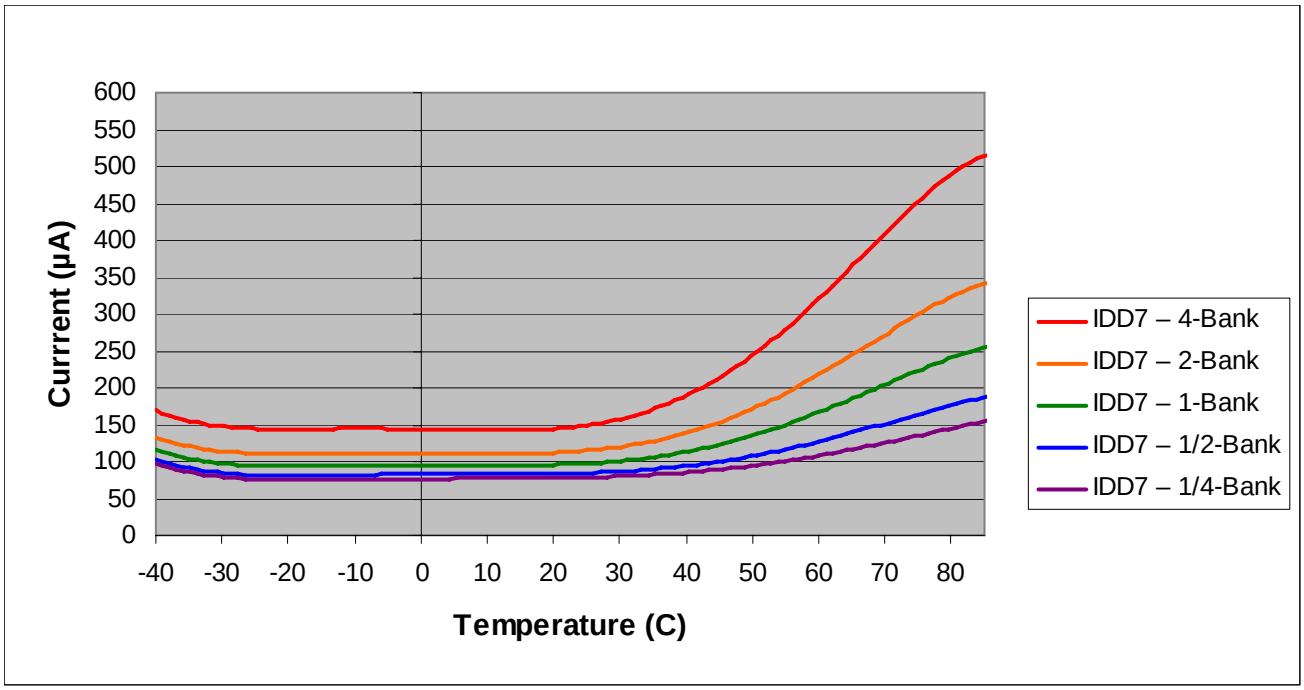
Notes: 4, 30; notes appear on page 54 and page 55

| Temperature Compensated Self Refresh Parameter/Condition | MAX Temperature | VDD = 3.3 | VDD = 2.5 | VDD = 1.8 | Units | Notes |
|---|---|---|---|---|---|---|
| Self Refresh Current: CKE = LOW – 4-bank refresh | 85ºC | 800 | 800 | 600 | µA | 4, 30 |
| | 70ºC | 647 | 647 | 480 | µA | 4, 30 |
| | 45ºC | 503 | 503 | 370 | µA | 4, 30 |
| | 15ºC | 432 | 432 | 315 | µA | 4, 30 |
| Self Refresh Current: CKE = LOW – 2-bank refresh | 85ºC | 600 | 600 | 450 | µA | 4, 30 |
| | 70ºC | 513 | 513 | 380 | µA | 4, 30 |
| | 45ºC | 437 | 437 | 320 | µA | 4, 30 |
| | 15ºC | 398 | 398 | 290 | µA | 4, 30 |
| Self Refresh Current: CKE = LOW – 1-bank refresh | 85ºC | 500 | 500 | 375 | µA | 4, 30 |
| | 70ºC | 447 | 447 | 330 | µA | 4, 30 |
| | 45ºC | 403 | 403 | 295 | µA | 4, 30 |
| | 15ºC | 382 | 382 | 278 | µA | 4, 30 |
| Self Refresh Current: CKE = LOW – Half-bank refresh | 85ºC | 450 | 450 | 338 | µA | 4, 30 |
| | 70ºC | 413 | 413 | 305 | µA | 4, 30 |
| | 45ºC | 387 | 387 | 283 | µA | 4, 30 |
| | 15ºC | 373 | 373 | 271 | µA | 4, 30 |
| Self Refresh Current: CKE = LOW – Quarter-bank refresh | 85ºC | 425 | 425 | 319 | µA | 4, 30 |
| | 70ºC | 397 | 397 | 293 | µA | 4, 30 |
| | 45ºC | 378 | 378 | 276 | µA | 4, 30 |
| | 15ºC | 369 | 369 | 268 | µA | 4, 30 |

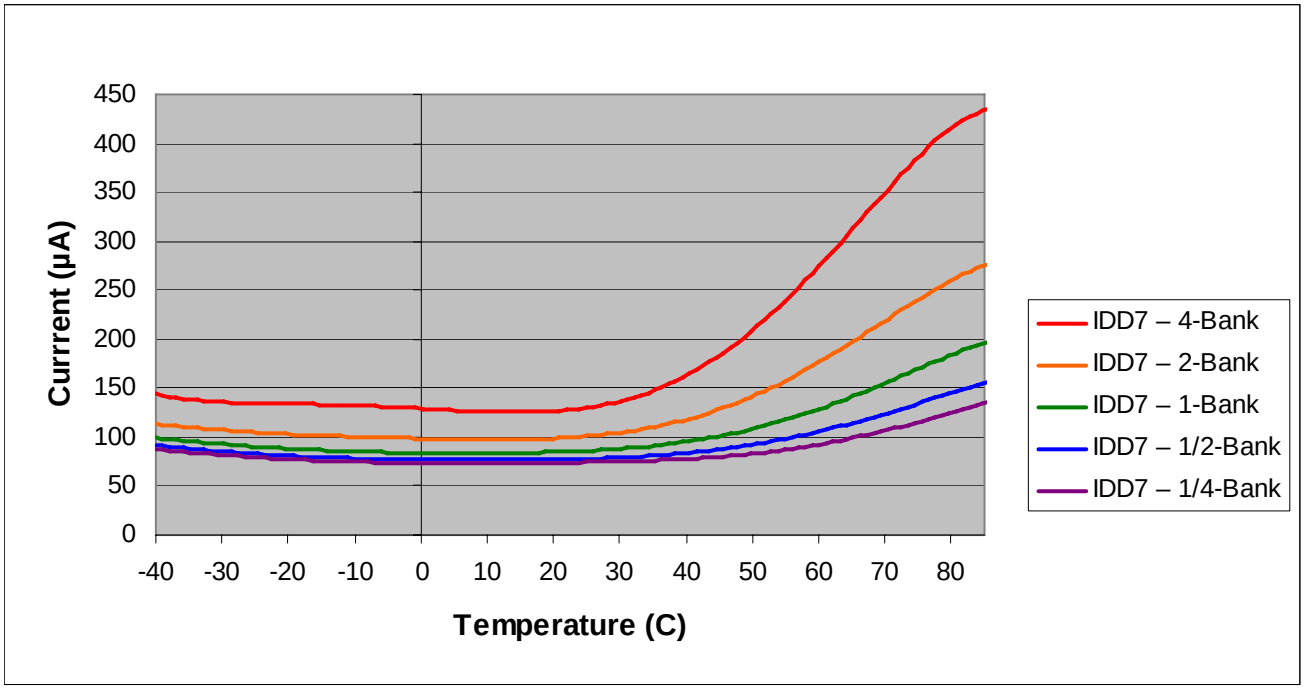
## Figure 31: Typical Self Refresh Current vs. Temperature – 3.3V Part



## Figure 32: Typical Self Refresh Current vs. Temperature – 2.5V Part




## Figure 33: Typical Self Refresh Current vs. Temperature – 1.8V Part



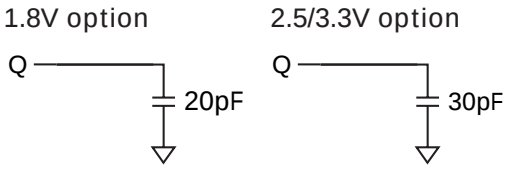
## Table 21: Capacitance

Note: 2; notes appear on page 54

| Parameter | Symbol | MIN | MAX | Units | Notes |
|---|---|---|---|---|---|
| Input Capacitance: CLK | $C_{I1}$ | 2.5 | 4.5 | pF | 2 |
| Input Capacitance: All other input-only balls | $C_{I2}$ | 2.5 | 4.5 | pF | 2 |
| Input/Output Capacitance: DQs | $C_{IO}$ | 4.0 | 6.0 | pF | 2 |

## Notes

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{DD}$, $V_{DDQ}$ = +1.8V, 2.5V or 3.3V; $T_A$ = 25°C; ball under test biased at 0.9V, 1.25V, and 1.4V respectively. f = 1 MHz.
3. $I_{DD}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-40°C ≤ $T_A$ ≤ +85°C for $T_A$ on IT parts) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ($V_{DD}$ and $V_{DDQ}$ must be powered up simultaneously. $V_{SS}$ and $V_{SSQ}$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the $^{t}$REF refresh requirement is exceeded.
7. AC characteristics assume $^{t}$T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
9. Outputs measured for 1.8V at 0.9V, 2.5V at 1.25V, or 3.3V at 1.65V with equivalent load:

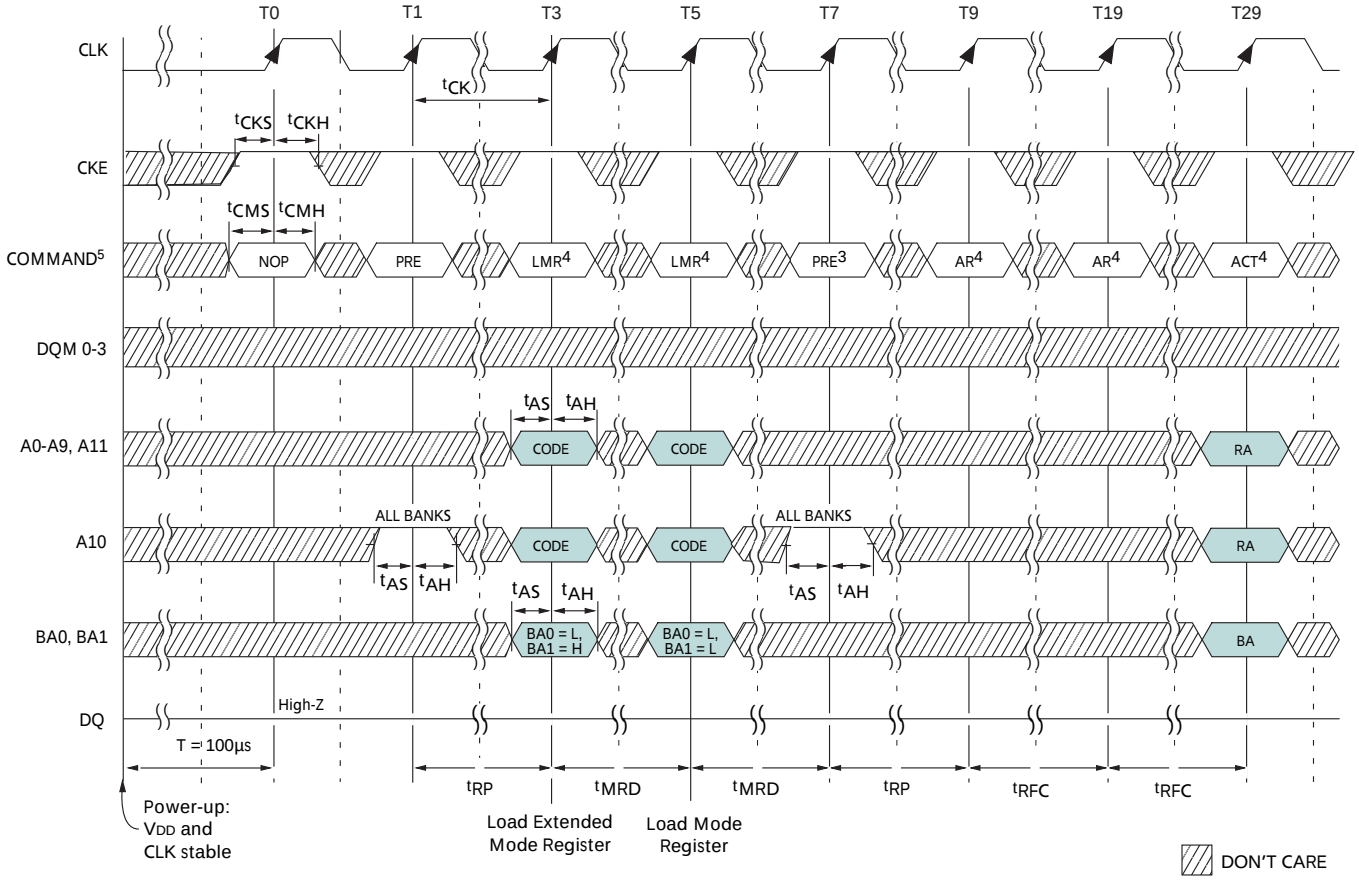



   Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.
10. $^{t}$HZ defines the time at which the output achieves the open circuit condition; it is not a reference to $V_{OH}$ or $V_{OL}$. The last valid data element will meet $^{t}$OH before going High-Z.
11. AC timing and $I_{DD}$ tests have $V_{IL}$ and $V_{IH}$, with timing referenced to $V_{IH}/2$ = crossover point. If the input transition time is longer than $^{t}$T (MAX), then the timing is referenced at $V_{IL}$ (MAX) and $V_{IH}$ (MIN) and no longer at the $V_{IH}/2$ crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid $V_{IH}$ or $V_{IL}$ levels.
13. $I_{DD}$ specifications are tested after the device is properly initialized.
14. Timing actually specified by $^{t}$CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by $^{t}$WR plus $^{t}$RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by $^{t}$WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The $I_{DD}$ current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.

20. CLK must be toggled a minimum of two times during this period.
21. Based on $^{t}$CK = 7.5ns for -75,$^{t}$CK = 8ns for -8, $^{t}$CK = 10ns for -10, and CL = 3.
22. $V_{IH}$ overshoot: $V_{IH}$ (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. $V_{IL}$ undershoot: $V_{IL}$ (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including $^{t}$WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget ($^{t}$RP) begins at 7ns for -8 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC specifies three clocks.
27. Parameter guaranteed by design.
28. For -10, CL = 3 and $^{t}$CK = 10ns.
29. CKE is HIGH during refresh command period $^{t}$RFC (MIN) else CKE is LOW. The $I_{DD}6$ limit is actually a nominal value and does not result in a fail value.
30. Values for $I_{DD}7$ for 85C are 100 percent tested. Values for 70C, 45C, and 15C are sampled only.
31. $^{t}$CK (2) MIN is 9.6 ns for -7.5 and -8 speed 1.8V product.

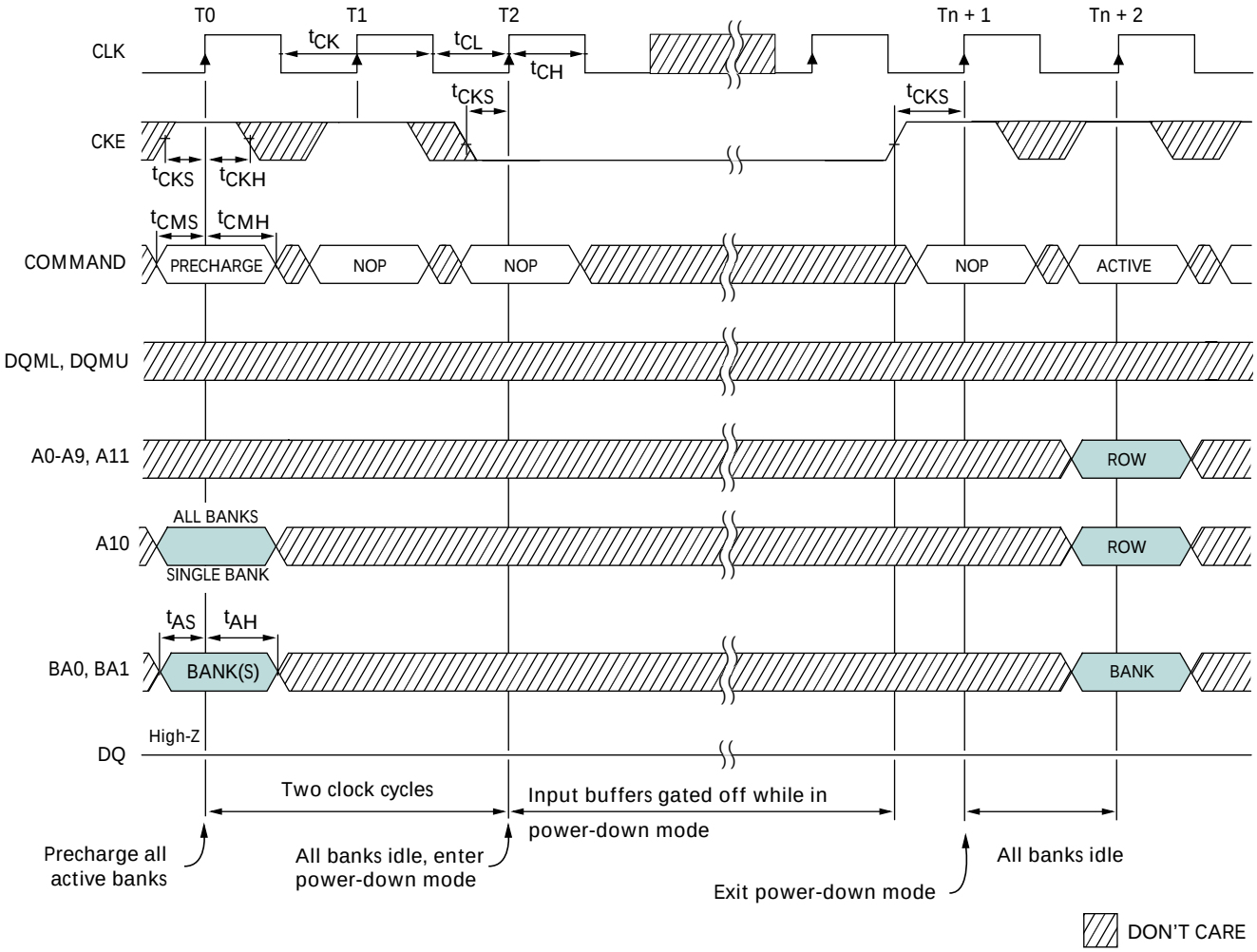
# Timing Diagrams

## Figure 34: Initialize and Load Mode Register[1,2]



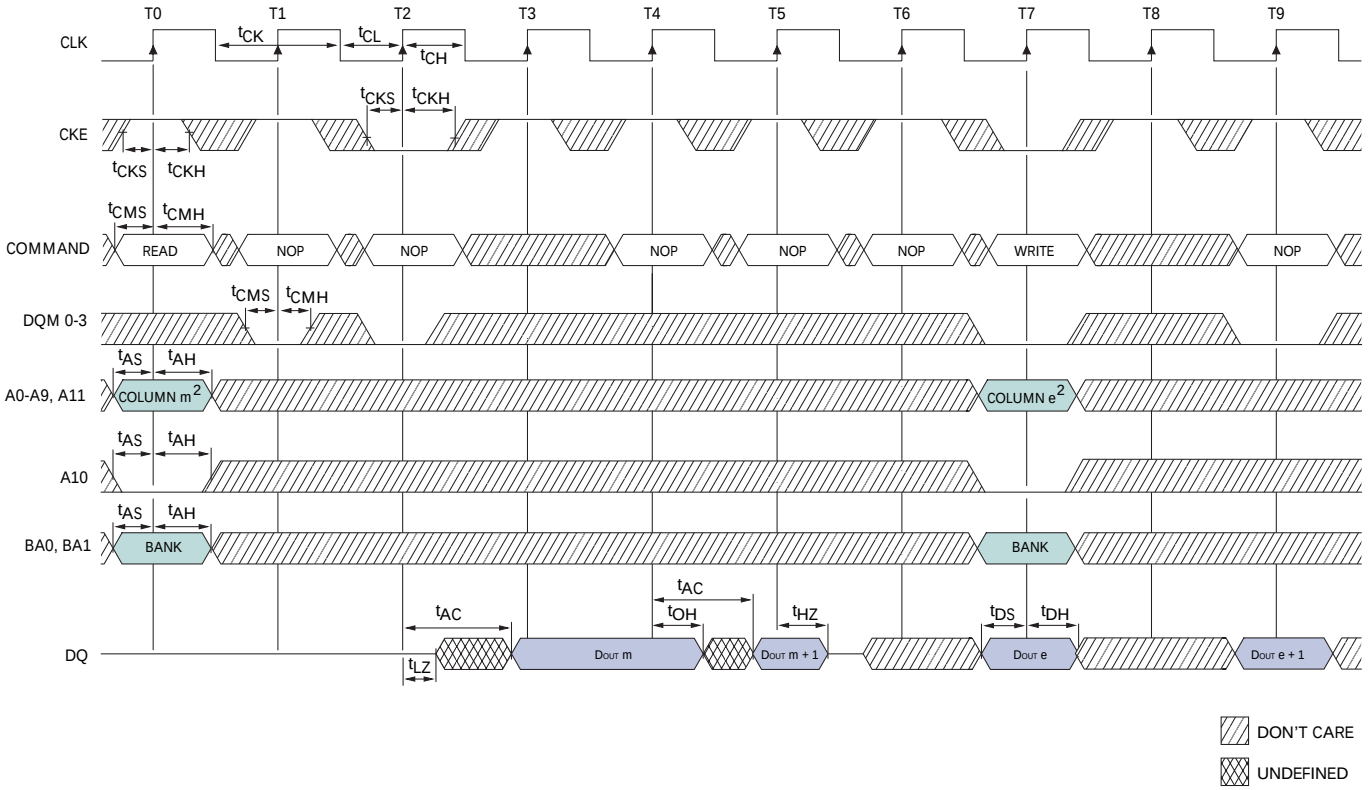

Notes: 1. The two AUTO REFRESH commands at T9 and T19 may be applied before either LOAD MODE REGISTER (LMR) command.
2. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address.
3. Optional REFRESH command.
4. The load mode register for both MR/EMR and 2 AUTO REFRESH commands can be in any order. However, all must occur prior to an ACTIVE command.
5. Device timing is -10 with 100 MHz clock.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 35: Power-Down Mode



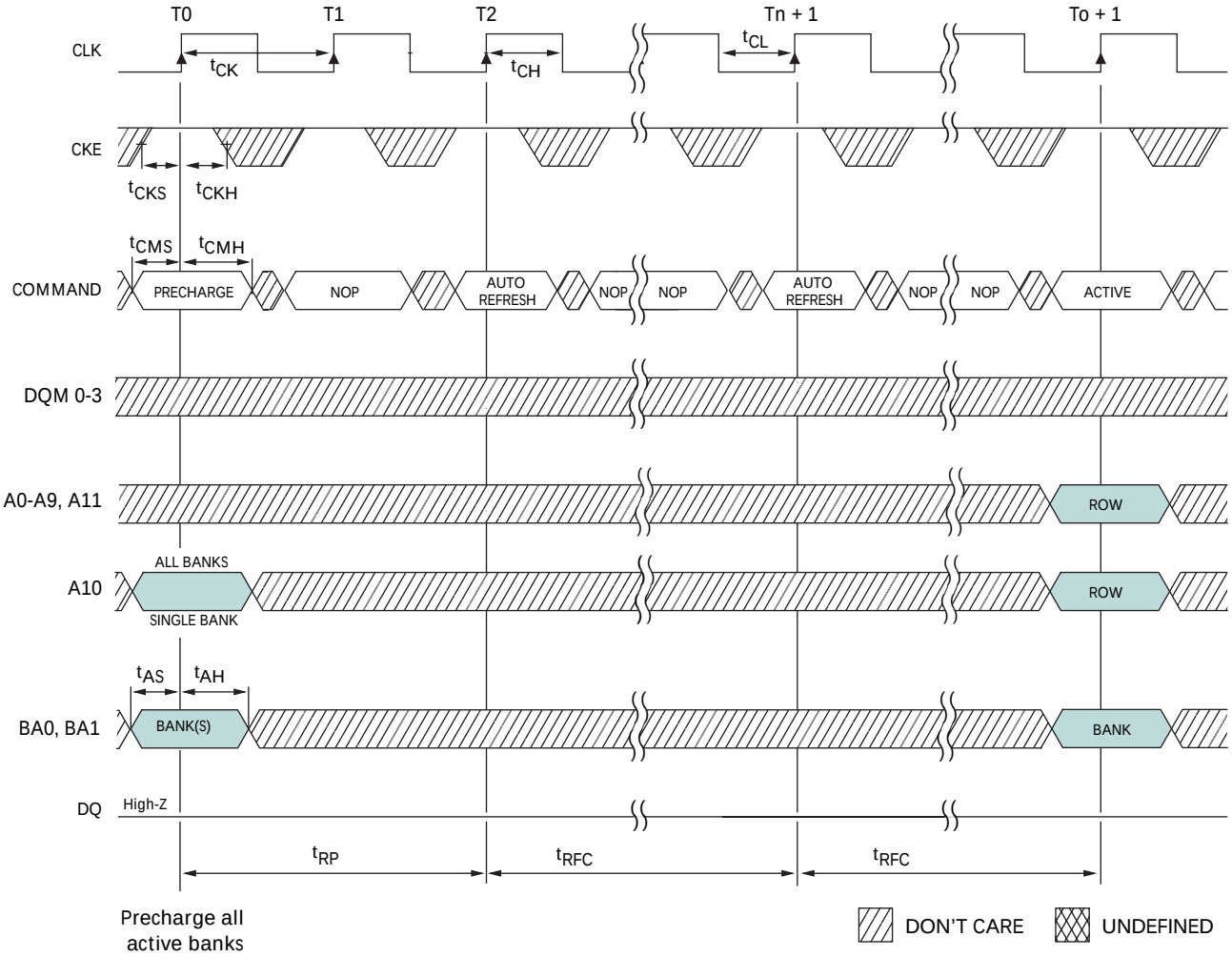

Note: Violating refresh requirements during power-down may result in a loss of data. See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 36: Clock Suspend Mode



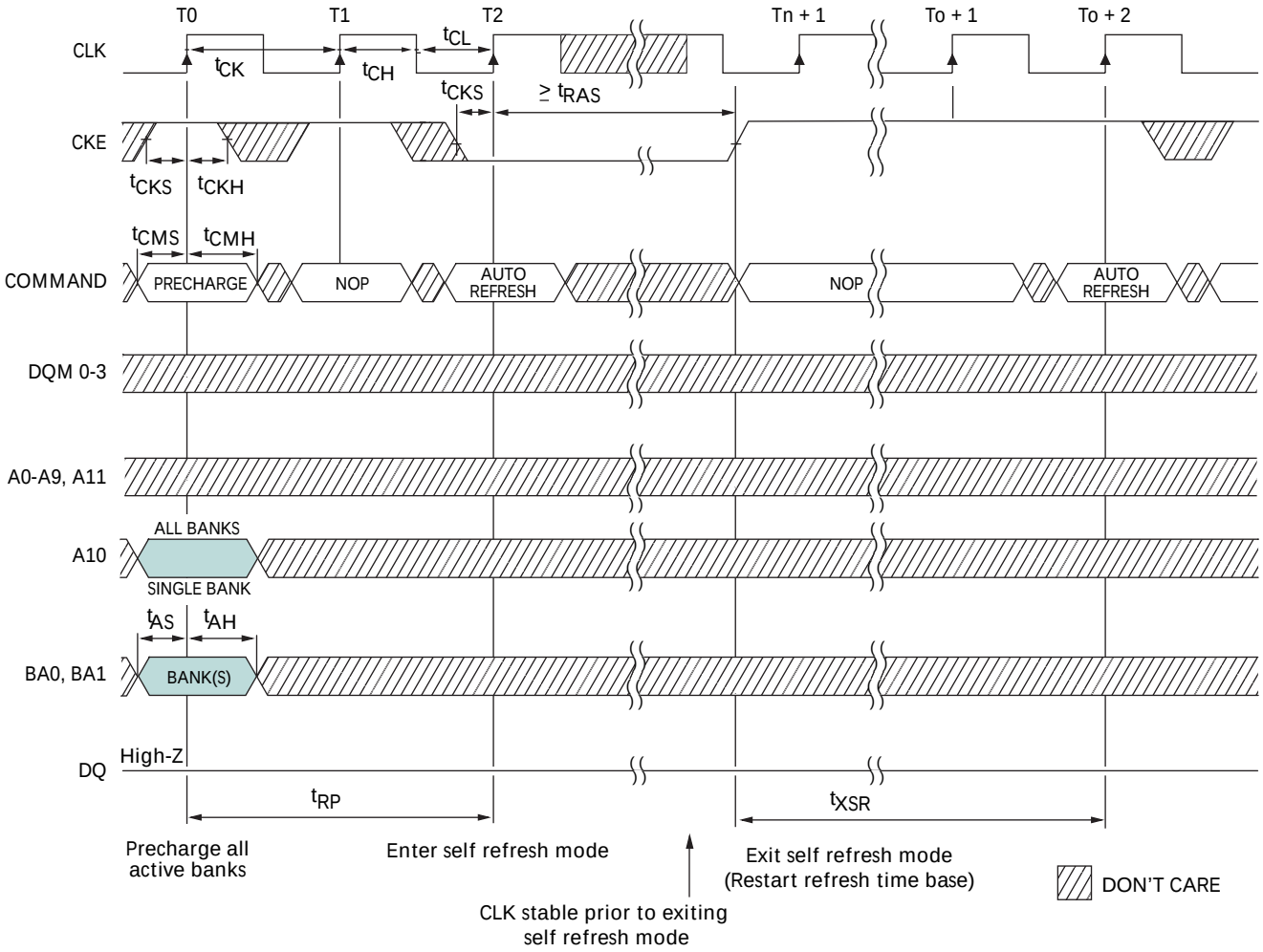

Notes: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.
2. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 37: Auto Refresh Mode



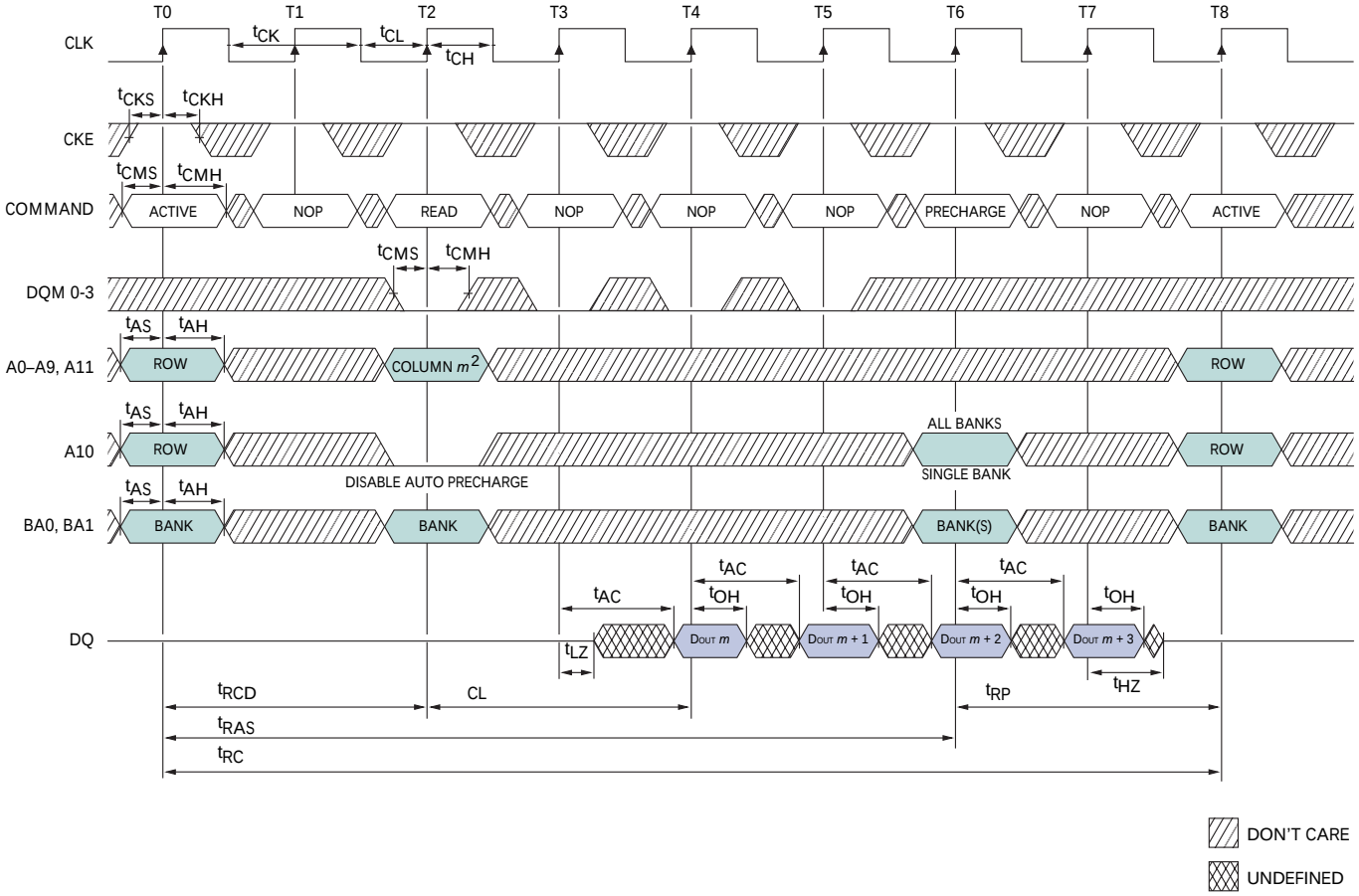

Note: Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 38: Self Refresh Mode



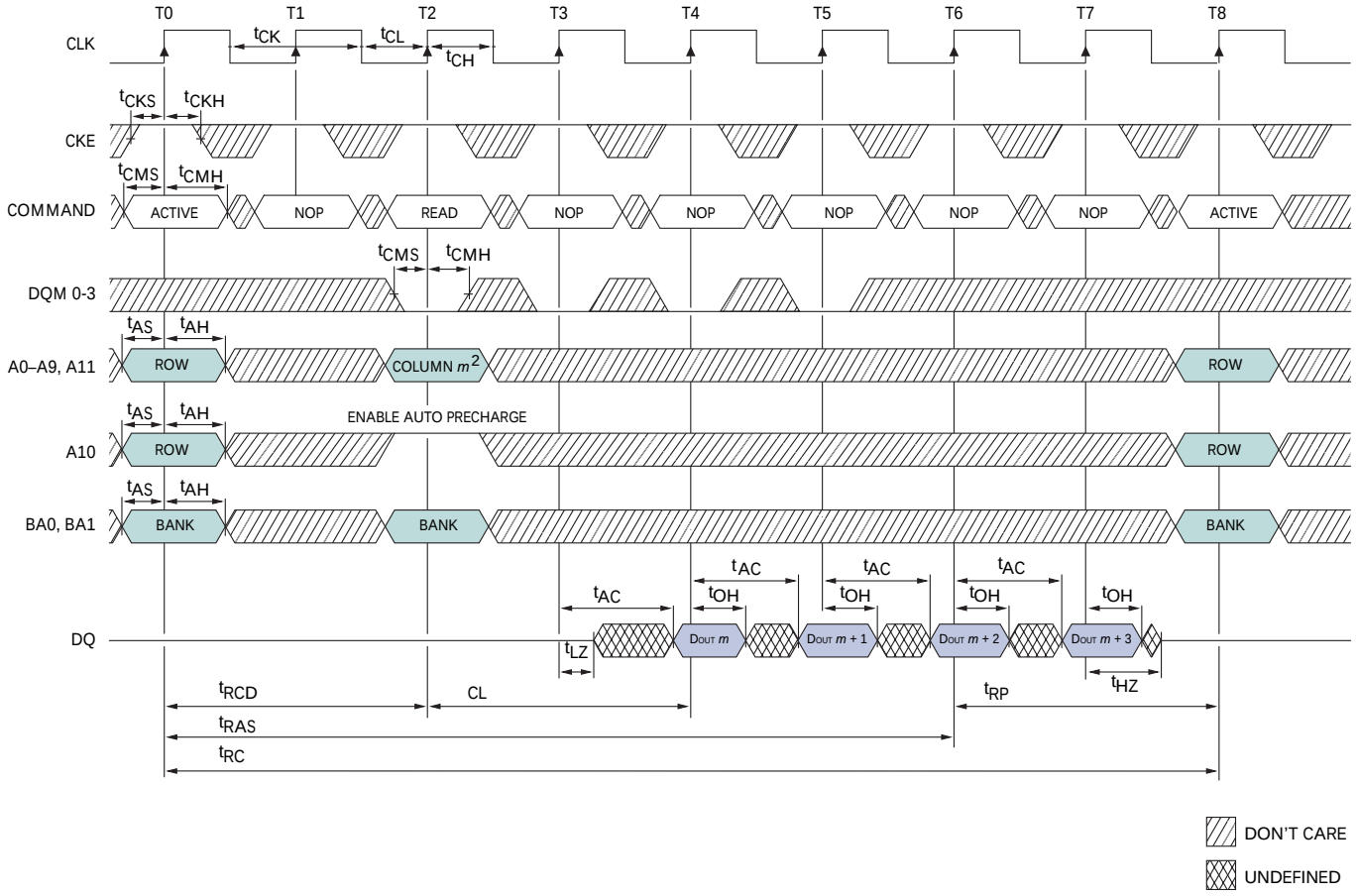

Note: Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 39: READ – Without Auto Precharge[1]



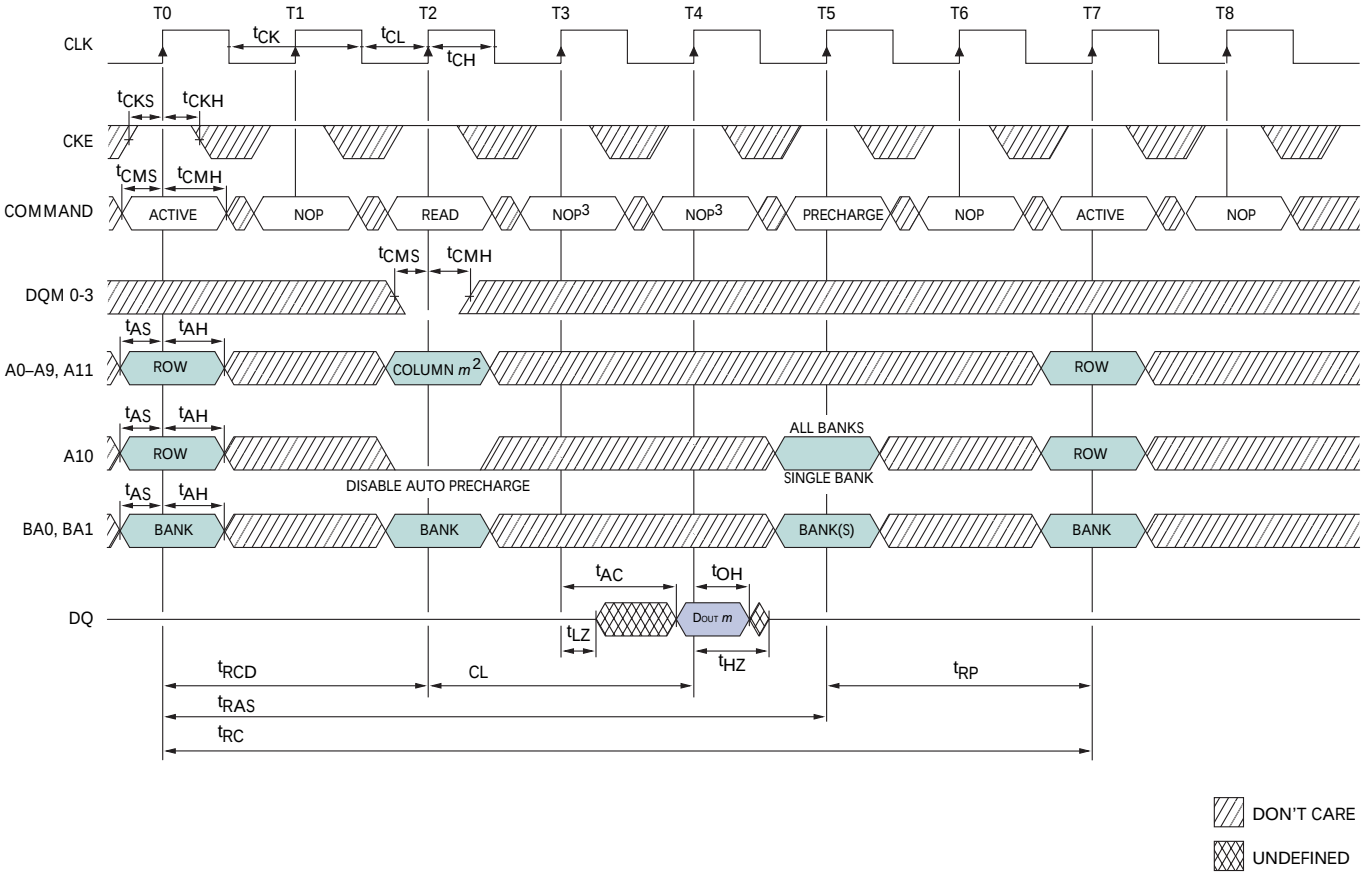

Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.
2. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 40: Read – With Auto Precharge[1]



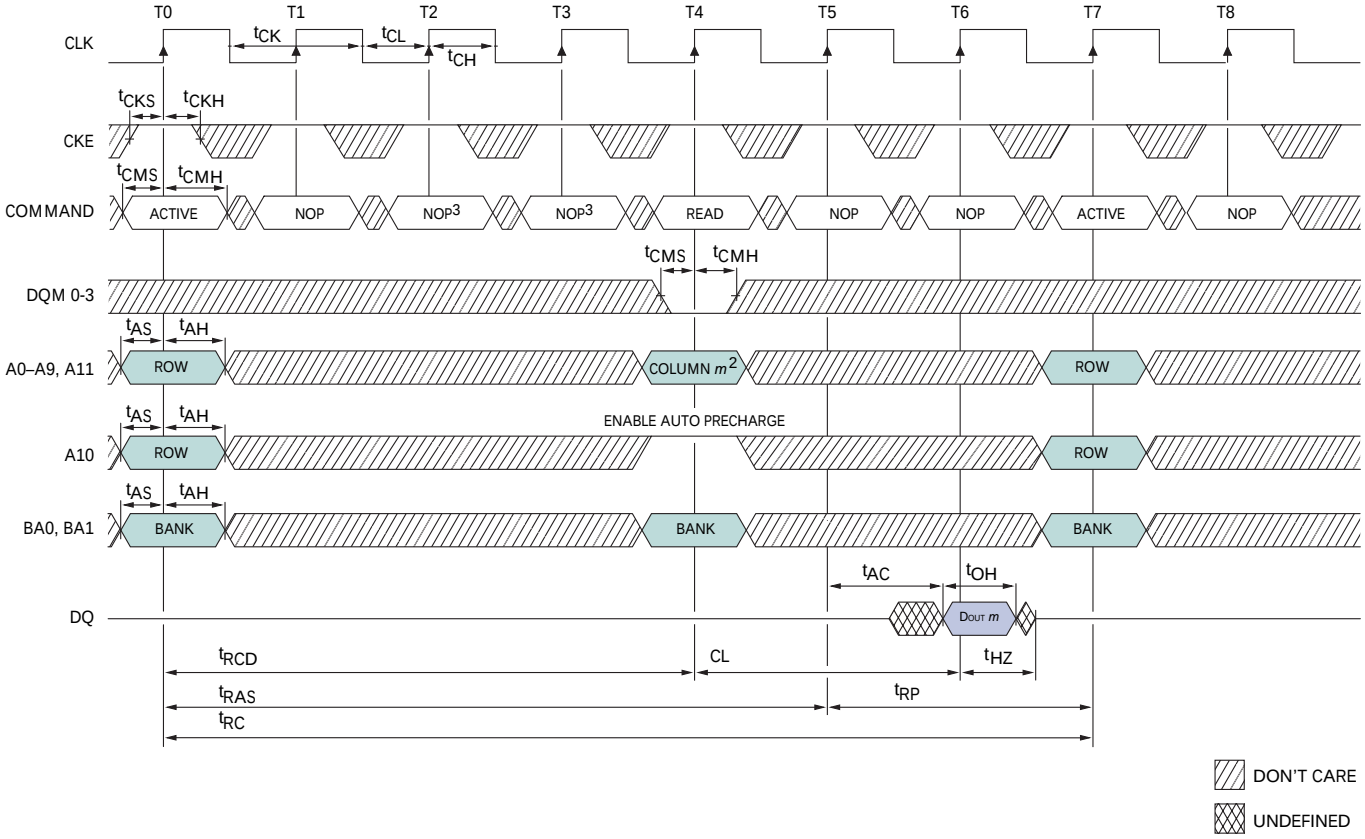

Notes: 1. For this example, BL = 4, CL = 2.
2. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 41: Single Read – Without Auto Precharge[1]



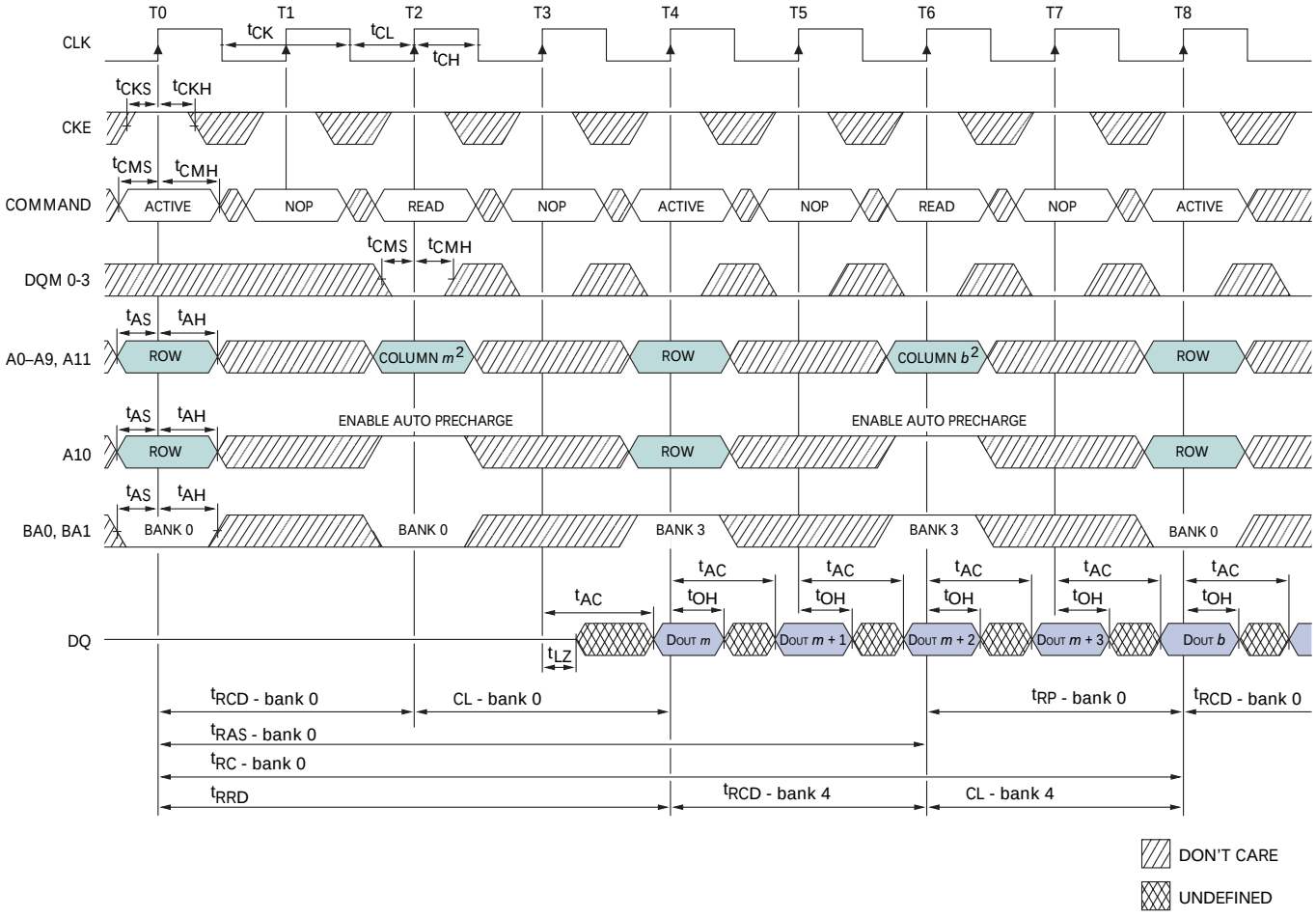

Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.
2. A9 and A11 = "Don't Care."
3. PRECHARGE command not allowed or tRAS would be violated.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 42: Single Read – With Auto Precharge[1]



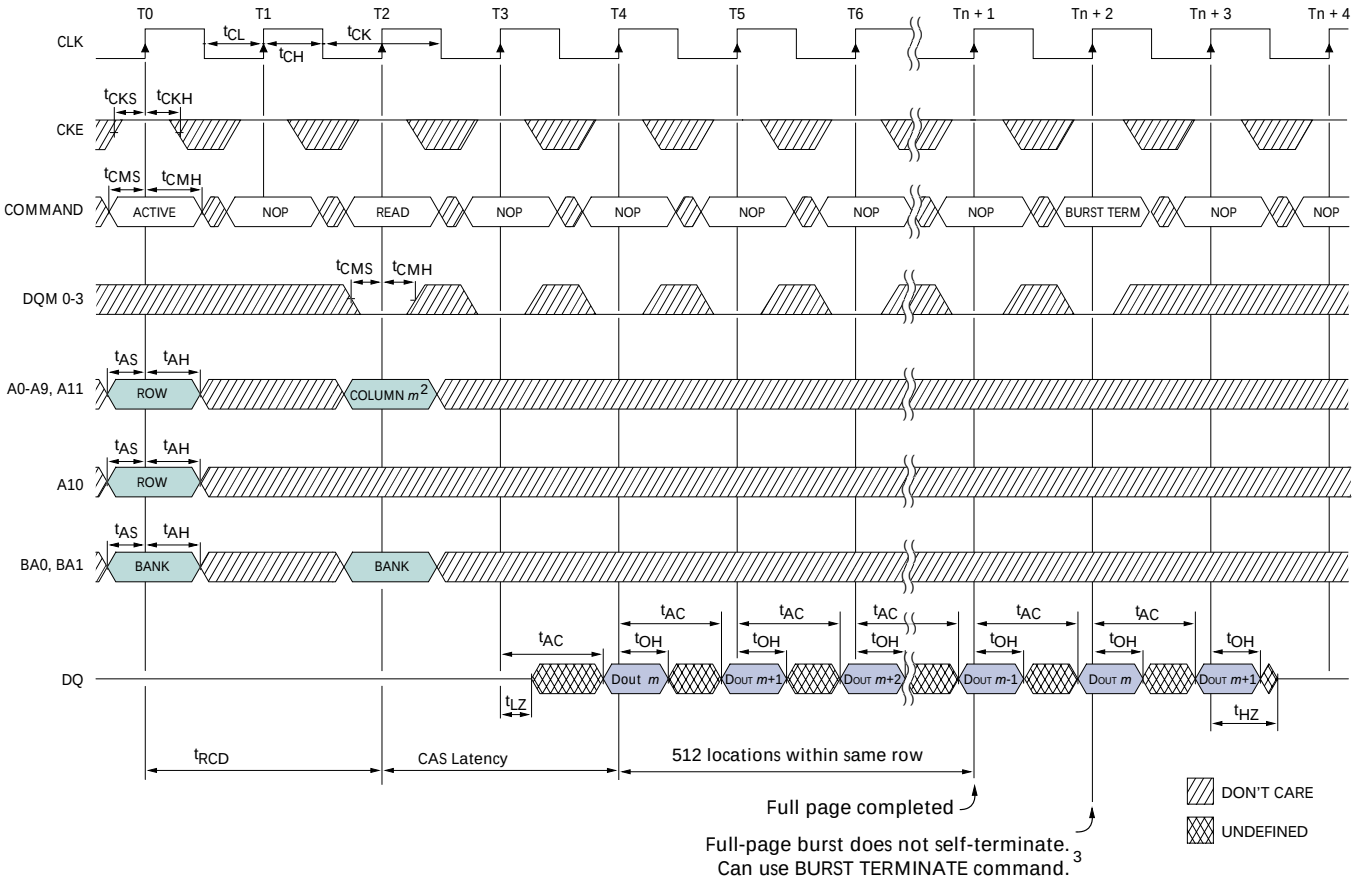

Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.
2. A9 and A11 = "Don't Care."
3. PRECHARGE command not allowed or $^{t}$RAS would be violated.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 43: Alternating Bank Read Accesses[1]



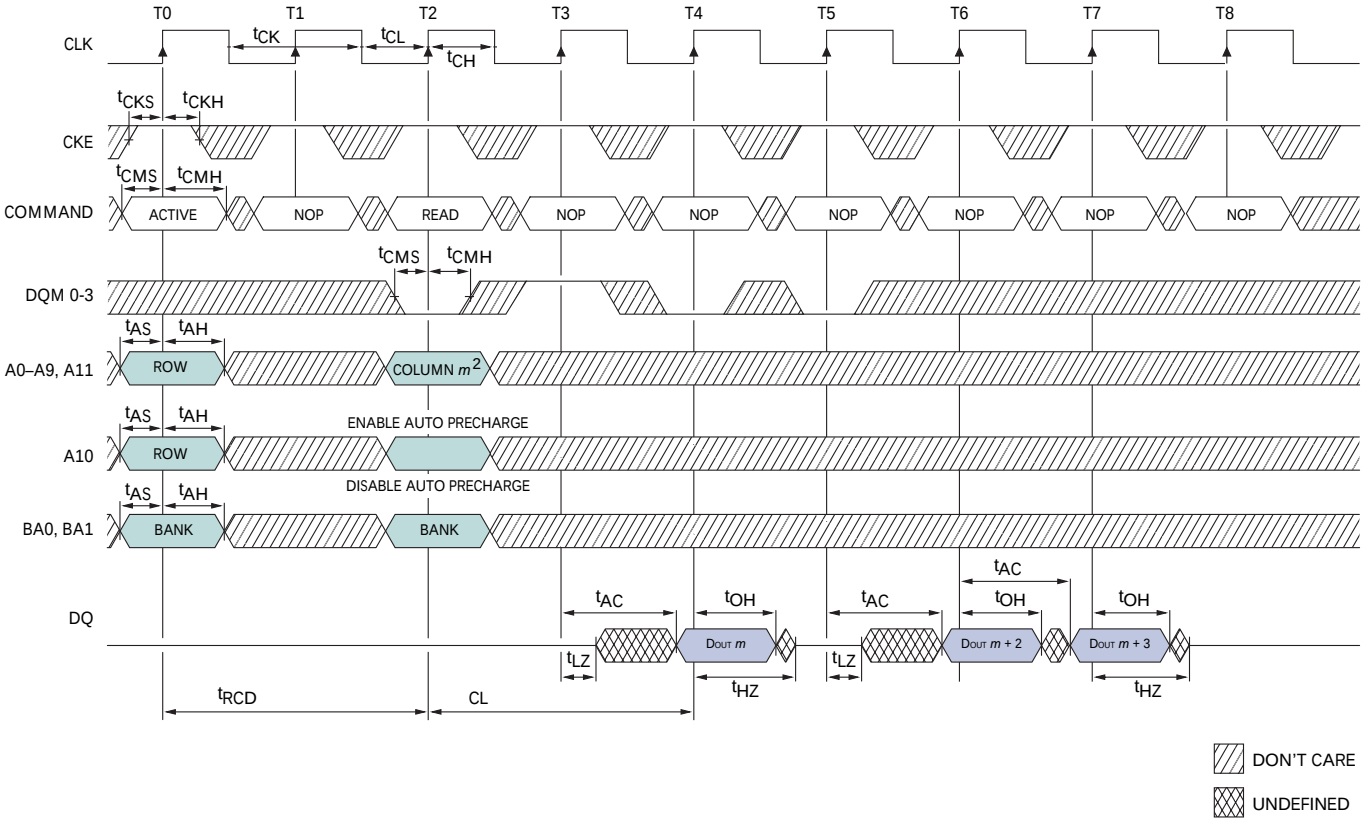

Notes: 1. For this example, BL = 4, CL = 2.
2. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 44: Read – Full-page Burst[1]



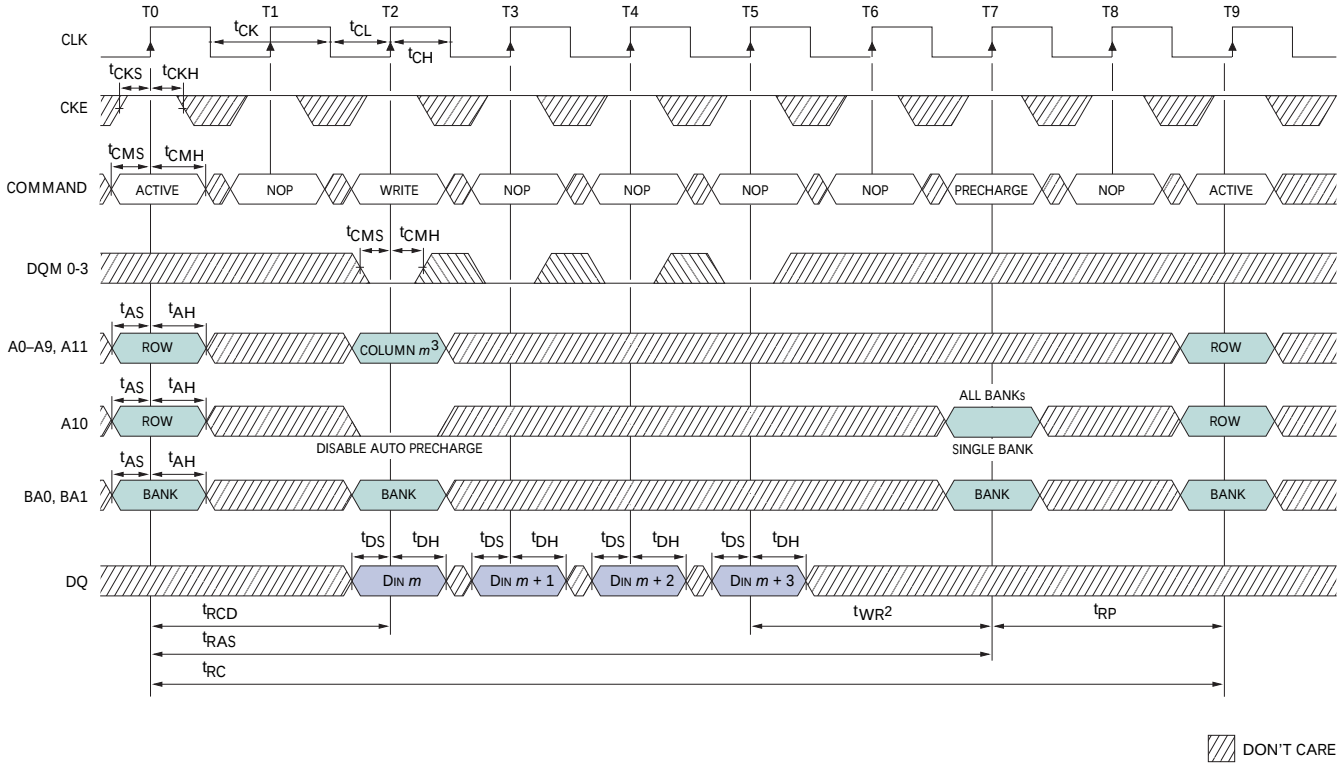

Notes: 1. For this example, CL = 2.
2. A9 and A11 = "Don't Care."
3. Page left open; no tRP.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 45: Read – DQM Operation[1]



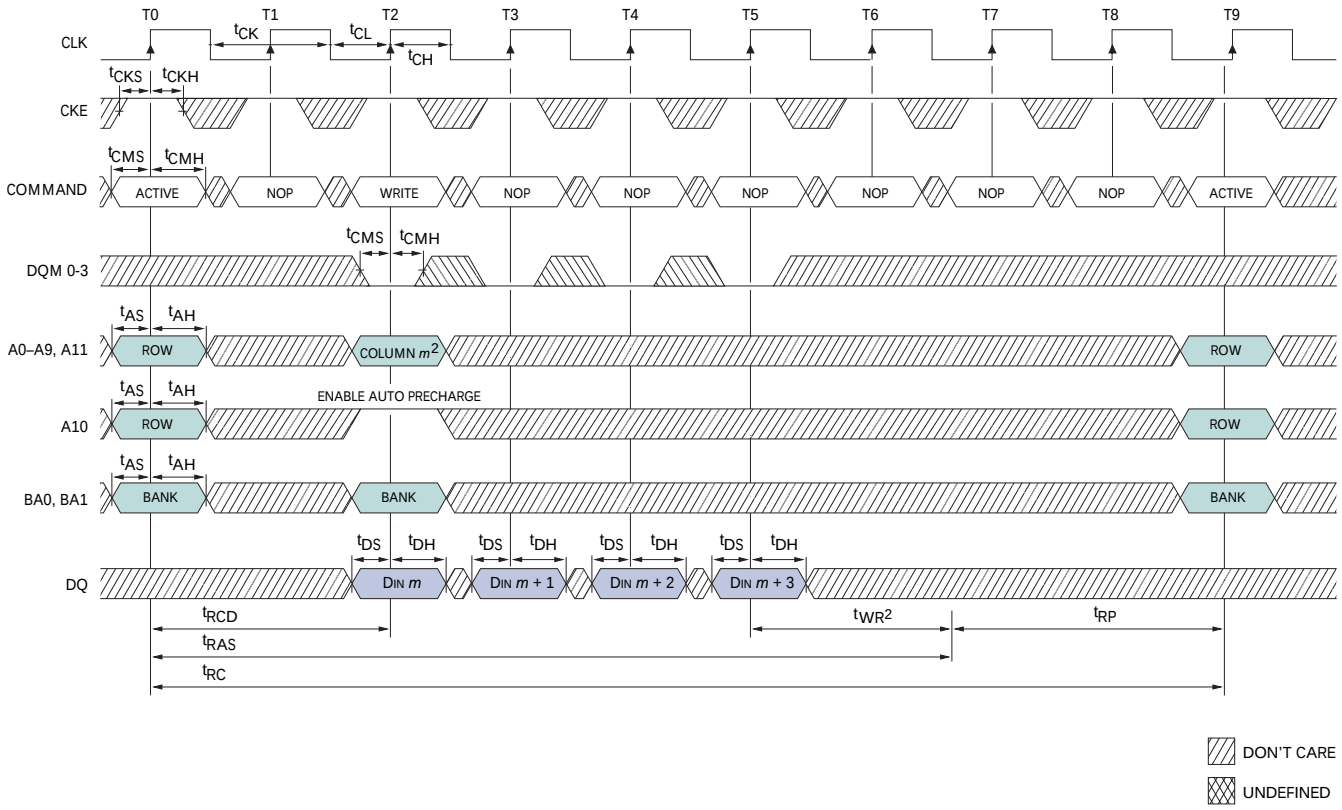

Notes: 1. For this example, CL = 2.
2. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 46: Write – Without Auto Precharge[1]



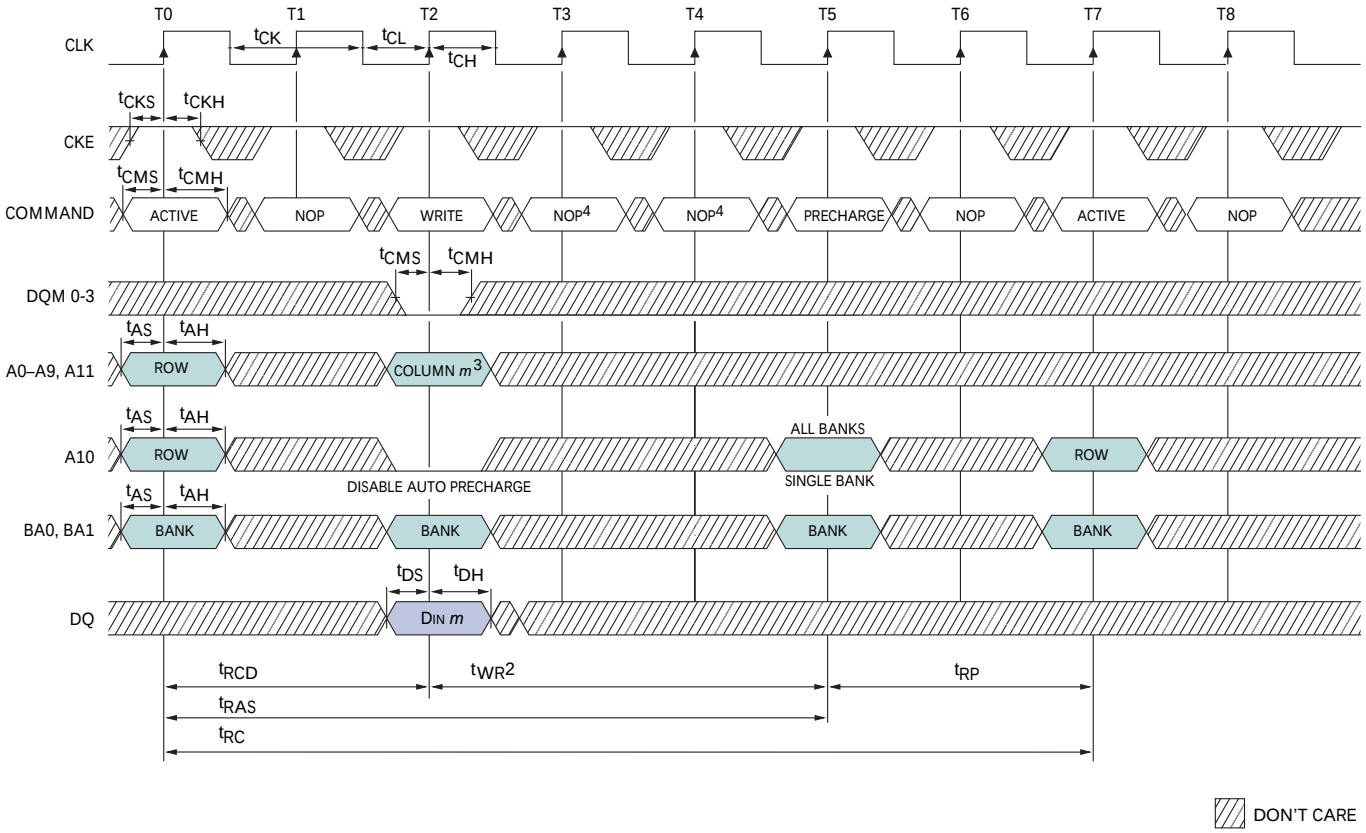

Notes: 1. For this example, BL = 4, and the WRITE burst is followed by a manual PRECHARGE.
2. 15ns is required between <DIN *m* + 3> and the PRECHARGE command, regardless of frequency.
3. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 47: Write – With Auto Precharge[1]



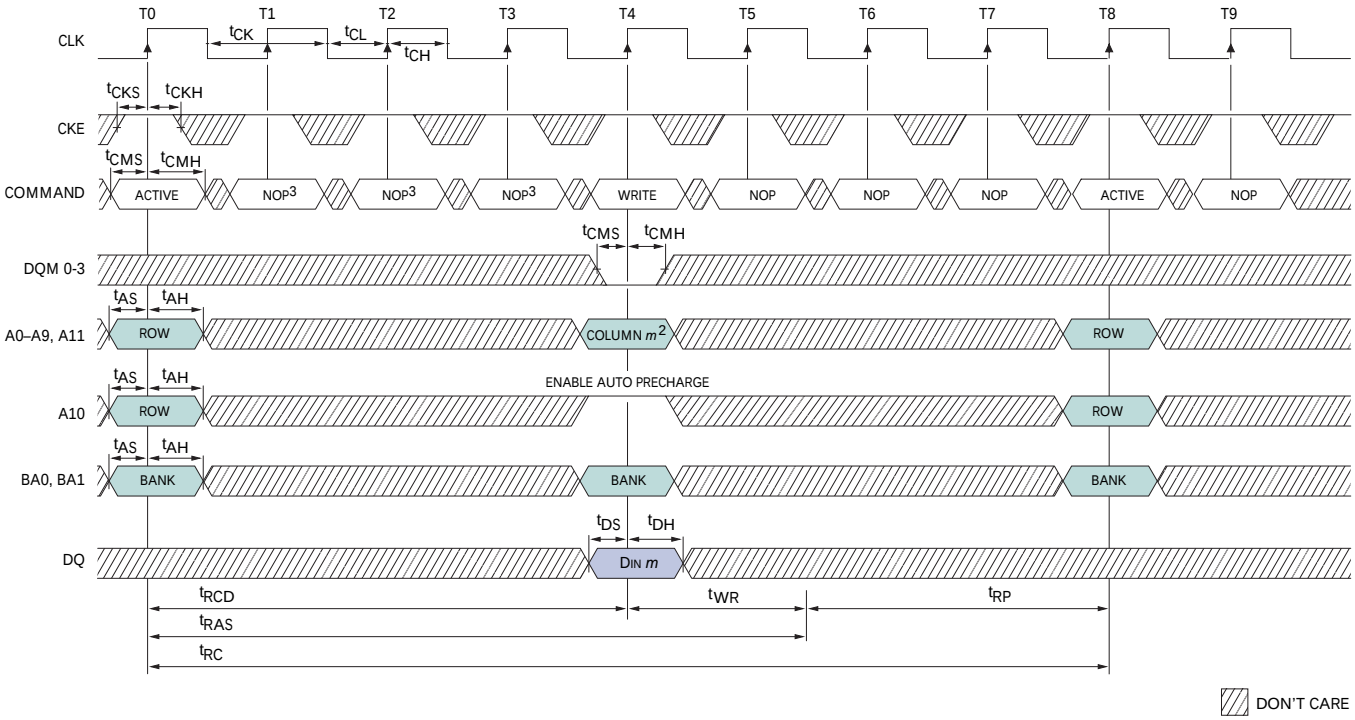

Notes: 1. For this example, BL = 4.
2. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 48: Single Write – Without Auto Precharge[1]



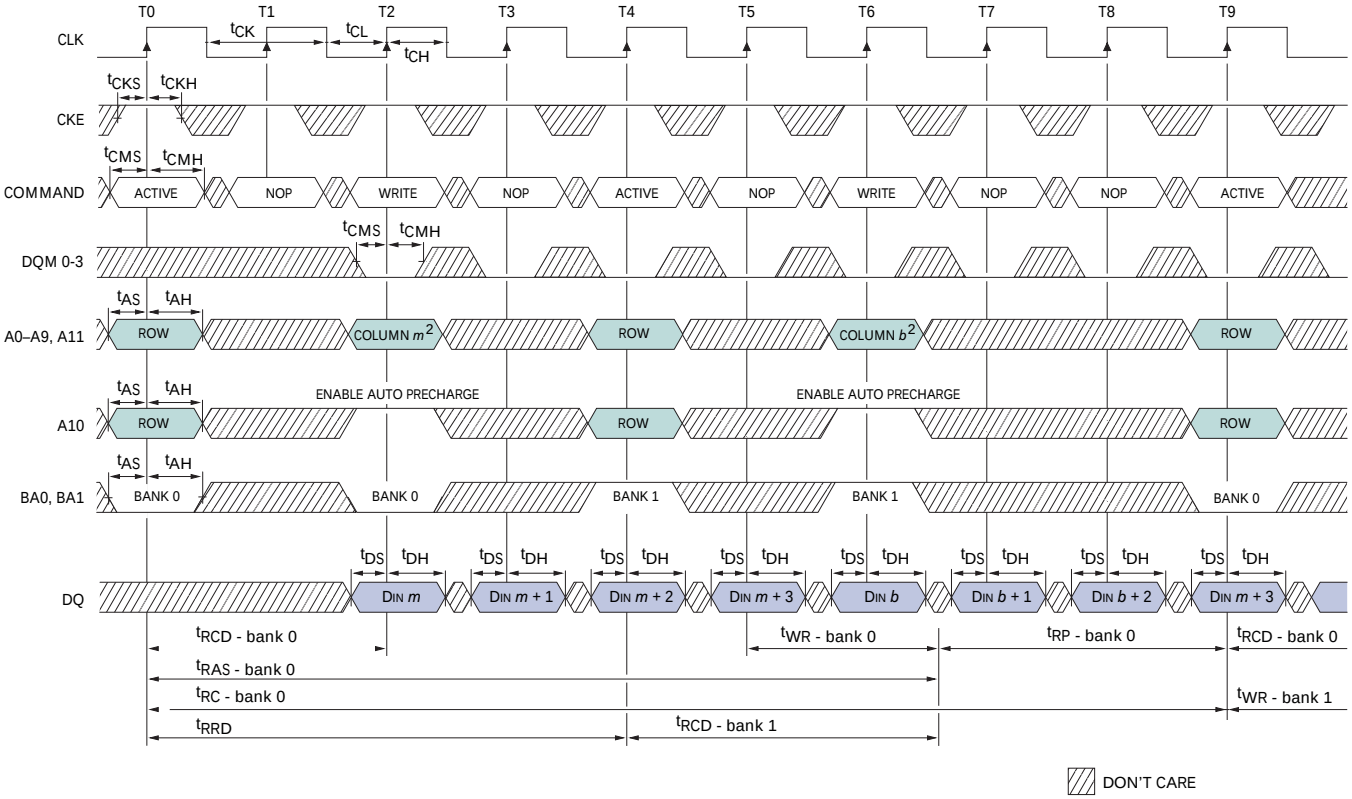

Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE.
2. 15ns is required between <DIN *m*> and the PRECHARGE command, regardless of frequency.
3. A9 and A11 = "Don't Care."
4. PRECHARGE command not allowed else tRAS would be violated.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 49: Single Write – With Auto Precharge[1]



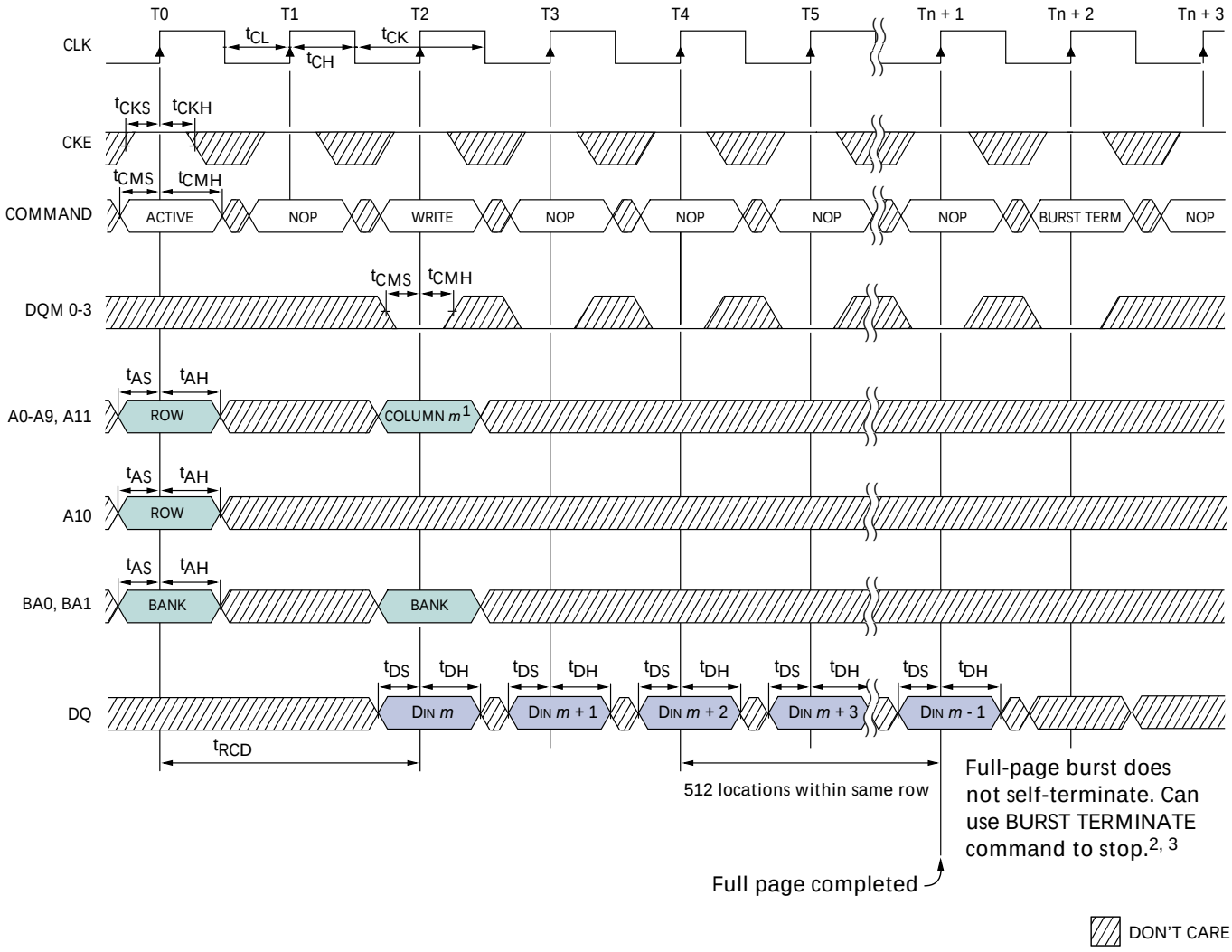

Notes: 1. For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE.
2. 15ns is required between <DIN *m*> and the PRECHARGE command, regardless of frequency.
3. A9 and A11 = "Don't Care."
4. WRITE command not allowed else tRAS would be violated.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 50: Alternating Bank Write Accesses[1]



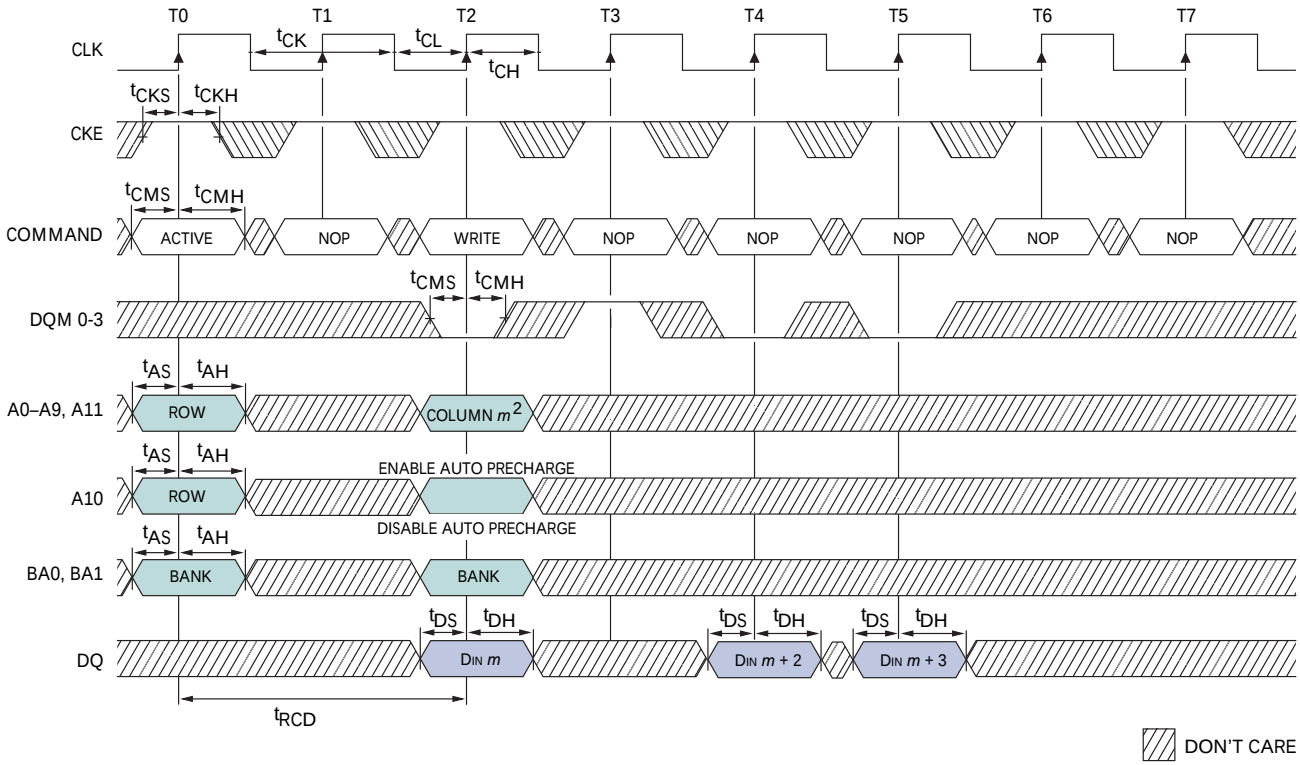

Notes: 1. For this example, BL = 4.
2. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

## Figure 51: Write – Full-page Burst[1]




Notes: 1. A9 and A11 = "Don't Care."
2. tWR must be satisfied prior to PRECHARGE command.
3. Page left open; no tRP.
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

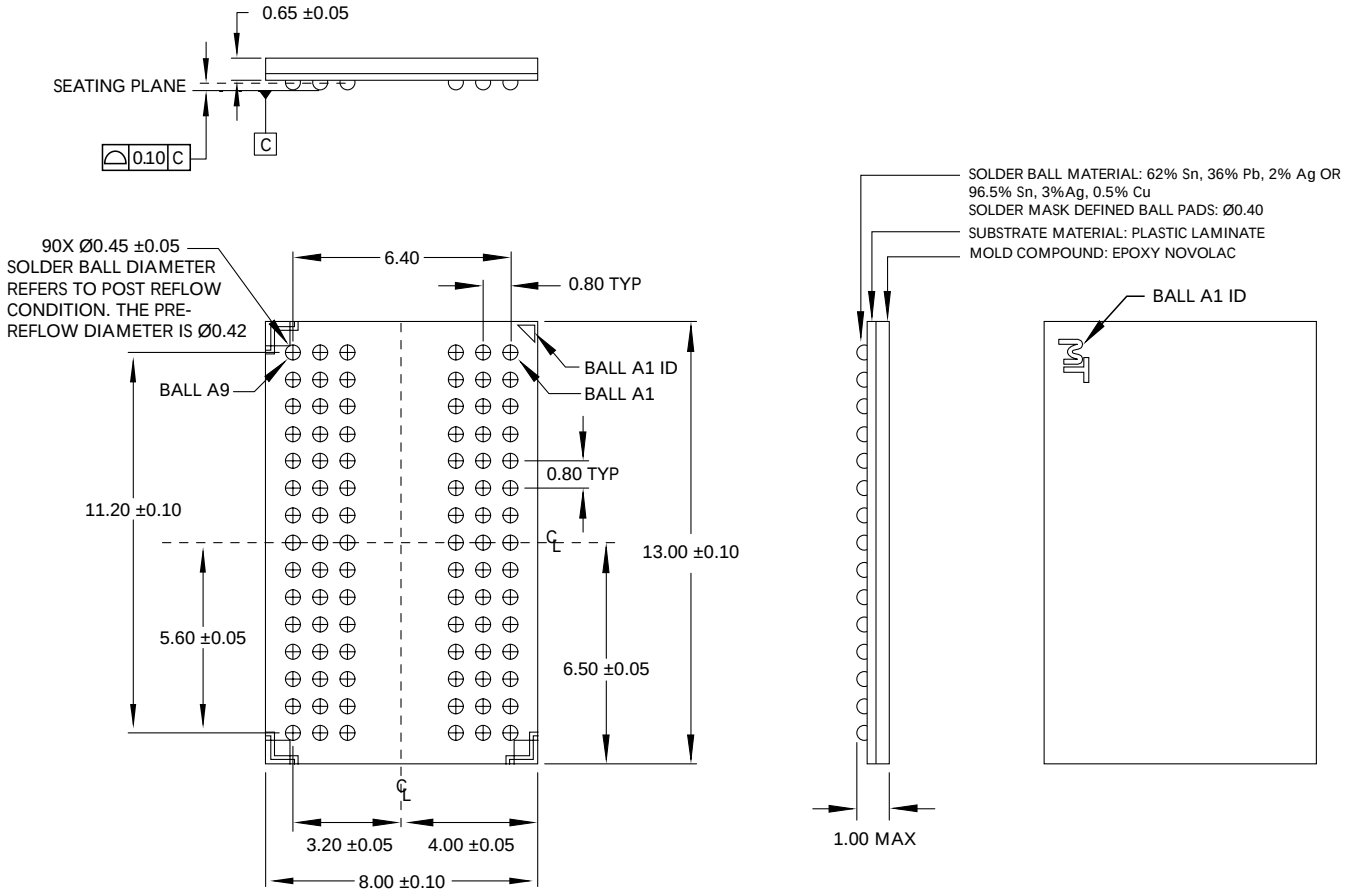
## Figure 52: Write – DQM Operation[1]




Notes: 1. For this example, BL = 4.
2. A9 and A11 = "Don't Care."
See Table 15, Electrical Characteristics and Recommended AC Operating Conditions, on page 48.

# Package Dimensions

## Figure 53: 90-Ball VFBGA (8mm x 13mm)




Note: All dimensions are in millimeters.

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