

## UHF linear power transistor

BLW33

### DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in **linear u.h.f. amplifiers** for television transmitters and transposers. The **excellent d.c. dissipation properties** for class-A operation are obtained by means of diffused emitter ballasting resistors and a multi-base structure, providing an optimum temperature profile on the crystal

area. The combination of optimum thermal design and the application of **gold sandwich metallization** realizes excellent reliability properties.

The transistor has a 1/4" capstan envelope with ceramic cap.

### QUICK REFERENCE DATA

MODE OF OPERATION	$f_{\text{vision}}$ MHz	$V_{\text{CE}}$ V	$I_{\text{C}}$ mA	$T_{\text{h}}$ °C	$d_{\text{im}}^{(1)}$ dB	$P_{\text{o sync}}^{(1)}$ W	$G_{\text{p}}$ dB
class-A; linear amplifier	860	25	300	70	-60	> 1,0	> 10,0
	860	25	300	25	-60	typ. 1,15	typ. 10,5

### Note

1. Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB), zero dB corresponds to peak sync level.

### PIN CONFIGURATION

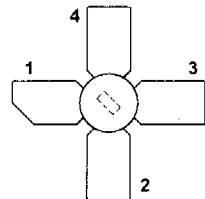


Fig.1 Simplified outline. SOT122A.

### PINNING - SOT122A.

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter



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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage

(peak value);  $V_{BE} = 0$

open base

Emitter-base voltage (open collector)

Collector current

d.c. or average

(peak value);  $f > 1$  MHz

Total power dissipation up to  $T_{mb} = 25$  °C

Storage temperature

Operating junction temperature

$V_{CESM}$  max. 50 V

$V_{CEO}$  max. 30 V

$V_{EBO}$  max. 4 V

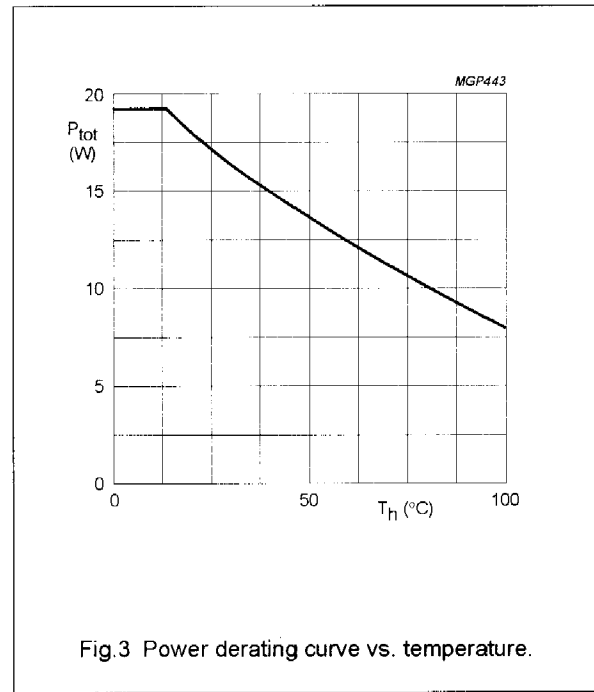
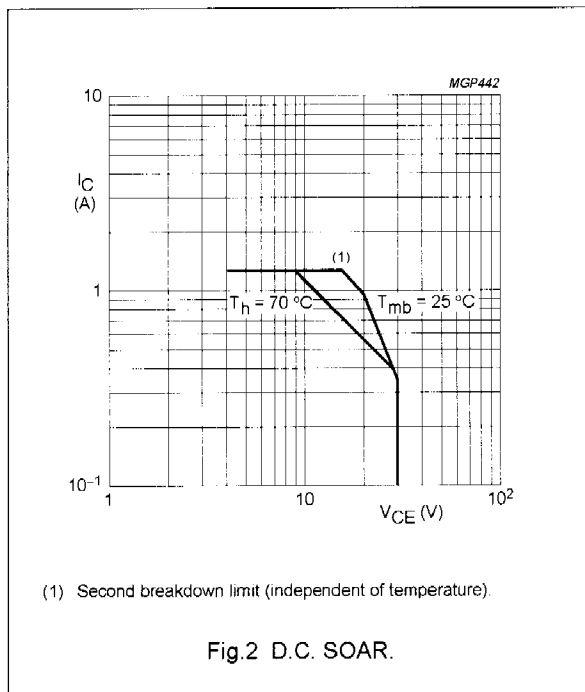
$I_C$  max. 1,25 A

$I_{CM}$  max. 1,9 A

$P_{tot}$  max. 19,3 W

$T_{stg}$  -65 to +150 °C

$T_j$  max. 200 °C



**THERMAL RESISTANCE** (see Fig.4)

From junction to mounting base

(dissipation = 7,5 W;  $T_{mb} = 74,5$  °C; i.e.  $T_h = 70$  °C)

From mounting base to heatsink

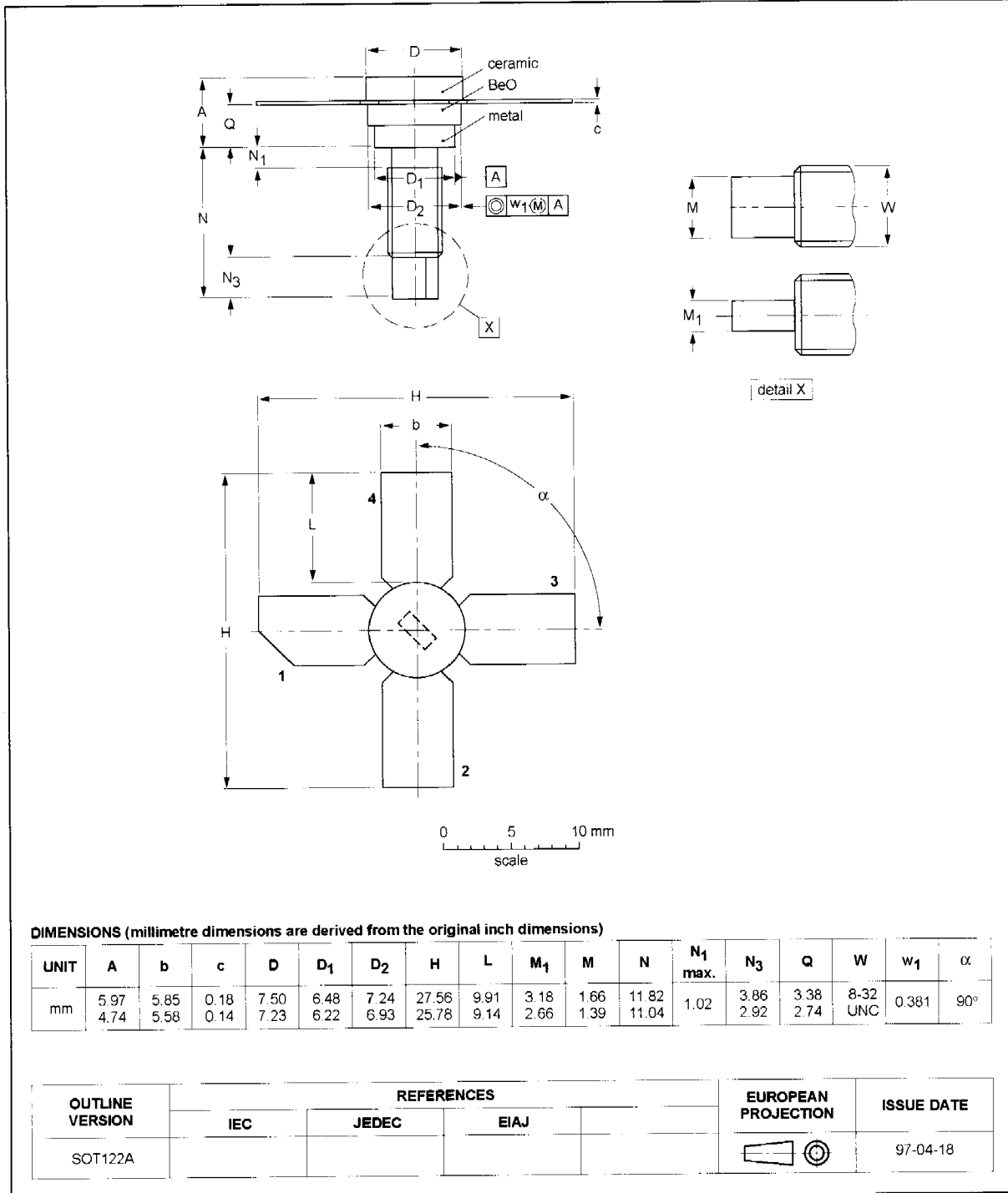
$R_{th\ j-mb} = 10,1$  KW

$R_{th\ mb-h} = 0,6$  KW

PACKAGE OUTLINE

Studded ceramic package; 4 leads

SOT122A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	H	L	M <sub>1</sub>	M	N	N <sub>1</sub> max.	N <sub>3</sub>	Q	W	w <sub>1</sub>	α
mm	5.97 4.74	5.85 5.58	0.18 0.14	7.50 7.23	6.48 6.22	7.24 6.93	27.56 25.78	9.91 9.14	3.18 2.66	1.66 1.39	11.82 11.04	1.02	3.86 2.92	3.38 2.74	8-32 UNC	0.381	90°

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT122A					97-04-18