TW8811 – TFT Flat Panel Controller

with built-in 3D Video Decoder, Triple ADCs, and PIP Support

Preliminary Data Sheet from Techwell, Inc.

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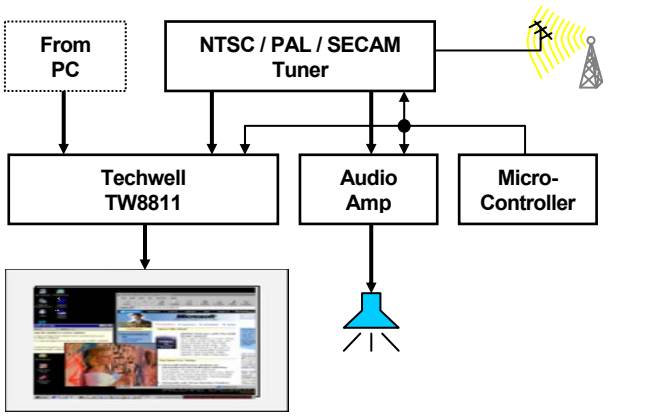
Introduction



Applications

- LCD TVs for home and mobile use
- Computer LCD Panel Monitors with Television
- Portable DVD and DVRs players
- Progressive Scan TV, DTV and HDTV monitors
- Portable media player

Features

The TW8811 incorporates many of the features required to create multi-purpose in-car LCD display system in a single package. It integrates a high quality 3D comb NTSC/PAL/SECAM video decoder, triple high speed RGB ADCs, dual scalers for PIP and multi-PIP support, bit-mapped OSD, TCON, triple DACs and images enhancement functions which include Black and White Stretch, favorite color enhancement and edge enhancement. To further facilitate the move to wide screen displays, it also supports panoramic scaling. On the input side, it supports a rich combination of CVBS, S-video, YPbPr, analog RGB as well as digital YPbPr/RGB inputs. On the output side, it supports both digital and analog panel type with its TTL and analog RGB output.

TW8811 also has a PIP (Picture in Picture) function that can display two sources display simultaneously on single display window. It also has built-in bit-mapped OSD with acceleration as well as 16-bit external OSD support.

Analog Video Decoder

NTSC (M, 4.34) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM with automatic format detection

– Three 10-bit ADCs and analog clamping circuit.

– Fully programmable static gain or automatic gain control for the Y or CVBS channel

– Programmable white peak control for the Y or CVBS channel

– Software selectable analog inputs allows any of the following combinations:

  - Up to 4 composite video
  - Up to 2 S-Video
  - Up to 1 YPbPr

– High quality motion adaptive 3D comb filter for both NTSC and PAL with concurrent 3D noise reduction

– PAL delay line for color phase error correction

– Image enhancement with 2D dynamic peaking and CTI.

– Digital sub-carrier PLL for accurate color decoding

– Digital horizontal PLL and Advanced synchronization processing for VCR playback and weak signal performance.

– Programmable hue, brightness, saturation, contrast, sharpness.

– High quality horizontal and vertical filtered down scaling with arbitrary scale down ratio

– Detection of level of copy protection according to Macrovision standard

– Supports YPbPr input up to 1080i with sub-sampled resolution

– Support automatic standard detection for YPbPr input

Analog RGB Inputs

– Triple high speed 10-bit ADCs with clamping and programmable gain amplifier.

– Up to three independent RGB / YPbPr channels with corresponding SOG

– Built-in line locked PLL with sync separator

– Allows high resolution components inputs like DTV 480p, 720p, 1080i

24bit Digital RGB and 8/16/24-bit YCbCr Inputs

– Allows connection with alternative Video and PC Graphics inputs.

– Support both 656 and 601 video formats

– Allows connection to external HDMI receiver

TFT Panel Support

– Supports panel with resolution up to WXGA

– Supports 3, 4, 6 or 8 bits per pixel up to 16.8 million colors with built-in dithering engine

– Support single channel TTL panel

– Support analog panel with analog RGB output

– Built-in programmable timing controller

On Screen Display

– Supports dual window bitmapped OSD.

– Built-in OSD controller with BitBlit Engine

– Supports variety functions included like blinking, transparency and blending.

– Supports External 16-bit OSD with external alpha blending control.

– Support OSD compression

Image Processing

– Built-in 2D de-interlacing engine with proprietary low angle compensation circuit for smooth video rendering.

– Built-in high quality scaler with nonlinear scaling support

– Programmable hue, brightness, saturation, contrast

– Sharpness control with vertical peaking up to +12db

– Programmable color transient improvement control

– Supports programmable cropping of input video and graphics.

– Independent RGB gain and offset controls

– Panorama / Water-glass scaling

– DTV hue adjustment

– Programmable 10-bit Gamma correction for each color

– Operated in Frame Sync mode only

– Black/White Stretch

– Programmable favorite color enhancement

PIP Function

– PIP with variable sub window size

– POP

– Multiple PIP support

– Built-in high quality down scaling engine for PIP

SDRAM

– Support 16bits Bus width SDRAM

Host Interface

– Supports 2-wire serial bus interface

– Supports 8Bits Parallel Host Interface

– Support DMA transfer

Clock Generation

– Frequency synthesizer with spread spectrum generate memory and display clocks

– Spread spectrum profile based on triangular modulation with center spread

– Modulation frequency and spread width can be selectable

Power Management

– Supports Panel power sequencing.

– Supports DPMS for monitor power management.

– 1.8 / 3.3 V operation

Miscellaneous

– Built-in single CCFL back light controller

– Built-in single LED back light controller

– Power-down mode

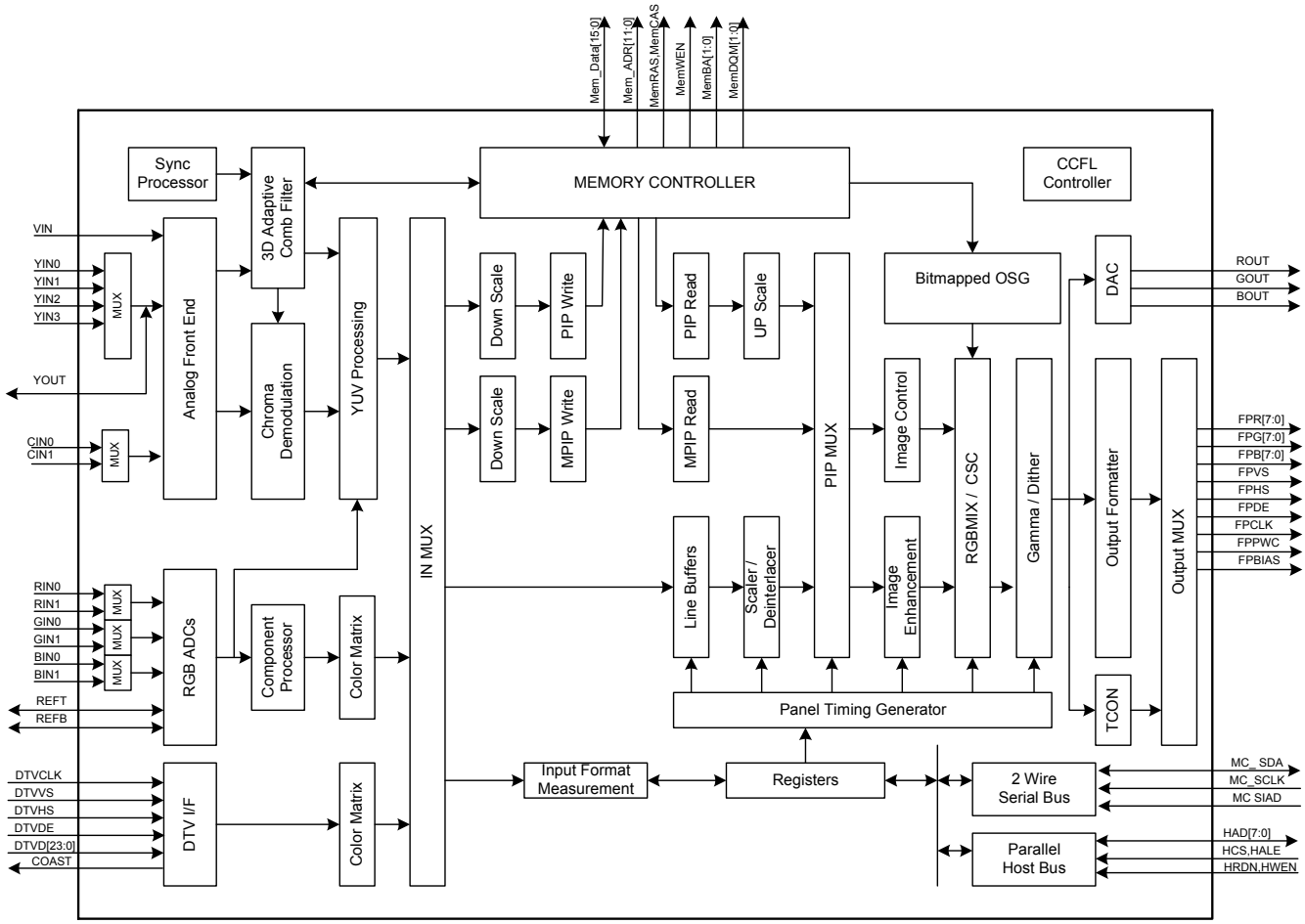
– Single 27MHz crystal

– 208-pin PQFP package

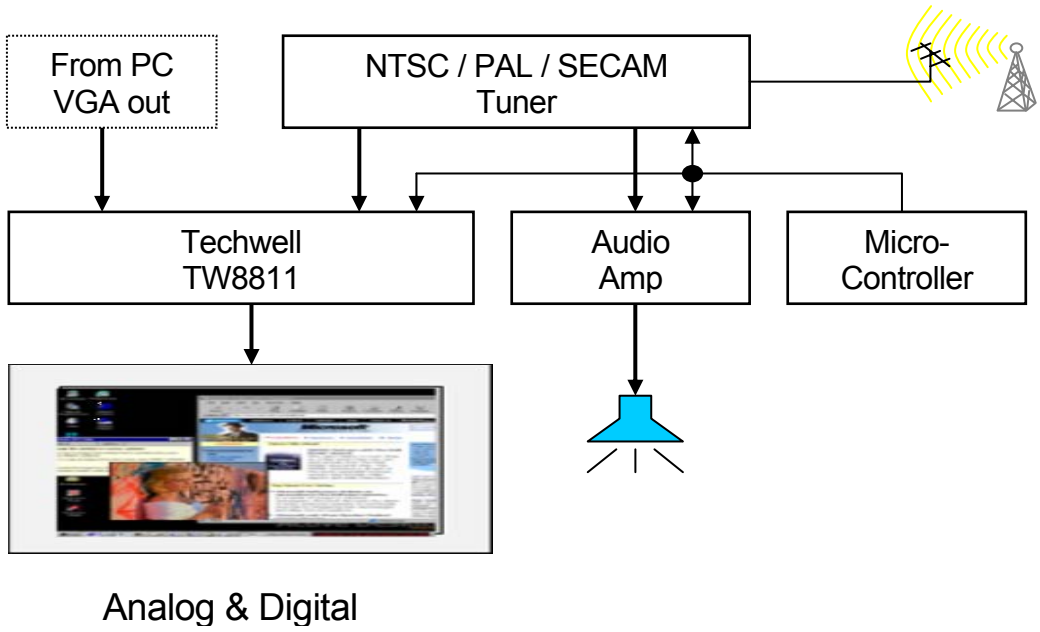
Order Information

Package Description

Part #	Name	Description	Pin Count	Body Size
TW8811	QFP 208	Quad Flat Package	208	28 x 28 mm^2



TW8811 Flat Panel TV/Monitor controller functional block diagram



TW8811 Flat Panel TV or TV + PC Monitor system

Functional Description

Overview

Techwell's TW8811 Flat Panel TV/Monitor controller is a highly integrated TFT panel controller. It integrates a high quality NTSC/PAL/SECAM 3D video decoder, triple high speed ADC, dual scalers for PIP support, timing controller, and flexible bit-mapped OSD engine. This unique level of mixed signal integration turns a TFT panel into a flexible display system. Its built-in triple ADCs and PLL allow both YPbPr and RGB input support. Separate flexible digital inputs interface also allow it to connect other front-end chips. It incorporates easy-to-operate and powerful features in a single package for multi-purpose PC display and LCD entertainment systems.

The TW8811 contains all the logic required to convert standard TV, DTV, and PC monitor signals to the digital control and data signals required to drive various TFT panel types. It supports TTL as well as analog TFT panel resolutions up to WXGA.

The chip accepts CVBS (composite) analog input or S-video analog input or YPbPr component input or analog RGB input for use as a video monitor. Up to 13 analog inputs can be connected simultaneously under external microprocessor control.

The integrated analog front-end contains total six ADCs with clamping circuits and Automatic Gain Control (AGC) circuit on certain channel to minimize external component count. It employs proprietary 3D Comb filter Y/C processing technologies to produce exceptionally high quality pictures.

TW8811 has three high speed ADCs that can support various analog signal inputs up to WXGA.

The chip's internal logic synchronizes the panel frame rate to the incoming input frame rate. A high quality image-scaling engine is used to convert the lower resolution formats or high resolution DTV formats to the output panel resolution. An internal de-interlacing engine also allows interlaced video to be supported.

On Screen Display is supported through either external OSD chip or on-chip OSD for maximum flexibility. A Closed Caption decoder is built in. The TW8811 also accepts a 24 bit digital RGB input from external HDMI™ receiver or ADCs. In addition, it accepts 8/16/24 bits digital YCbCr input.

For the variety for usage, TW8811 has a built-in TCON for direct connecting with low cost TCON-less panel.

The TW8811 also supports TFT panel power sequencing, DPMS (VESATM Display Power Management Signaling) signaling and power management. It also has built-in single channel CCFL or LED back light controller to further simplify the system design. The control interface supports both a 2-wire serial bus interface and 8bit parallel interface. The TW8811 core operates at 1.8 V, the IO at 3.3 V and packaged in a 208-pin LQFP package.

Analog Front-end

The analog front-end converts analog video signals to the required digital format. There are six analog front-end channels. Three channels are dedicated to analog video support. Every channel contains analog anti-aliasing filter, clamping circuit and 10-bit ADCs. It allows the support of CVBS, S-video and YPbPr component input signals for main or sub display. The other three channels are dedicated to YPbPr component video or RGB input support. Every channel contains the analog clamping circuit, variable gain amplifier and ADCs. It allows three separate inputs to be connected simultaneously. A built-in line locked PLL is used to generate the sampling clock for various inputs.

Video Source Selection

TW8811 has total 13 analog inputs for maximum flexibility. Of the 13 inputs, 6 are used for 2 channels of YPbPr/RGB input with corresponding SOG pin. The other 7 inputs are used by video decoder to allow up to 4 CVBS or 2 S-Video or 1 component input. All inputs are software selectable.

Clamping and Automatic Gain Control

All six channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a programmable level. The C, Pb and Pr channels restore the back porch of the digitized video to a level of 128. The R, G, and B channels restore the blank to a level of 16. This operation is automatic through internal feedback loop.

In the case of RGB channel, two clamping modes are provided. When the input is YPbPr signal, the clamping to pre-determined DC level is done through internal feedback loop. When the input is PC RGB signal, the input is self clamped to the zero level.

The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. The white peak protection logic is included to prevent saturation in the case of abnormal proportion between sync and white peak level.

Video Decoder

Sync processor

TW8811 has two sync processors, one for RGB channel and one for video channel. The sync processor of video input detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-Video or component signal. The processor contains a digital phase-

locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal sync processing

The horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. From there, the PLL also provides orthogonal sampling raster for the down stream processor. It has wide lock-in range for tracking any non-standard video signal.

Vertical sync processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. A detection window controls the determination of sync. This provides more reliable synchronization. It simulates the functionality of a PLL without the complexity of a PLL. The field status is determined at vertical synchronization time based on the vertical and horizontal sync relationship.

Color Decoding

Y/C separation

The color-decoding block contains the luma / chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma / chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter can be found in the filter curve section.

In the case of comb filter, the TW8811 separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 3D/2D adaptive comb filter. This technique leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

Color demodulation

The color demodulation for NTSC and PAL standard is done by quadrature mixing the chroma signal to the base band and extracting the chroma components with low-pass filter. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The SECAM color demodulation process consists of bell filtering, FM demodulator and de-emphasis filtering. The chroma carrier frequency is identified in the process and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by transmission loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then compensated in amplitude accordingly. The range of ACC control is –6db to +24db.

Low Color Detection and Removal

For low color amplitude signals, black and white video, or very noisy signals, the color will be “killed”. The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent

oscillation of the color killer operation. This function can be disabled by programming a low threshold value.

Automatic standard detection

The TW8811 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

Video Format support

TW8811 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported by the TW8811

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.58 MHz	Japan
PAL-B, G, N	625	50	4.43 MHz	Many
PAL-D	625	50	4.43 MHz	China
PAL-H	625	50	4.43 MHz	Belgium
PAL-I	625	50	4.43 MHz	Great Britain, others
PAL-M	525	60	3.58 MHz	Brazil
PAL-CN	625	50	3.58 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.43 MHz	China
NTSC (4.43)	525	60	4.43 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

Luminance Processing

The TW8811 decoder adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW8811 decoder also provides a sharpness control function through a control register. The center frequency of the peaking filter is selectable. A coring function is provided along with the sharpness control to reduce enhancement to the noise.

The Hue and Saturation

When decoding NTSC signals, TW8811 decoder can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Analog RGB / YPbPr Processor

Analog Front-end

This input path has three ADCs to support analog RGB input or YPbPr input. The built-in clamping circuit works based on the mode selected. Every channel includes variable gain amplifier for gain adjustment. Both gain and offset can be adjusted for flexibility. Two software selectable inputs are available for each channel to allow two inputs to be connected simultaneously. Both separated H/V sync and sync-on-green are supported.

Sync Processor

The sync processor for the RGB channel either takes the separated H/V sync input or separates the composite sync input from one of the SOG inputs into H/V sync for driving the on-chip sampling PLL. It contains necessary logics to detect and bypass irregular syncs. The on-chip PLL has sub-phase control to enable accurate sampling timing.

Component Processor

There are built-in color space converter and tint control logic for the YPbPr input. During YPbPr component input operation, luminance Contrast and Brightness as well as Pb / Pr Saturation can be controlled by registers. In the case of RGB mode, the gain and offset of RGB can also be digitally controlled.

Digital Input Support

In addition to analog inputs, the TW8811 has a 24-bit digital input for YPbPr or RGB data. The input includes VSYNC, HSYNC, pixel clock and the optional data qualifier. For interlaced video, the timing relationship between VSYNC and HSYNC determine the field flag. The optional data qualifier is needed when input video data is not continuously valid within a line. For the YPbPr mode, TW8811 can support 8-bit 656 as well as 8/16-bit 601 modes. The 656 interface supports both interlaced and progressive standard.

TFT Panel Support

The TW8811 supports varieties of active matrix TFT panels including TTL, as well analog panel. It supports panel with resolution up WXGA resolution.

Dithering

If the color depth of the input data is larger than the LCD panel color depth, the TW8811 can be set to dither the image. Up to four bits of apparent color depth can be added with the internal dithering ability of the TW8811. This allows LCD panels with 4, 6 or 8 bits per color per pixel to display up to 16.8 million colors and LCD panels with 3 bits per color per pixel to can display up to 2.1 million colors.

The TW8811 has both spatial and frame modulation dithering. When dithering with the least significant 4-bits of input data the TW8811 uses spatial modulation with 4x4 blocks of pixels. When dithering with the least significant 1 to 3 bits of input data, the TW8811 uses either spatial modulation with 2x2 pixel blocks, or frame modulation.

Image Control

Input Image Control

The input cropping control provides a way for programming the active display window region for the selected input video or graphic. In the normal operation, the first active line starts with the VSYNC signal. This and vertical active length register setting are used to determine the active vertical window. The active pixel starts HSYNC. This and the horizontal active width register are used to determine the active horizontal window. The vertical window is programmed in line increments. The horizontal window is programmed in one pixel increments for single pixel input mode or two pixels increments for double pixels input mode. If data qualifier is used, then only qualified pixels will be counted in the window size.

Image Scaling

The TW8811 internal image-scaling engine operates in several modes. The first is the bypass mode. No image scaling is done in this mode. The number of active output lines per frame and the number of active output pixels per line are identical to the input active lines and pixels, respectively. This mode is best used for displaying computer graphic at panel's native resolution.

By default, the input active window is zoomed up to the full screen for display. This is used for non-interlaced data like PC graphics or progressive scan video. The vertical and horizontal magnification ratio can be adjusted independently. TW8811 has frame-sync mode which does not use frame buffer. In this mode, the zoom ratio and output clock rate should be coordinated appropriately to avoid internal buffer overrun.

The TW8811 has a de-interlacing mode to process interlaced video inputs. In this mode, every input field is zoomed to the full output frame resolution. The de-interlaced fields can also be properly compensated to have fields aligned correctly to avoid any artifacts. The offset can be programmed to provide maximum flexibility.

The horizontal scaler can be programmed to perform non-linear scaling : panorama scaling for displaying 4:3 input on a 16:9 display and water-glass scaling for displaying 16:9 input on a 4:3 display.

Image Enhancement Processing

Adaptive Black/White Stretch

This feature is to expand dynamic range of the input image, which creates more vivid image impression.

Favorite Color enhancement

TW8811 provides three independent color enhancements. The center axis of each color can be adjusted over a 360 degrees range provided none of those two are overlapped. The range and the amount of enhancement can also be independently adjusted.

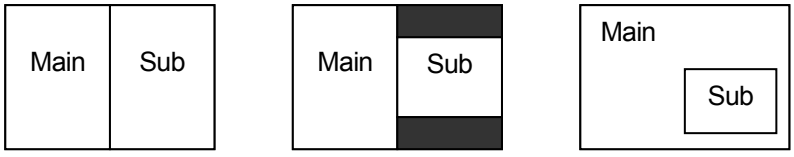
Picture-In-Picture

Double Window / Picture-in-Picture (PIP)

TW8811 can display two live pictures on a single display. In the case of what we called PIP, small size of sub-window can be displayed over full size of main-window.

The frame (outline of window) can be added with choice of color and width.

Example of double window modes

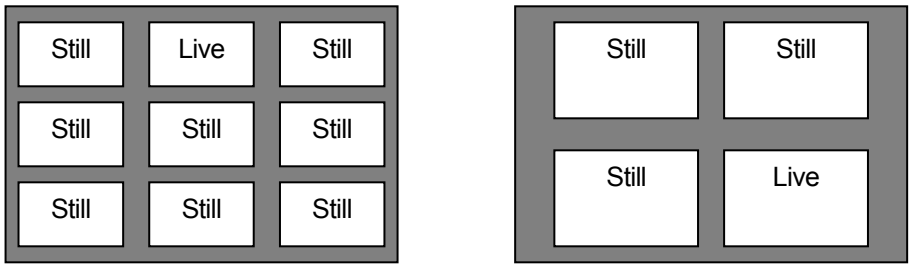


Multiple Window

In case of Multiple Window, multiple images come from one of the source can be displayed on a single display. Only one of the window can be live (motion picture) and the others will be previously stored still image. User also can freeze live window by register set.

User can overlay main-window over multiple-windows.

Example of multiple window modes



PIP alpha blending

PIP image can be used as an OSD type overlay graphics. User can specify specific color as a 'key color' which disabling overlaying and showing behind main image. Where PIP and main image are overlaid, user can define blending ratio (Alpha1). And also can define blending ratio of main image with Black color (Alpha2) as a dimming function.

[Usage]

- Enable PIP alpha blending (0x2EF[7] = 1). Enable 565 mode (0x2EF[6] = 1) as well, if it is preferred.

- Set 'Key color' center level by using Rkey (0x2F0), Gkey (0x2F1) and Bkey (0x2F2). Also set 'Key range' (0x2F3) for the 'Key color' deviation from its center setting.

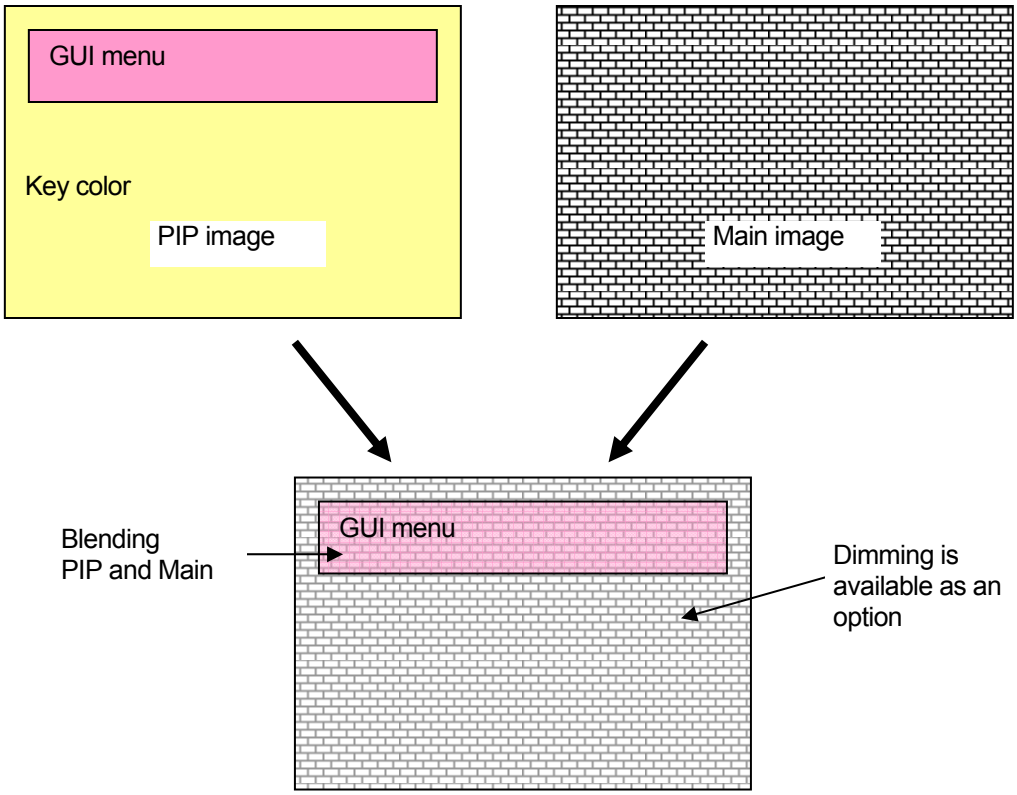
- Turn on 'Key position display' mode if you want to make sure the area detected as 'Keyed'.

- Adjust Alpha1 (0x2EF[4:0]) and Alpha2 (0x2E6[4:0]).

[Limitations]

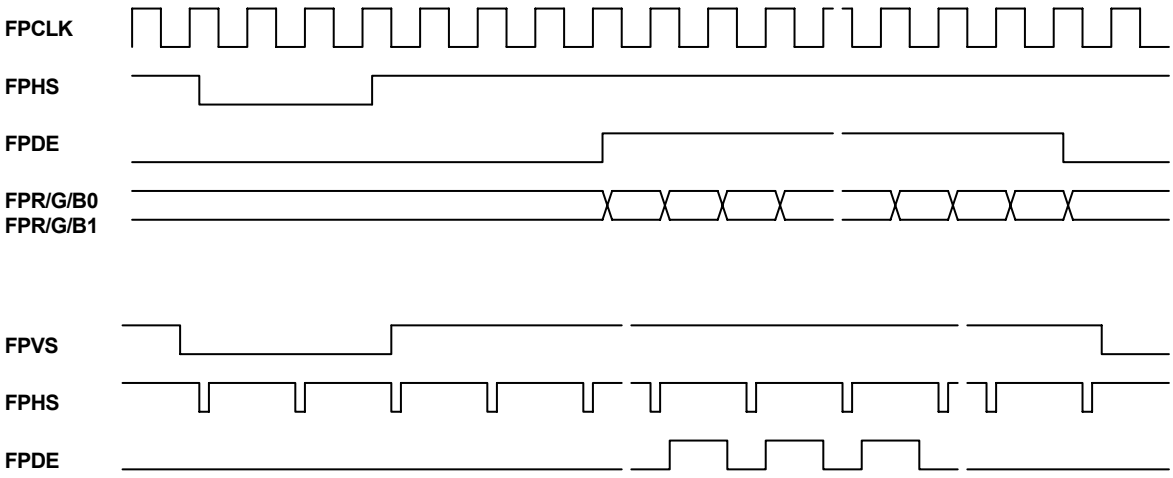
- When 565 mode, color depth is limited and may show steps on original gradation.

- When 565 mode, try to choose color of input image which truncated portion (LSB 2 bit will be truncated in Y, LSB 3 bit in Cb and Cr) has about middle value (If 3 bit is truncated, these portion better have value of around 3 or 4) to avoid input level translated into 2 different output level due to noise. (If input is digital signal, this situation may be avoidable.)



Display Timing

The TW8811 is operated in Frame Sync mode only with no external memory required. In this mode, the output frame rate is synchronized with the input frame rate. Since there is no frame buffer, the display clock frequency and zoom ratio have to be properly selected to match the panel resolution. The internal scaling engine absorbs the difference between the input line rate and output line rate as well as the difference between the input pixel rate and output pixel rate.



Flat Panel Output Signals

The frequency of the Flat Panel Clock Output pin can be controlled by an internal frequency synthesizer. It also has spread spectrum function to reduce EMI. The frequency equation of the Flat Panel Clock Output signal is described in the register section.

On Screen Display

TW8811 OSD controller supports bitmap with 4/8 Bit-per-pixel mode. The powerful Bit-Blit Engine makes your system more fancy. Any pixel can be assigned any one of 16 user-defined true colors. Using 24 bits x 16 Look-Up-Table, user can achieve 16 true color from 24 bits true color. The TW8811 OSD architecture doesn't use any internal memory.

Bitmapped mode

The bitmap is loaded into external SDRAM with same way as Character-mapped mode. User can define the displayed pixel colors on a pixel by pixel basis. The pixels can be represented using either 4 bits per pixel(16 simultaneous colors). The maximum bitmapped image size depends on panel resolution and SDRAM size. Our recommendation is 512(H) x 512(V).

External OSD port

A dedicated port is provided for an external OSD controller. The TW8811 provides the HACTIVE, VSYNC and dot clock signals, and external OSD controller provides a 18 bits color data values together with valid data indicator (6 bits for each R, G and B color). It's compatible with popular OSD controllers from Renesas (Mitsubishi) and other companies.

In case of 18 bit OSD data reception, color palette is not used and 18 bit data represents 262144 color space directly.

Microcontroller Interface

The TW8811 registers are accessed via 2-wire serial bus interface as well as parallel host interface. It operates as a slave device.

Two Wire Serial Bus Interface

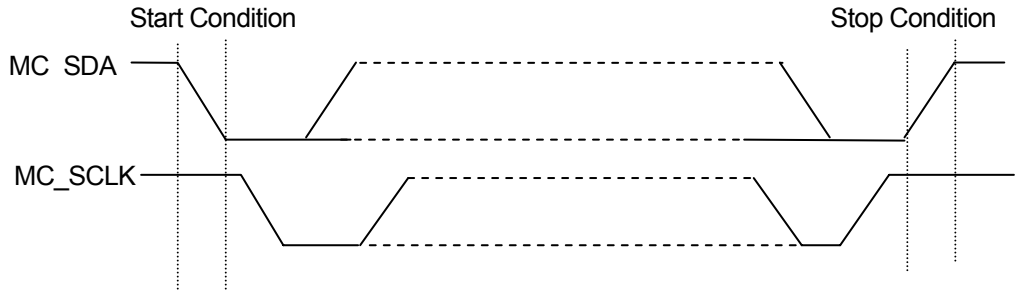


Figure 1. Definition of the serial bus interface bus start and stop

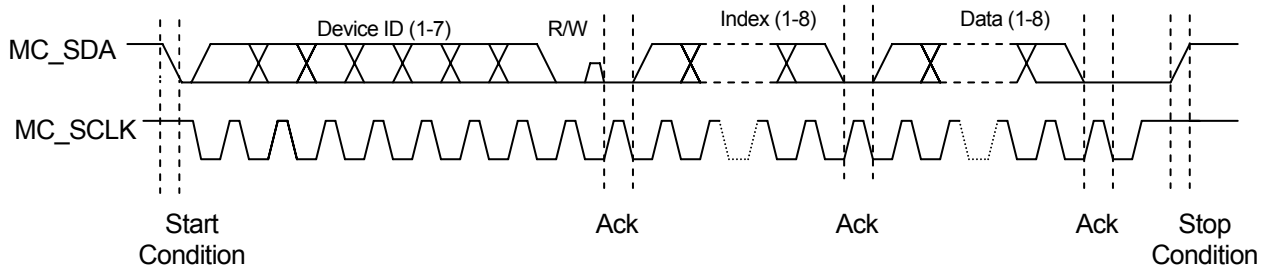


Figure 2. One complete register Write sequence via the serial bus interface

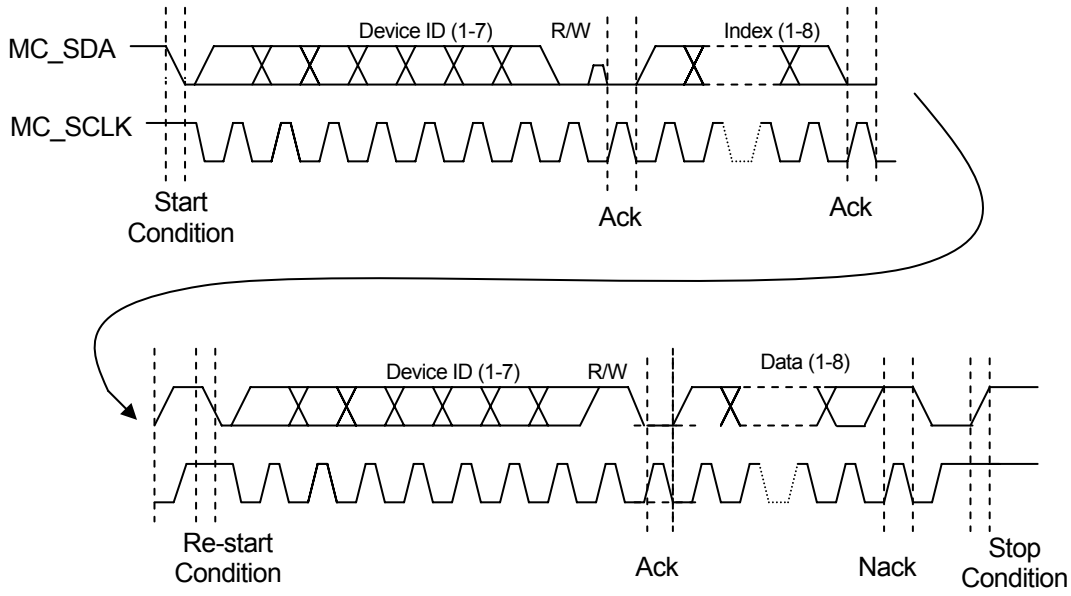


Figure 3. One complete register Read sequence via the serial bus interface

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW8811 registers. MC_SCLK is the serial clock and MC_SDA is the data line. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling MC_SCLK and MC_SDA low through open drain outputs. In normal operation the master generates all clock pulses, but control of the MC_SDA line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever MC_SCLK is high.

The TW8811 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the ADDRSEL (Serial Interface Address) pin ether to VDD or GND (See Table 2.). If the ADDRSEL pin is tied to VDD, then the least significant bit of the 7-bit address is a “1”. If the ADDRSEL pin is tied to GND then the least significant bit of the 7-bit address is a “0”. The most significant 6-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives MC_SDA from high to low, while MC_SCLK is high, this is defined to be a start condition (See Figure 1.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for the their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 2. (For the TW8811, the next byte is normally the index to the TW8811 registers and is a write to the TW8811 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the MC_SDA line while holding MC_SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the MC_SDA line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of the TW8811, the master sends another 8-bits of data, the TW8811 loads this to the register pointed by the internal index register. The TW8811 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW8811 if they are in ascending sequential order. After each 8-bit transfer the TW8811 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW8811 the host will issue a stop condition.

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	0	ADDRSEL	1=Read 0=Write

Table 2. TW8811 serial bus interface 7-bit slave address and read write bit

A TW8811 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See figure 3). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the MC_SDA line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (MC_SDA is left high during a clock pulse) and issue a stop condition.

Parallel Host Interface for 8bit Micro Processor

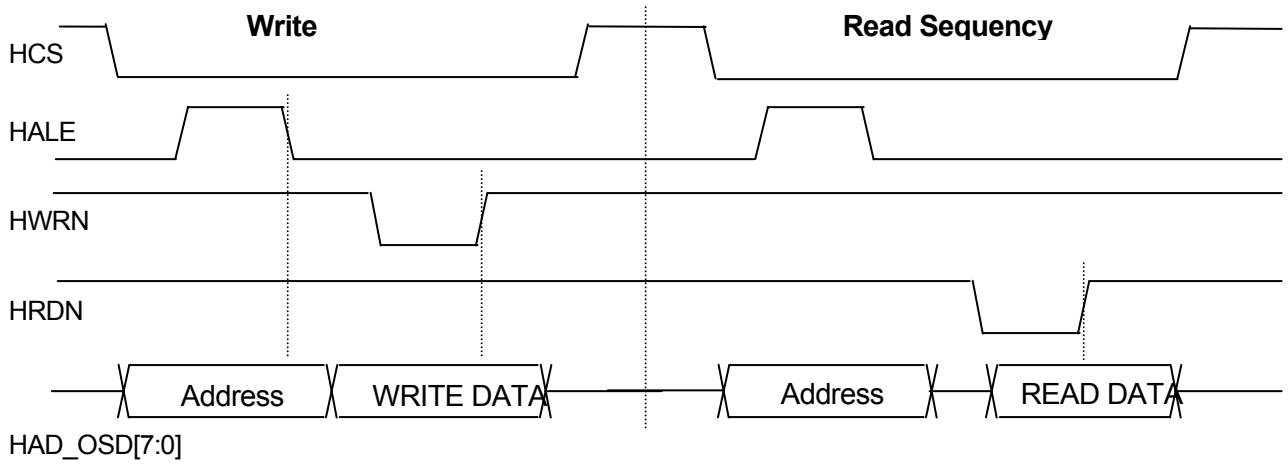


Figure 4. Parallel Interface mode1 Timing Diagram. (HOST = 0)

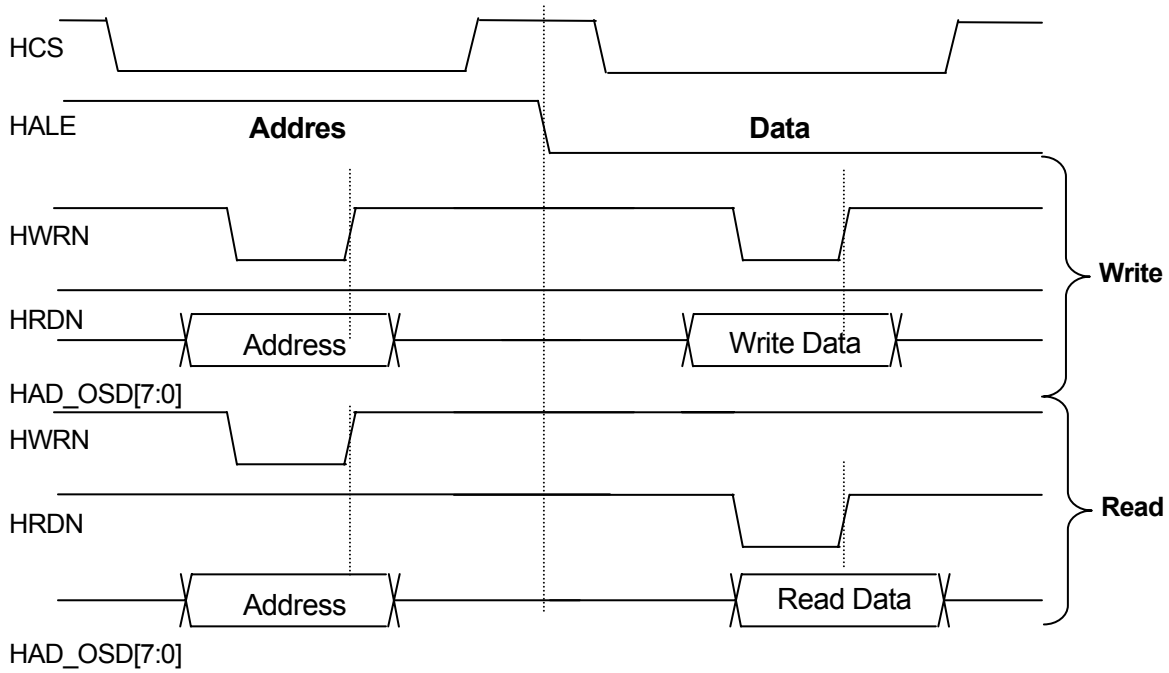


Figure 5. Parallel Interface mode2 Timing Diagram. (HOST =1)

Power Management

The TW8811 supports panel power sequencing. Typical TFT panels require different parts of the panel power to be applied in the right sequence to avoid premature damage to the panel. Pins are provided to control the panel backlight generator, digital circuitry and panel driver, separately. The TW8811 controls the power up and power down sequence for the LCD panels. The time lapses between different stages of the sequence are independently programmable to meet various power sequencing requirements.

The TW8811 also supports VESA™ DPMS for monitor power management. It can detect the DPMS status from input sync signals and automatically change into On/Off mode. To support the power management, the TW8811 has three operating modes: Power On mode, Power Off mode, and Panel Off mode. All the DPMS power saving mode will be covered by the Power Off mode.

Gamma Correction

TW8811 has built-in independent RGB 10-bit Gamma RAM for the purpose of table lookup Gamma correction.

Memory Interface

TW8811 supports external SDRAM for various functions including bit-mapped OSD, 3D comb, 3D noise reduction and PIP that require memory buffer. The memory controller of the TW8811 supports 16bit data width up to 133 MHz clock rate.

When power is up, it is reset by the internal reset signal and wait for the initial memory- timing period. To configuration of the SDRAM internal register memory controller performs initial cycle. After all initial cycles performed, memory controller does the normal operation. The memory controller performs arbitration, access timing generation and refresh and configuration.

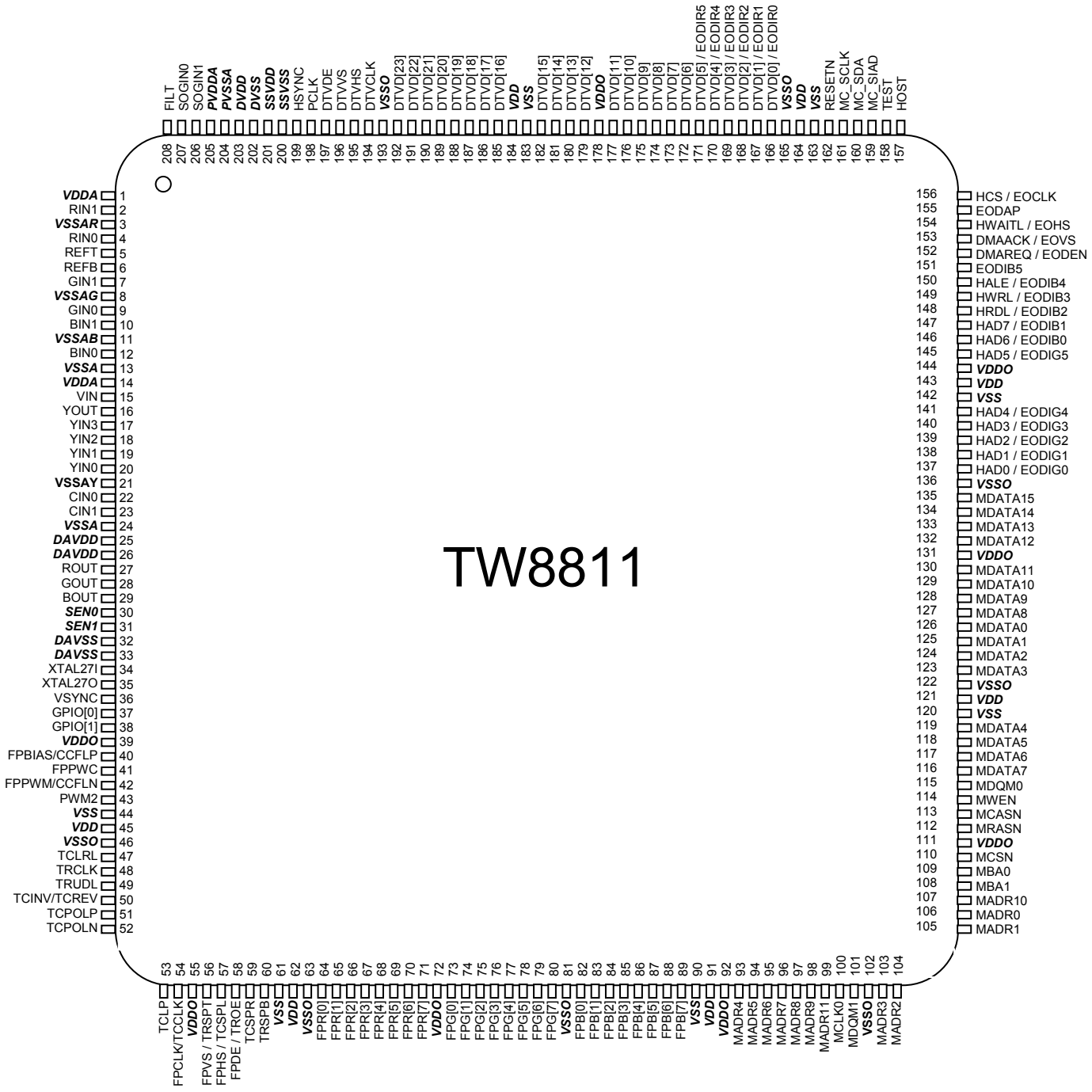
Test Modes

The TEST1 input pin provides test mode selection. If this pin is low at the rising edge of the RESET# pin and remains low, the TW8811 is in its normal operating mode. Table 3 shows the other test modes made available with this pin.

Table 3 Test modes

Test mode	TEST1 Before RESET# rising edge	TEST1 After RESET# rising edge	Description
Normal	0	0	Normal operation
Output tri-state	0	1	In this mode, all pin output drivers are tri-stated. Pin leakage current parameters can be measured.
Outputs high	1	0	In this mode, all pin output drivers are forced to the high output state. V_{OH} and I_{OH} can be measured.
Outputs low	1	1	In this mode, all pin output drivers are forced to the low output state. V_{OL} and I_{OL} can be measured.

Pin Diagram


TW8811
1 VDDA
2 RIN1
3 VSSAR
4 RIN0
5 REFT
6 REFB
7 GIN1
8 VSSAG
9 GIN0
10 BIN1
11 VSSAB
12 BIN0
13 VSSA
14 VDDA
15 VIN
16 YOUT
17 YIN3
18 YIN2
19 YIN1
20 YIN0
21 VSSAY
22 CIN0
23 CIN1
24 VSSA
25 DAVDD
26 DAVDD
27 ROUT
28 GOUT
29 BOUT
30 SEN0
31 SEN1
32 DAVSS
33 DAVSS
34 XTAL27I
35 XTAL27O
36 VSYNC
37 GPIO[0]
38 GPIO[1]
39 VDDO
40 FPBIAS/CCFLP
41 FPPWC
42 FPPWM/CCFLN
43 PWM2
44 VSS
45 VDD
46 VSSO
47 TCLRL
48 TRCLK
49 TRUDL
50 TCINV/TCREV
51 TCPOLP
52 TCPOLN
53 TCLP
54 FPCLK/TCCLK
55 VDDO
56 FPVS / TRSPT
57 FPHS / TCSPL
58 FPDE / TROE
59 TCSPR
60 TRSPB
61 VSS
62 VDD
63 VSSO
64 FPR[0]
65 FPR[1]
66 FPR[2]
67 FPR[3]
68 FPR[4]
69 FPR[5]
70 FPR[6]
71 FPR[7]
72 VDDO
73 FPG[0]
74 FPG[1]
75 FPG[2]
76 FPG[3]
77 FPG[4]
78 FPG[5]
79 FPG[6]
80 FPG[7]
81 VSSO
82 FPB[0]
83 FPB[1]
84 FPB[2]
85 FPB[3]
86 FPB[4]
87 FPB[5]
88 FPB[6]
89 FPB[7]
90 VSS
91 VDD
92 VDDO
93 MADR4
94 MADR5
95 MADR6
96 MADR7
97 MADR8
98 MADR9
99 MADR11
100 MCLK0
101 MDQM1
102 VSSO
103 MADR3
104 MADR2
105 MADR1
106 MADR0
107 MADR10
108 MBA1
109 MBA0
110 MCSN
111 VDDO
112 MRASN
113 MCASN
114 MWEN
115 MDQM0
116 MDATA7
117 MDATA6
118 MDATA5
119 MDATA4
120 VSS
121 VDD
122 VSSO
123 MDATA3
124 MDATA2
125 MDATA1
126 MDATA0
127 MDATA8
128 MDATA9
129 MDATA10
130 MDATA11
131 VDDO
132 MDATA12
133 MDATA13
134 MDATA14
135 MDATA15
136 VSSO
137 HAD0 / EODIG0
138 HAD1 / EODIG1
139 HAD2 / EODIG2
140 HAD3 / EODIG3
141 HAD4 / EODIG4
142 VSS
143 VDD
144 VDDO
145 HAD5 / EODIG5
146 HAD6 / EODIB0
147 HAD7 / EODIB1
148 HRDL / EODIB2
149 HWRL / EODIB3
150 HALE / EODIB4
151 EODIB5
152 DMAREQ / EODEN
153 DMAACK / EOVS
154 HWAITL / EOHS
155 EODAP
156 HCS / EOCLK
157 HOST
158 TEST
159 MC_SIAD
160 MC_SDA
161 MC_SCLK
162 RESETN
163 VSS
164 VDD
165 VSSO
166 DTVD[0] / EODIR0
167 DTVD[1] / EODIR1
168 DTVD[2] / EODIR2
169 DTVD[3] / EODIR3
170 DTVD[4] / EODIR4
171 DTVD[5] / EODIR5
172 DTVD[6]
173 DTVD[7]
174 DTVD[8]
175 DTVD[9]
176 DTVD[10]
177 DTVD[11]
178 VDDO
179 DTVD[12]
180 DTVD[13]
181 DTVD[14]
182 DTVD[15]
183 VSS
184 VDD
185 DTVD[16]
186 DTVD[17]
187 DTVD[18]
188 DTVD[19]
189 DTVD[20]
190 DTVD[21]
191 DTVD[22]
192 DTVD[23]
193 VSSO
194 DTVCLK
195 DTVHS
196 DTVVS
197 DTVDE
198 PCLK
199 HSYNC
200 SSVSS
201 SSVDD
202 DVSS
203 DVDD
204 PVSSA
205 PVDDA
206 SOGIN1
207 SOGIN0
208 FILT

Pin Description

This section provides a detailed description of each pin for the TW8811. The pins are arranged in functional groups according to their associated interface.

The active state of the signal is determined by the trailing symbol at the end of the signal name. A "#" symbol indicates that the signal is active or asserted at a low voltage level. When "#" is not present after the signal name, the signal is active at the high voltage level.

The pin description also includes the buffer direction and type used for that pin.

PIN#	I/O	Pin Name	Description
1	P	VDDA	A/D Power +1.8V
2	I	RIN1	Analog Red input 1
3	P	VSSAR	Analog Ground for R-channel
4	I	RIN0	Analog Red input 0
5	I	REFT	RGB A/D Voltage Reference Top
6	I	REFB	RGB A/D Voltage Reference Bottom
7	I	GIN1	Analog Green input 1
8	P	VSSAG	Analog Ground for G-channel
9	I	GIN0	Analog Green input 0
10	I	BIN1	Analog Blue input 1
11	P	VSSAB	Analog Ground for B-channel
12	I	BIN0	Analog Blue input 0
13	P	VSSA	Analog Ground
14	P	VDDA	Analog Power +1.8V
15	I	VIN	Analog component V input
16	O	YOUT	Y output (Y out or Y+C out)
17	I	YIN3	Analog composite or luma input 3
18	I	YIN2	Analog composite or luma input 2
19	I	YIN1	Analog composite or luma input 1
20	I	YIN0	Analog composite or luma input 0
21	P	VSSAY	Video A/D Ground
22	I	CIN0	Analog component C input 0
23	I	CIN1	Analog component C input 1
24	P	VSSA	Analog Ground
25	P	DAVDD	DAC Analog Power +3.3V
26	P	DAVDD	DAC Analog Power +3.3V
27	O	ROUT	DAC Analog Red data output
28	O	GOUT	DAC Analog Green data output
29	O	BOUT	DAC Analog Blue data output
30	I	SEN0	Analog Sensing 0 input / CCFL or LED current sensing
31	I	SEN1	Analog Sensing 1 input / CCFL or LED voltage sensing
32	P	DAVSS	DAC Analog Ground

PIN#	I/O	Pin Name	Description
33	P	DAVSS	DAC Analog Ground
34	I	XTAL27I	Crystal terminal (if crystal is used)
35	O	XTAL27O	Crystal terminal (if crystal is used) or oscillator input
36	I	VSYNC	Vertical Sync Input
37	I/O	GPIO[0]	General Purpose Input/Output or IRQ output
38	I/O	GPIO[1]	General Purpose Input/Output
39	P	VDDO	Digital I/O Power +3.3V
40	O	FPBIAS / CCFLP	Power on/off control for panel backlight bias / CCFL Driver Polarity (Positive)
41	O	FPPWC	Power on/off control for flat panel display
42	O	FPPWM / CCFLN	PWM control for panel backlight / CCFL Driver Polarity (Negative)
43	O	PWM2	PWM control2
44	P	VSS	Digital Core Ground
45	P	VDD	Digital Core Power +1.8V
46	I	VSSO	Digital I/O Ground
47	O	TCLRL	Left Right selection (Left : high, Right : low)
48	O	TRCLK	TCON - Row Driver Shift Clock
49	O	TRUDL	TCON - Up Down selection (Up : high, Down : low)
50	O	TCINV / TCREV	TCON - Column Driver Inversion / Column Driver Reverse
51	O	TCPOLP	TCON - Column Driver Polarity (Positive) - Sharp : REVC
52	O	TCPOLN	TCON - Column Driver Polarity (Negative) ** Only use some companies Sharp : REVV TMD : TCPOLN
53	O	TCLP	TCON - Column Driver Load Pulse
54	O	FPCLK / TCCLK	TCON - Flat Panel Clock Output / Column Driver Clock
55	P	VDDO	Digital I/O Power +3.3V
56	O	FPVS / TRSPT	Flat Panel VSYNC / TCON - Row Driver Starting Pulse (Top Start)
57	O	FPHS / TCSPL	Flat Panel HSYNC / TCON - Column Driver Start Pulse (Left to right scan)
58	O	FPDE / TROE	Flat Panel Data Enable / TCON - Row Driver Output Enable
59	O	TCSPR	TCON - Column Driver Start Pulse (Right to left scan)
60	O	TRSPB	TCON - Row Driver Starting Pulse (Bottom Start)
61	P	VSS	Digital Core Ground
62	P	VDD	Digital Core Power +1.8V
63	P	VSSO	Digital I/O Ground
64	O	FPR[0]	Red Flat Panel Output bits
65	O	FPR[1]	Red Flat Panel Output bits
66	O	FPR[2]	Red Flat Panel Output bits
67	O	FPR[3]	Red Flat Panel Output bits
68	O	FPR[4]	Red Flat Panel Output bits
69	O	FPR[5]	Red Flat Panel Output bits
70	O	FPR[6]	Red Flat Panel Output bits
71	O	FPR[7]	Red Flat Panel Output bits
72	P	VDDO	Digital I/O Power +3.3V

PIN#	I/O	Pin Name	Description
73	O	FPG[0]	Green Flat Panel Outputs bit
74	O	FPG[1]	Green Flat Panel Outputs bit
75	O	FPG[2]	Green Flat Panel Outputs bit
76	O	FPG[3]	Green Flat Panel Outputs bit
77	O	FPG[4]	Green Flat Panel Outputs bit
78	O	FPG[5]	Green Flat Panel Outputs bit
79	O	FPG[6]	Green Flat Panel Outputs bit
80	O	FPG[7]	Green Flat Panel Outputs bit
81	P	VSSO	Digital I/O Ground
82	O	FPB[0]	Blue Flat Panel Outputs bit
83	O	FPB[1]	Blue Flat Panel Outputs bit
84	O	FPB[2]	Blue Flat Panel Outputs bit
85	O	FPB[3]	Blue Flat Panel Outputs bit
86	O	FPB[4]	Blue Flat Panel Outputs bit
87	O	FPB[5]	Blue Flat Panel Outputs bit
88	O	FPB[6]	Blue Flat Panel Outputs bit
89	O	FPB[7]	Blue Flat Panel Outputs bit
90	P	VSS	Digital Core Ground
91	P	VDD	Digital Core Power +1.8V
92	P	VDDO	Digital I/O Power +3.3V
93	O	MADR4	SDRAM Interface memory address bit
94	O	MADR5	SDRAM Interface memory address bit
95	O	MADR6	SDRAM Interface memory address bit
96	O	MADR7	SDRAM Interface memory address bit
97	O	MADR8	SDRAM Interface memory address bit
98	O	MADR9	SDRAM Interface memory address bit
99	O	MADR11	SDRAM Interface memory address bit
100	O	MCLK0	Clock output for external SDRAM.
101	O	MDQM1	SDRAM Interface memory data mask
102	P	VSSO	Digital I/O Ground
103	O	MADR3	SDRAM Interface memory address bit
104	O	MADR2	SDRAM Interface memory address bit
105	O	MADR1	SDRAM Interface memory address bit
106	O	MADR0	SDRAM Interface memory address bit
107	O	MADR10	SDRAM Interface memory address bit
108	O	MBA1	SDRAM Interface memory bank address
109	O	MBA0	SDRAM Interface memory bank address
110	O	MCSN	SDRAM Interface memory chip select, low active
111	P	VDDO	Digital I/O Power +3.3V
112	O	MRASN	SDRAM Interface memory row address strobe, low active
113	O	MCASN	SDRAM Interface memory column address strobe, low active
114	O	MWEN	SDRAM Interface memory write enable
115	O	MDQM0	SDRAM Interface memory data mask

PIN#	I/O	Pin Name	Description
116	I/O	MDATA7	SDRAM Interface memory data bit
117	I/O	MDATA6	SDRAM Interface memory data bit
118	I/O	MDATA5	SDRAM Interface memory data bit
119	I/O	MDATA4	SDRAM Interface memory data bit
120	P	VSS	Digital Core Ground
121	P	VDD	Digital Core Power +1.8V
122	P	VSSO	Digital I/O Ground
123	I/O	MDATA3	SDRAM Interface memory data bit
124	I/O	MDATA2	SDRAM Interface memory data bit
125	I/O	MDATA1	SDRAM Interface memory data bit
126	I/O	MDATA0	SDRAM Interface memory data bit
127	I/O	MDATA8	SDRAM Interface memory data bit
128	I/O	MDATA9	SDRAM Interface memory data bit
129	I/O	MDATA10	SDRAM Interface memory data bit
130	I/O	MDATA11	SDRAM Interface memory data bit
131	P	VDDO	Digital I/O Power +3.3V
132	I/O	MDATA12	SDRAM Interface memory data bit
133	I/O	MDATA13	SDRAM Interface memory data bit
134	I/O	MDATA14	SDRAM Interface memory data bit
135	I/O	MDATA15	SDRAM Interface memory data bit
136	P	VSSO	Digital I/O Ground
137	I	HAD0 / EODIG0	Host Interface address data / External OSD G Data Input
138	I	HAD1 / EODIG1	Host Interface address data / External OSD G Data Input
139	I	HAD2 / EODIG2	Host Interface address data / External OSD G Data Input
140	I	HAD3 / EODIG3	Host Interface address data / External OSD G Data Input
141	I	HAD4 / EODIG4	Host Interface address data / External OSD G Data Input
142	P	VSS	Digital Core Ground
143	P	VDD	Digital Core Power +1.8V
144	P	VDDO	Digital I/O Power +3.3V
145	I	HAD5 / EODIG5	Host Interface address data / External OSD G Data Input
146	I	HAD6 / EODIB0	Host Interface address data / External OSD B Data Input
147	I	HAD7/ EODIB1	Host Interface address data / External OSD B Data Input
148	I	HRDL / EODIB2	Host Interface read indicate signal / External OSD B Data Input
149	I	HWRL / EODIB3	Host Interface write indicate signal / External OSD B Data Input
150	I	HALE / EODIB4	Host Interface address latch enable signal / External OSD B Data Input
151	I	EODIB5	External OSD B Data Input
152	I	DMAREQ / EODEN	DMA Request Signal / External OSD Data Enable
153	O	DMAACK / EOVS	DMA Acknowledge Signal / External OSD Vertical Sync Signal
154	O	HWAITL / EOHS	Host Interface Wait Signal / External OSD Horizontal Sync Signal
155	I	EODAP	External OSD Alpha Blending Control Signal
156	O	HCS / EOCLK	Host Interface chip select signal / External OSD clock
157	I	HOST	Host Interface mode selection

PIN#	I/O	Pin Name	Description
158	I	TEST	Chip test mode selection
159	I	MC_SIAD	2-wire Microprocessor interface address pin
160	I/O	MC_SDA	2-wire Microprocessor interface data pin
161	I	MC_SCLK	2-wire Microprocessor interface clock pin
162	I	RESETN	Reset Pin
163	P	VSS	Digital Core Ground
164	P	VDD	Digital Core Power +1.8V
165	P	VSSO	Digital I/O Ground
166	I	DTVD[0] / EODIR0	Digital input, Cr/ B External OSD R Data Input
167	I	DTVD[1] / EODIR1	Digital input, Cr/ B. External OSD R Data Input
168	I	DTVD[2] / EODIR2	Digital input, Cr/ B External OSD R Data Input
169	I	DTVD[3] / EODIR3	Digital input, Cr/ B External OSD R Data Input
170	I	DTVD[4] / EODIR4	Digital input, Cr/ B External OSD R Data Input
171	I	DTVD[5] / EODIR5	Digital input, Cr/ B External OSD R Data Input
172	I	DTVD[6]	Digital input, Cr/ B
173	I	DTVD[7]	Digital input, Cr/ B
174	I	DTVD[8]	Digital input, Cb/ G
175	I	DTVD[9]	Digital input, Cb/ G
176	I	DTVD[10]	Digital input, Cb/ G
177	I	DTVD[11]	Digital input, Cb/ G
178	P	VDDO	Digital I/O Power +3.3V
179	I	DTVD[12]	Digital input, Cb/ G
180	I	DTVD[13]	Digital input, Cb/ G
181	I	DTVD[14]	Digital input, Cb/ G
182	I	DTVD[15]	Digital input, Cb/ G
183	P	VSS	Digital Core Ground
184	P	VDD	Digital Core Power +1.8V
185	I	DTVD[16]	Digital input, Y/ R
186	I	DTVD[17]	Digital input, Y/ R
187	I	DTVD[18]	Digital input, Y/ R
188	I	DTVD[19]	Digital input, Y/ R
189	I	DTVD[20]	Digital input, Y/ R
190	I	DTVD[21]	Digital input, Y/ R
191	I	DTVD[22]	Digital input, Y/ R
192	I	DTVD[23]	Digital input, Y/ R
193	P	VSSO	Digital I/O Ground
194	I	DTVCLK	Clock input for DTV interface
195	I	DTVHS	Horizontal sync for DTV interface

PIN#	I/O	Pin Name	Description
196	I	DTVVS	Vertical sync for DTV interface
197	O	DTVDE	Data valid for DTV interface or raw HSYNC for DTV interface (Set by register 0xF6 bit #1)
198	I/O	PCLK	Input : external clock for Panel Clock PLL test (test mode only) Output : Panel clock PLL output
199	I	HSYNC	Digital HSYNC Input
200	P	SSVSS	SS-PLL Analog Ground
201	P	SSVDD	SS-PLL Analog Power +1.8V
202	P	DVSS	Analog Ground for Low Voltage analog Power (DVDD)
203	P	DVDD	Low Voltage Analog Power +1.8V
204	P	PVSSA	PLL(Internal Analog) Ground
205	P	PVDDA	PLL (Internal Analog) Power +1.8V
206	I	SOGIN1	Sync On Green input 1
207	I	SOGIN0	Sync On Green input 0
208	I	FILT	Filter input

Parametric Information

AC/DC Electrical Parameters

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
DAVDD (measured to DAVSS) 3.3V	V_{DDAEM}	-	-	3.6	V
VDDA (measured to VSSA) 1.8V	V_{DDAM}	-	-	1.92	V
VDD (measured to VSS)	V_{DDM}	-	-	1.98	V
VDDO (measured to VSSO)	V_{DDEM}	-	-	3.6	V
Voltage on any digital signal pin (See the note below)	-	VSSO – 0.5	-	V_{DDEM} + 0.5	V
Analog Input Voltage (supplied by 1.8V)	-	VSSA – 0.5	-	1.92	V
Analog Input Voltage (supplied by 3.3V)	-	DAVSS - 0.5		3.6	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Vapor Phase Soldering(15 Seconds)	T_{VSOL}	-	-	+220	°C

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in Table 4 can induce destructive latch-up.

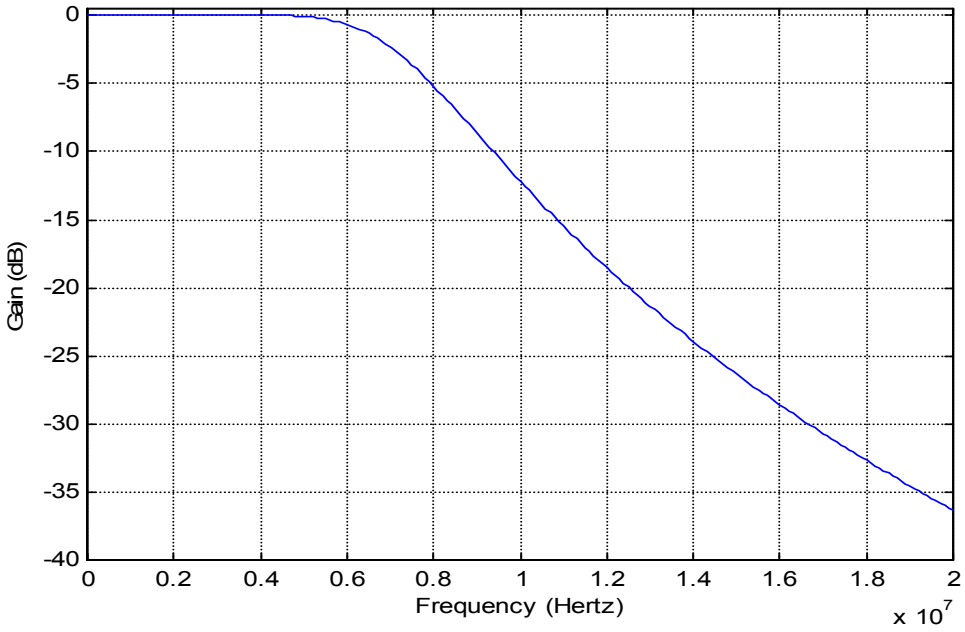
Table 5. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Supply					
Power Supply — IO	V_{DDE}	3.15	3.3	3.6	V
Power Supply — Digital	V_{DD}	1.62	1.8	1.98	V
Power Supply — Analog 3.3V	V_{DDAE}	3.15	3.3	3.6	V
Power Supply — Analog	V_{DDA}	1.62	1.8	1.92	V
Ambient Operating Temperature	T_A	-40		+85	°C
Analog Supply current (CVBS only)	Iaa	-	TBD	-	mA
(S-video)		-	TBD	-	mA
Digital I/O Supply current	Idde	-	TBD	-	mA
Digital Core Supply Current	Idd	-	TBD	-	mA
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DDE} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	μA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	μA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF

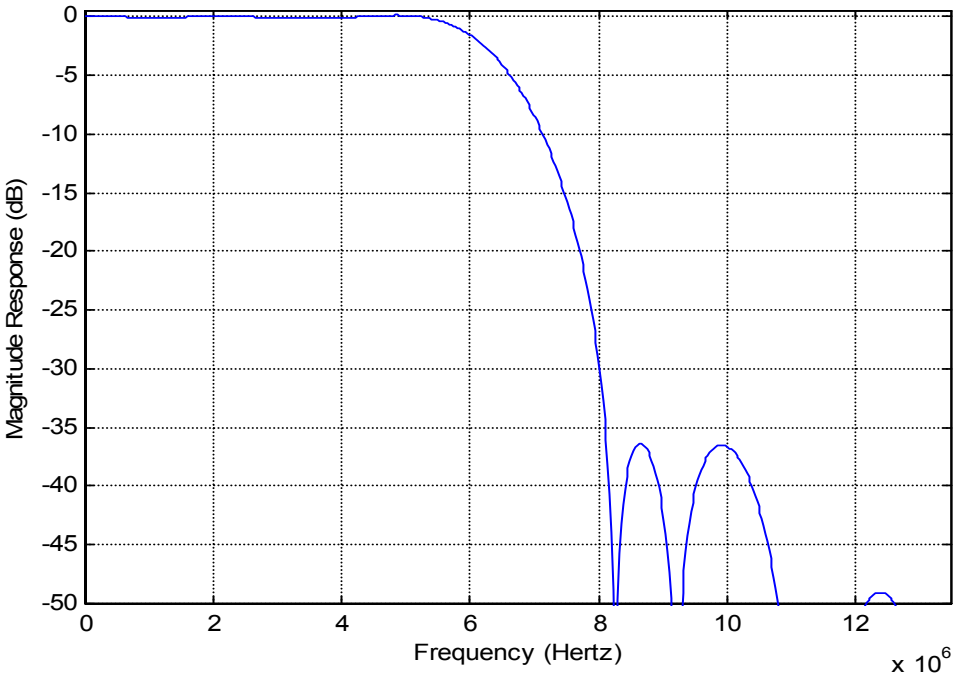
Parameter	Symbol	Min	Typ	Max	Units
Digital Outputs					
Output High Voltage (I_{OH} = –4mA)	V_{OH}	2.4	-	V_{DDE}	V
Output Low Voltage (I_{OL} = 4mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	μA
Output Capacitance	C_O	-	5	-	pF
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
YIN0, YIN1 , YIN2 and YIN3 Input Range (AC coupling required)		0.5	1.0	2.0	Vpp
CIN0, CIN1 Amplitude Range (AC coupling required)		0.5	1.0	2.0	Vpp
VIN Amplitude Range (AC coupling required)		0.5	1.0	2.0	Vpp
SEN0, SEN1 DC Input Range		0.65	1.65	2.65	V
Analog Pin Input Capacitance	C_A	-	7	-	pF
ADCs					
ADC resolution	ADCR	-	9	-	Bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	27	60	MHz
Video bandwidth (-3db)	BW	-	10	-	MHz
Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
Subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
Subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
Subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
Subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±450	-	-	Hz
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
Deviation		-	-	±50	ppm
Load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm

Filter Curves

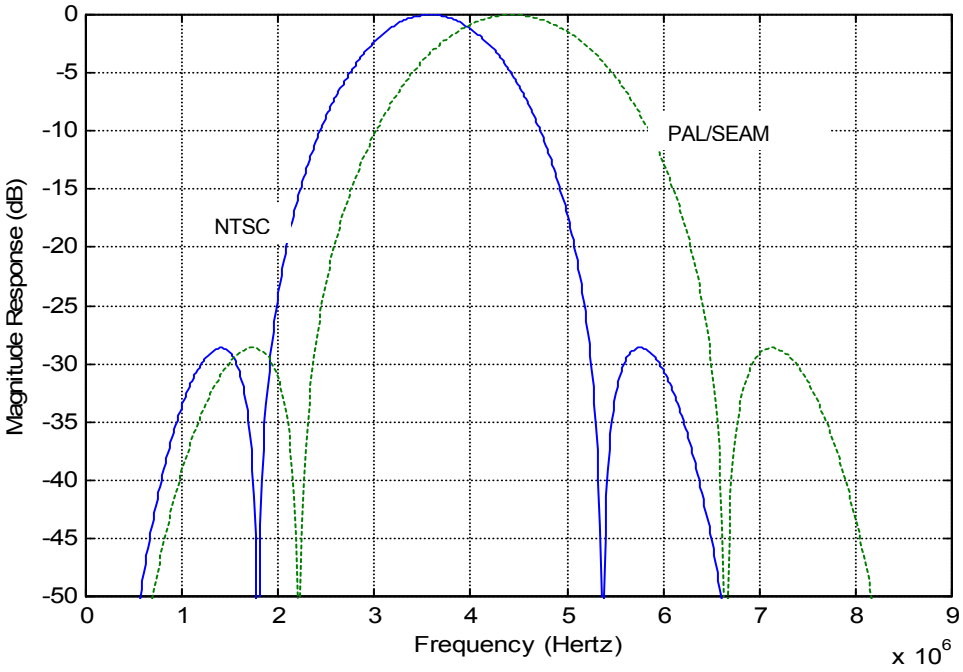
Anti-alias filter



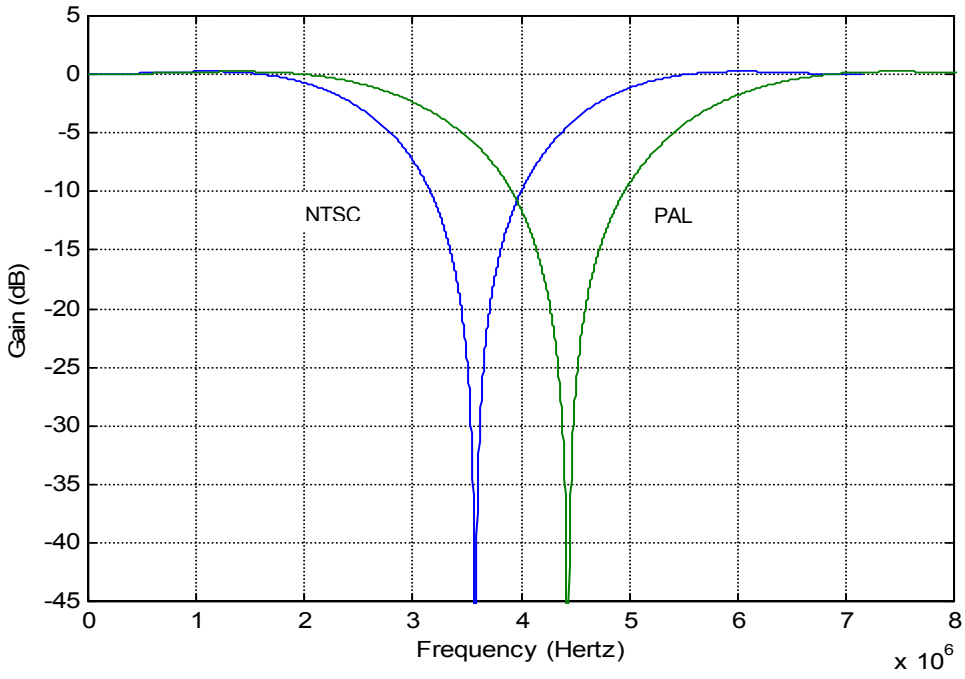
Decimation filter



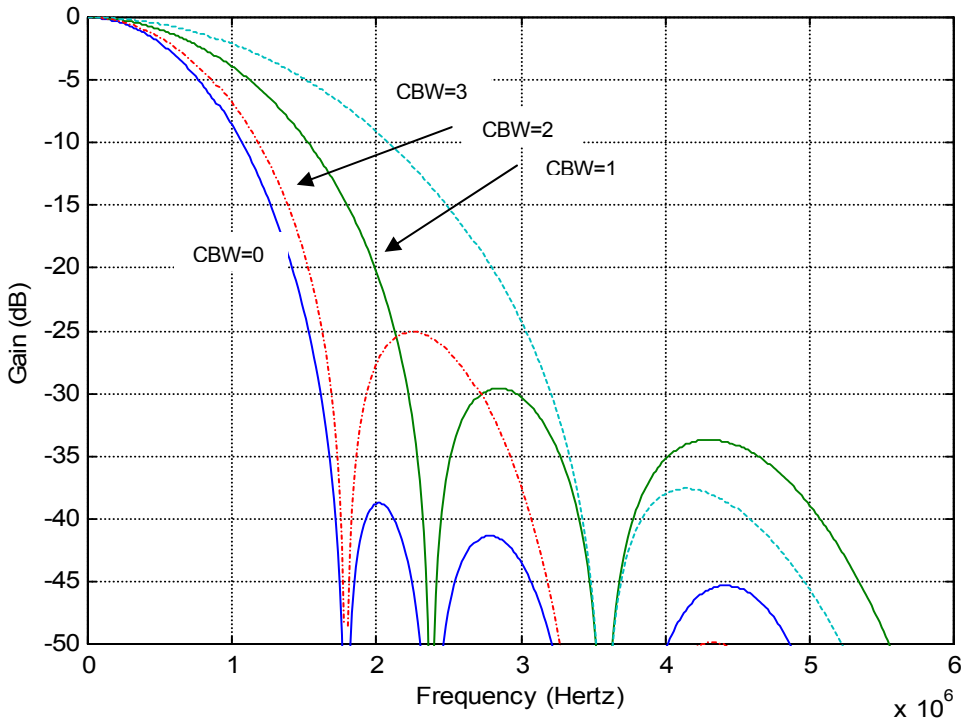
Chroma Band Pass Filter Curves



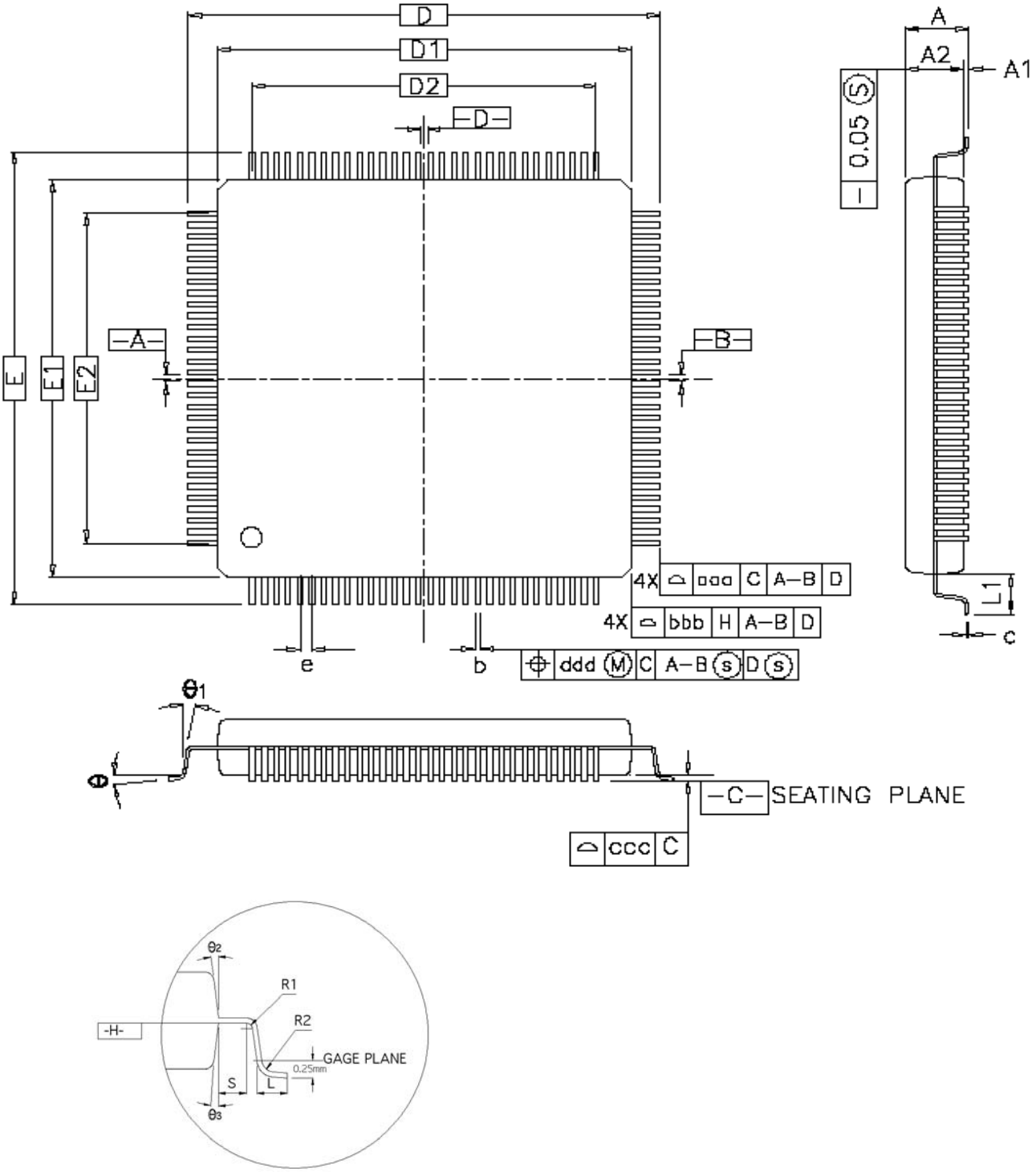
Luma Notch Filter Curve for NTSC and PAL



Chrominance Low-Pass Filter Curve



Mechanical Data 208 QFP



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	4.10	---	---	0.161
A1	0.25	---	---	0.010	---	---
A2	3.15	3.32	3.60	0.124	0.131	0.142
D	30.60 BSC.			1.205 BSC.		
D1	28.00 BSC.			1.102 BSC.		
E	30.60 BSC.			1.205 BSC.		
E1	28.00 BSC.			1.102 BSC.		
R2	0.08	---	0.25	0.003	---	0.010
R1	0.08	---	---	0.003	---	---
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	---	---	0°	---	---
θ2	8° REF			8° REF		
θ3	8° REF			8° REF		
c	0.09	0.15	0.20	0.004	0.006	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.30 REF			0.051 REF		
S	0.20	---	---	0.008	---	---
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	---	0.08	---	---	0.003	---
ddd	---	0.08	---	---	0.003	---

CONTROL DIMENSIONS ARE IN MILLMETERS.

NOTES:

1. Dimensions D1 and E1 do not include mold protrusion.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.
   Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and a adjacent lead is 0.07mm.
   The top package body size may be smaller than the bottom package body size.

TW8811 Register Summary

The registers are organized in functional groups in this Register Summary. A register containing different functional bits may appear more than once in different functional groups. If a particular bit of a register is not related to that functional group, it is printed in smaller font than those related. For example, bit 7 of index 006 is classified as "General" and is printed in normal size; the other bits in this register are printed in smaller size for their functionality is not classified as "General".

General (Common for any page)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0x0FF 0x1FF 0x2FF 0x3FF	*	*	*	*	*	*	PAGE[1:0]		00h

TOTAL PAGES : 4 (0 to 3)

PAGE #	Register Group
#0	Decoder / 3D Com / NR Control / Hi Speed ADC / Internal Test
#1	OSD / VBI Interrupt / Font OSD / Host IF / DMA / Gamma
#2	Input Ctrl / Input Measure / Scaling / Image / Display / Power Mgm / Memory Ctrl / Pip / Mpip
#3	TCON / Others

=== PAGE 0 : Decoder/3D Com/Hadc ===

Decoder

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
000	ID					REV			28h
001	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	*	MONO	DET50	-
002	YSEL2	FC27	IFSEL		YSEL		CSEL	*	40h
003	*								20h
004	*	CKHY		*					00h
005	*								AFh
006	SRESET	*	FBP	AGC_EN	CLKPDN	Y_PDN	C_PDN	V_PDN	00h
007	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02h
008	VDELAY_LO								12h
009	VACTIVE_LO								F0h
00A	HDELAY_LO								0Ch
00B	HACTIVE_LO								D0h
00C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CCh
00D	*	*	*	*					15h
00E	*	*	*						-
00F	*								-
010	BRIGHTNESS								00h
011	CONTRAST								60h
012	SCURVE	VSF	CTI		SHARPNESS				51h
013	SAT_U								80h
014	SAT_V								80h
015	HUE								00h
016	-				-				-
017	SHCOR				*	VSHP			80h
018	CTCOR		CCOR		VCOR		CIF		44h
019	*								-
01A	*	EDS_EN	CC_EN	PARITY	FF_OVF	FF_EMP	CC_EDS	LO_HI	
01B	CC_DATA								
01C	DTSTUS	STDNOW			ATREG	STANDARD			07h
01D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSC	7Fh
01E	*	CVSTD			CVFMT				08h
01F	TEST								00h

Decoder

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
020	CLPEND				CLPST				50h
021	NMGAIN				WPGAIN			AGCGAIN	42h
022	AGCGAIN								F0h
023	PEAKWT								D8h
024	CLMPLD	CLMPL							BCh
025	SYNCTD	SYNCT							B8h
026	MISSCNT				HSWIN				44h
027	PCLAMP								2Ah
028	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00h
029	BSHT			VSHT					00h
02A	CKILLMAX		CKILLMIN						78h
02B	HTL				VTL				44h
02C	CKLM	YDLY			HFLT				30h
02D	HPLC	EVCNT	PALC	SDET	TBC_EN	BYPASS	SYOUT	HADV	14h
02E	HPM		ACCT		SPM		CBVV		A5h
02F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0h
030	SID_FAIL	PID_FAIL	FSC_FAIL	SLOCK_FAIL	CSBAD	MVCSN	CSTRIPE	CTYPE	-
031	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	-
032	HFREF/GVAL/PHERRDO/CGAINO/BAMPO/MINAVG/SYTHRD/SYAMP								-
033	FRM		YNR		CLMP		PSP		05h
034	Index		NSEN/SSEN/PSEN/WKTH						1Ah
035	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	00h

RGB/YPbPr (Analog)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
036	-								00h
037	-								00h
038	-							SY_C	00h
039	-								
03A	-								
03B	-								
03C	-								
03D	-								
03E	-								
03F	FBSTUS				-	-	-		0h

LCDC – 3D Comb/NR Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
060	MD_TH								08h
061	*								50h
062	3DEN	MIXMD1	MIXMD2	*	*	TEST3D	TM_3D		00h
063	*								80h
064	*								53h
065	MSTRETCH								4Ch
066	*								4Bh
067	TESTNR	NREN	NRGAIN		NRLEVEL				14h
068	NONSTD	*	*	*	*	NS_LNUM	NS_LLEN	NS_FLEN	07h
069	NSTH1								04h
06A	NSTH2								03h
06B	NSON				NSOFF				C1h
06C	*								00h
06D	*								98h
06E	*	*	*	*	*	*	*	*	00h
06F	*	*	*	*	*	*	*	*	00h

Internal Test

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0C0	COUNTER_READ_BYTE_0								00h
0C1	COUNTER_READ_BYTE_1								00h
0C2	COUNTER_READ_BYTE_2								00h
0C3	COUNTER_READ_BYTE_3								00h
0C4	PCCINIA_INDEX				FRC_2F	FRC_1F	PCCINIA_SUB_INDX		00h
0C5	PCCINID								00h
0C6	SEL_C	GRAYD	DATA_0	LDCHMA	TLMODE		ROMSFT	RAMSFT	00h
0C7	BWYMIN								-
0C8	BWYMAX								-
0C9	BWFMIN								-
0CA	BWFMAX								-
0CB	BWBTILT								-
0CC	BWWTILT								-
0CD									
0CE	TEST_MODE								00h
0CF	.	.	.	*	.	.		*	00h

=== PAGE 1 : OSD/ VBI Int. ===

LCDC – OSD I

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
100	*	*	XF_ZOOM[1:0]		*	*	YF_ZOOM[1:0]		11h
101	BC_BLINK[3:0]				FILL_COLOR[3:0]				0Ch
102	*	*	*	WC_ MODE2	WC_MODE3[1:0]		WC_MODE1[1:0]		00h
103	*	*	*	B_FILL_ EN	*	*	*	B_TRAN_ EN	00h
104	*	*	*	*	*	*	*	BT_ START	00h
105	*	*	*	BITMAP _EN	*	*	*	SOURCE _EN	00h
106	GRH_MAP_ST[7:0]								00h
107	GRH_MAP_ST[15:8]								00h
108	*	*	*	GRH_MAP_ST[20:16]					0Ah
109	GRAPHV_ST[7:0]								14h
10A	GRAPHH_ST[7:0]								20h
10B	GRAPHV_ST[11:8]				GRAPHH_ST[11:8]				03h
10C	GRAPHV_LN[7:0]								80h
10D	GRAPHH_LN[7:0]								80h
10E	GRAPHV_LN[11:8]				GRAPHH_LN[11:8]				00h
10F	B1PHV_ST[7:0]								00h
110	B1PHH_ST[7:0]								00h
111	B1PHV_ST[11:8]				B1PHH_ST[11:8]				00h
112	B1PHV_LN[7:0]								00h
113	B1PHH_LN[7:0]								00h
114	B1PHV_LN[11:8]				B1PHH_LN[11:8]				00h
115	B2PHV_ST[7:0]								00h
116	B2PHH_ST[7:0]								00h
117	B2PHV_ST[11:8]				B2PHH_ST[11:8]				00h
118	UP_DATA[7:0]								00h
119	*	*	*	*	*	*	*	GRH_EN	00h
11A	STABLE_ADD[7:0]								00h
11B	ST_EN	ST_SEL	COLOR_SEL[1:0]		TABLE_SEL[3:0]				00h
11C	COLOR_ATTRIBUTE_DATA								00h
11D	WIN_LT _SEL	*	*	COLOR _CON	*	CON_SEL[2:0]			00h
11E	COLOR_CONTROL_SELECTION								10h
11F	*	*	*	*	*	VBEND	BWEND	TWEND	-

LCDC – Reserve

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
120	*	*	LUT_SEL_WIN1	LUT_SEL_WIN0	C8T_WIN_SEL	C8T_WEN	C8T_SEL[1:0]		00h
121	C8T_ADD[7:0]								00h
122	C8T_DATA[7:0]								00h
123	*	*	*	PKT_EN	*	*	RLC_RST	RLC_BYPASS	01h
124	DAT_BIT[3:0]				CNT_BIT[3:0]				00h
125	*	*	*	*	*	*	*	GRH_EN_W1	00h
126	*	*	XF_ZOOM_W1[1:0]		*	*	YF_ZOOM_W1[1:0]		11h
127	GRH_MAP_ST_W1[7:0]								00h
128	GRH_MAP_ST_W1[15:8]								00h
129	*	*	*	GRH_MAP_ST_W1[20:16]					0Ah
12A	GRAPHV_ST_W1[7:0]								00h
12B	GRAPHH_ST_W1[7:0]								00h
12C	GRAPHV_ST_W1[11:8]				GRAPHH_ST_W1[11:8]				00h
12D	GRAPHV_LN[7:0]								00h
12E	GRAPHH_LN[7:0]								00h
12F	GRAPHV_LN[11:8]				GRAPHH_LN[11:8]				00h
130	RF_XZOOM_W0				RF_YZOOM_W0				00h
131	RF_XZOOM_W1				RF_YZOOM_W1				00h
132	*				LOGIC _SEL				00h
133	RF_LOGIC								00h
134	RF_LOGIC_C15~8								00h
135	RF_LOGIC_C7~0								00h
136	*			RF_D_W	*			RF_D_H	00h

CCFL Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
138	OVEN	OIEN	UIEN	FBEN	LOCKV	LOCKH	CCFLENB	CCFLDEN	F2h
139	LVT		LILT		LIT				ADh
13A	*	*	CCFL_LEDC_ST		LSTP				04h
13B	FPWM								80h
13C	FDIM								84h
13D	LEDC_DIG_EN	*	*	DDIM					00h
13E	PWMTOP								20h

LCDC – External OSD & Misc.

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
151	*	*	*	OSD_W_MASK	*	*	OSD_WAIT	*	1-h
152	OSD_MODE	POLARITY[2:0]			OSDDELAY[2:0]			OSD_PORTEN	80h
153	*	*	*	*	*	*	EXSYNC_SEL	EXHACT_SEL	00h
154	*	OCKTPS[2:0]			*	OSD_GAIN[2:0]			00h

155	OSD_TEST_MODE								**00h**
156	*	*	SUB_SEL[1:0]		*	*	MAIN_SEL[1:0]		**00h**
157	*	*	*	EXT_ALPHA_CON[4:0]					**00h**
158	*	*	*	DMA_W_ MASK	*	*	*	DMA_ WAIT	**00h**
159	AEOSD	EODEN_DLY[2:0]			AEO_VS-POL	AEO_HS-POL	*	RLC_ INTR	**00h**

LCDC – DMA

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1A0	*						WAIT	DMA_SEL	**02h**
1A1	XFER_CNT[15-8]								**00h**
1A2	XFER_CNT[7-0]								**00h**
1A3	MEM_ADR[20-16]								**00h**
1A4	MEM_ADR[15-8]								**00h**
1A5	MEM_ADR[7-0]								**00h**
1A6	DATA_CH								**00h**
1A7	*							RD_WR	**00h**
1A8	*					RD_MON	WR_MON	WAIT_MO N	**00h**

LCDC – Status & Interrupt

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1B0	LB_OVF	LB_UNF	V_LOS_C	H_LOS_C	VDLOS_C	V_LOSS	H_LOSS	SYNCS	**00h**
1B1	M_RDY	PWS_C	V_PRD_C	H_PRD_C	LBOUNF	VDC_C	VH_LOS_C	SYNCS_C	**00h**
1B2	IRQ_B_B17	IRQ_B_B16	IRQ_B_B15	IRQ_B_B14	IRQ_B_B13	IRQ_B_B12	IRQ_B_B11	IRQ_B_B10	**FFh**
1B3	*	*				IRQ_B_VD	IRQ_B_CC	IRQ_B_50	**07h**
1B4			P_VLOS_C	P_VLOS_C		P_VLOSS	P_HLOSS	P_SYNCS	**00h**
1B5			P_VPRD_C	P_HPRD_C			P_VHLOSC	P_SYNCSC	**00h**
1B6			M_VLOS_C	M_VLOS_C		M_VLOSS	M_HLOSS	M_SYNCS	**00h**
1B7			M_VPRD_C	M_HPRD_C			M_VHLOSC	M_SYNCS	**00h**
1B8	MEAS_SEL		IRQ_1B5_5	IRQ_1B5_4			IRQ_1B5_1	IRQ_1B5_0	**00h**
1B9			IRQ_1B7_5	IRQ_1B7_4			IRQ_1B7_1	IRQ_1B7_0	**00h**

LCDC : ADC/LLPLL

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1C0	INP_SEL		CS_INV	CS_SEL	SOG_SEL	HS_POL	HS_SEL	CK_SEL	00h
1C1	VS_POL	HS_POL	VS_DET	HS_DET	CS_DET	IN_SRC			
1C2	LLC_POST		LLC_VCO		*	LLC_IPMP			00h
1C3	*				LLC_ACKN[11:8]				03h
1C4	LLC_ACKN[7:0]								5Ah
1C5	LLC_PHA								00h
1C6	LLC_ACPL	LLC_APG			*	LLC_APZ			20h
1C7	*				LLC_ACKI[11:8]				04h
1C8	LLC_ACKI[7:0]								00h
1C9	PRE_COAST								06h
1CA	POST_COAST								06h
1CB	PUSOG	PUPLL	*	SOG_TH					30h
1CC	*			VSY_SEL	*		VSY_POLC	HSY_POLC	00h
1CE	ADC_CLK_SEL	*	DTV	*	PDA	*	INREFI	INREFI	00h
1CF	INP_SEL_ADC		SAVE						24h
1D0	*					GAINY[8]	GAINC[8]	GAINV[8]	00h
1D1	GAINY								F0h
1D2	GAINC								F0h
1D3	GAINV								F0h
1D4	RGB_MODE	*	CL_EDGE	CKLY	CKLC	Y_CL_EN	C_CL_EN	V_CL_EN	00h
1D5	CL_START								00h
1D6	CL_END								10h
1D7	CL_LOC								70h
1D8	*	LLC_DBG_SEL			CL_TEST	ADC_TEST	CL_Y_TEST	CL_UV_TEST	00h
1D9	CL_Y_VAL								10h
1DA	CL_UV_VAL								80h
1DD	OFFSETR								00h
1DE	OFFSETG								00h
1DF	OFFSETB								00h

LCDC – Gamma

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1F0	GAMAE_R	GAMAE_G	GAMAE_B	*	AUTO_INC	*	GAMMA_RGB_INDX		00h
1F1	GAMMA_RAM_STARTING_ADDR								00h
1F2							GAMMA_RAM_DATA[9:8]		00h
1F3	GAMMA_RAM_DATA[7:0]								00h

=== PAGE 2 : Image/Display/Memory ===

LCDC – Input Type

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
20e	*	*	*	*	*	*	*	DUAL_656	00h
20f	SEQRGB_LTG[1:0]		SEQRGB_ORDER[1:0]		SEQRGB_SEL8BIT[1:0]		SEQRGB_ POL	SEQRGB	00h

LCDC – Input and Input Related

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
210	OFDM	RVODDP	SLVSFLD	ECSYNC	DE_POL	HS_POL	VS_POL	DCLK_POL	00h
211	EPDEN	PDEN_POL	EXT_HA	SELDE	*	DTVCK_DELAY			20h
212	VGAFLD	SELFVS	VSDL_656	SELFTHS	CR601	INPUT_DATA_BUS_ROUTING			04h
213	INTERNAL_CLK_POL							yuv_rgb_hs RGB	01h
214	COAST_RANGE		VGA_INP	B8601	COMP	yuv_rgb	IP_SEL		28h
215	OFD_DET_END				OFD_DET_ST				54h
216	CSYNC_VS_OFFSET								20h
217	IP_HA_ST_LO								00h
218	IP_HA_END_LO								CFh
219	IP_HA_END_HI				*	IP_HA_ST_HI			20h
21A	IP_VA_ST_ODD_LO								13h
21B	IP_VA_ST_EVN_LO								13h
21C	IP_VA_LENGTH_LO								00h
21D	*	IP_VA_LENGTH_HI			IP_VA_ST_EVN_HI		IP_VA_ST_ODD_LO		30h
21E	HSCKTPS 2[2]	GPIOEN2	GPIOEN1	GPIOEN0	IRQ_AL	*	HSCKTPS2[1:0]		00h
21F	GPIO1_P	GPIO1_SRC		GPIO1_D	GPIO0_P	GPIO0_SRC		GPIO0_D	00h

LCDC – Input Measurement

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
220	*								
221	MEA_WIN_H_ST_LO								20h
222	MEA_WIN_H_END_LO								FFh
223	MEA_WIN_H_END_HI				*	MEA_WIN_H_ST_HI			10h
224	MEA_WIN_V_ST_LO								20h
225	MEA_WIN_V_END_LO								FAh
226	*	MEA_WIN_V_END_HI			*	MEA_WIN_V_ST_HI			00h
227	RESULT_0								-
228	RESULT_1								-
229	RESULT_2								-
22A	RESULT_3								-
22B	RESULT_SEL				FIELD_SEL		RD_LOCK	STARTM	00h
22C	U_27M	NOISE_MASK			ERR_TOLER			ENDET	00h
22D	THRESHOLD_FOR_ACT_DET				ENALU	NOFSEL		DE_MEA	30h
22E									
22F									

LCDC - Scaling

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
230	X_SCALE_UP_MID								B4h
231	X_SCALE_DOWN_LO								80h
232	Y_SCALE_UP/DOWN_MID								50h
233	PANORA_MA	LNDB	PXDB	ZOOMBP	Y_SCALE_UP/ DOWN_HI		X_SCALE_DOWN_HI	X_SCALE_UP_HI	00h
234	X_OFFSET								00h
235	Y_ODD_OFFSET								80h
236	H_NON_DISPLAY_PIXEL / H_PANORAMA_PIXEL								00h
237	LB_CE	*	*	*	*	*	H_NON_DISPLAY / H_PANORMAN_PIXEL		00h
238	X_SCALE_UP_LO (AT_THE_SIDE_FOR_PANORAMA)								00h
239	X_SCALE_UP_LO								00h
23A	Y_SCALE_UP_LO								00h
23B	Y_EVEN_OFFSET								00h
23C									
23D									
23E									
23F									

LCDC – Image Adjustment

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
240	*	INDX_CB	HUE						20h
241	CONTRAST_R / CONTRAST_Y								80h
242	CONTRAST_G / CONTRAST_Cb								80h
243	CONTRAST_B / CONTRAST_Cr								80h
244	BRIGHTNESS_R / BRIGHTNESS_Y								80h
245	BRIGHTNESS_G								80h
246	BRIGHTNESS_B								80h
247	H_SHARP_COR				H_SHARPNESS				3Fh
248	H_SHARP_FREQ	*	DYNR		*	HFLT			00h
249		INDX_CB2	HUE2						20h
24A	CONTRAST_R2 / CONTRAST_Y2								80h
24B	CONTRAST_G2 / CONTRAST_Cb2								80h
24C	CONTRAST_B2 / CONTRAST_Cr2								80h
24D	BRIGHTNESS_R2 / BRIGHTNESS_Y2								80h
24E	BRIGHTNESS_G2								80h
24F	BRIGHTNESS_B2								80h
250	H_SHARP_COR2				H_SHARPNESS2				3Fh
251	H_SHARP_FREQ2	*	DYNR2		*	HFLT2			00h
252	V_SHARP_A	V_SHARP_B			DIS_EDG	INDEX_FOR_07A			00h
253	EDGE_ENHANCEMENT_THRESHOLD_REG_0/1/2/3/4								-
254	*	*			RSV				04h
255	T_BW	*	PEDLVL	WHTLVL	*	*	BPBW	*	1Ch
256	BW_LINE_ST_LO								08h
257	BW_LINE_END_LO								F6h
258	*				BW_LINE_END_HI		BW_LINE_ST_HI		08h
259	BW_H_DELAY								10h
25A	*	BW_H_FILTER_GAIN							0Dh
25B	BW_BLACK_TILT								67h
25C	BW_WHITE_TILT								94h
25D	BW_BLACK_GAIN								2Ah
25E	BW_WHITE_GAIN								D0h
25F	PDOF_EN	PIP_DN_OFF*							CAh
260	*	BW_GAIN							02h
261	HRED_EN	MPIP_H_REDUCTION							00h
262	*	*							18h
263	CE_CENTER0								3Dh
264	CE_CENTER1								C3h
265	CE_CENTER2								FCh
266	CE_EN	CE_SPREAD0	CE_GAIN0						00h
267	*	CE_SPREAD1	CE_GAIN1						00h
268	*	CE_SPREAD2	CE_GAIN2						00h
269	*								00h
26A	*	*	*	*					00h
26B	*	*							00h

LCDC – Display Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
270	DBLOP	FPDEAH	FPHSAH	FPVSAH	RVFPCK	RVHILO	RVBIT	FPCLKC	40h
271	TCONS	USEREG	DEMODE	OP6B	TRIFP	FPCLK_DELAY			00h
272	FPHS_PERIOD_LO								3Ah
273	FPHS_ACTIVE_PW								10h
274	FP_H_BACK_PORCH								1Bh
275	FPDE_ACTIVE_LO								00h
276	FPDE_ACTIVE_HI				FPHS_PERIOD_HI				45h
277	FPVS_PERIOD_LO								26h
278	FPVS_ACTIVE_PW								06h
279	FP_V_BACK_PORCH								1Fh
27A	FP_V_ACTIVE_LO								00h
27B	EARLY_ST	FP_V_ACTIVE_HI			*	FPVS_PERIOD_HI			33h
27C	*	DITHER_OPTION			*	DITHER_FORMAT			00h
27D	VSYNC_DELAY								08h
27E	FRCLONG	FRCSHRT	EPWMX	PWM_AL	VH_DISHA	FRERUN	AUTOC	SDELVS	00h
27F	DISP_SNGFLD		RVF_AC	TVVSF4	NOEVNI	EVNDLY			00h
280	INI_CNT_EVN_LO								00h
281	INI_CNT_ODD_LO								00h
282	INI_CNT_EVN_HI				INI_CNT_ODD_HI				00h
283	EVNPM	NUMBER_OF_LINES_TO_BLACK_OUT							00h
284	PWMC_D2	PWM_COUNTER							40h
285									
286									
287	DUAL_SELH								
289									

LCDC – Memory Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
2A0	RD_PH	MCLKOSEL			**NOMCST**	TESTEN	BCONFIG		A2h
2A1	TAFRSH								07h
2A2	RASMAX								20h
2A3	TRP				TRCD				22h
2A4	AD21	*	*	*	TRFC				07h
2A5	*	RDLTNC			TMINC				43h
2A6	*	*	CYCDEL		*	CASLTNC			13h
2A7	*	*	*	*	*	*	*		40h
2A8									
2A9									
2AA									
2AB									
2AC									
2AD									
2AE	PIP_H_POS_ADJ								20h
2AF	PIP_V_POS_ADJ								2Ch

LCDC – PIP/MPIP Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
2B0	PIPGW_XST[7:0]								10h
2B1	PIPGW_WIDTH[7:0]								60h
2B2	PPFIL_MAN	PIPGW_WIDTH[10:8]			PPFIL_SEL		PIPGW_XST[9:8]		20h
2B3	PIPGW_YST[7:0]								02h
2B4	PIPGW_HEIGHT[7:0]								E0h
2B5	PIPWHGT[8]	*	PIPEFDOFF		PIPWYST[8]	*	PIPOFDOFF		00h
2B6	PIPDNSXFAC[7:0]								00h
2B7	PIPDNSYFAC[7:0]								00h
2B8	PIPDNSYFAC[11:8]				PIPDNSXFAC[11:8]				11h
2B9	PIP_WR_BASE								00h
2BA	PIP_WR_WIDTH[7:0]								30h
2BB	PIP_WR_HEIGHT[7:0]								70h
2BC	PIPWREN	WCPH	PIPOFEN	PIPOFPH	HEIGHT[8]	*	PIP_WR_WIDTH[9:8]		01h
2BD	PRDEN	WR_PDN	PIPEN	SNGL_FD	PFPPOL	PXDB	*	BLACK	00h
2BE	PUPSXFAC[7:0]								00h
2BF	PUPSYFAC[7:0]								00h
2C0	PUPSYFAC[11:8]				PUPSXFAC[11:8]				88h
2C1	PIPWBASEX[7:0]								80h
2C2	PIPWBASEY[7:0]								80h
2C3	CK_INV	PIPWBASEY[10:8]			PIPWBASEX[11:8]				12h
2C4	PIPWYOFF				PIPWXOFF				2Ch
2C5	PIPWWIDTH[7:0]								30h
2C6	PIPWHEIGHT[7:0]								E0h
2C7	PRCPH	PIPWHEIGHT[10:8]			PIPWWIDTH[11:8]				01h
2C8	MPIP_H_POS_ADJ								2Ch
2C9	MPIP_V_POS_ADJ								2Eh
2CA	MPIPGW_XST[7:0]								00h
2CB	MPIPGW_WIDTH[7:0]								00h
2CC	MPFIL_MAN	MPIPGW_WIDTH[10:8]			MPFIL_SEL		MPIPGW_XST[9:8]		00h
2CD	MPIPGW_YST[7:0]								00h
2CE	MPIPGW_HEIGHT[7:0]								00h
2CF	MPIPWHGT[8]	*	MPIPEFDOFF		MPIPWYST[8]	*	MPIPOFDOFF		00h

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
2D0	MPIPDNSXFAC[7:0]								00h
2D1	MPIPDNSYFAC[7:0]								00h
2D2	MPIPDNSYFAC[11:8]				MPIPDNSXFAC[11:8]				11h
2D3	MPIP_WR_BASE								00h
2D4	MPIP_WR_WIDTH[7:0]								00h
2D5	MPIP_WR_HEIGHT[7:0]								00h
2D6	MPWREN	WCPH	MPOFEN	MPOFPH	HEIGHT[8]	*	MPIP_WR_WIDTH[9:8]		00h
2D7	MPRDEN	WR_PDN	MPIPEN	*	MPFPPOL	PXDB	*	BLACK	00h
2D8	PUPSXFAC[7:0]								00h
2D9	PUPSYFAC[7:0]								00h
2DA	PUPSYFAC[11:8]				PUPSXFAC[11:8]				88h
2DB	PIPWBASEX[7:0]								20h
2DC	PIPWBASEY[7:0]								2Ch
2DD	PIPVUPS_OFF*								80h
2DE	PIPWYOFF				PIPWXOFF				00h
2DF	PIPWWIDTH[7:0]								00h
2E0	PIPWHEIGHT[7:0]								00h
2E1	CK_INV	PIPWHEIGHT[10:8]			PIPWWIDTH[11:8]				00h
2E2	PRCPH							INIT_EN	00h
2E3	MPIPORGX[7:0]								00h
2E4	MPIPORGY[7:0]								00h
2E5	INIT_COLOR								00h
2E6	KEY_DSP			ALPHA2					10h
2E7	MPIPHIGHT [8]		MPIPWIDTH[9:8]		MPIPORGY [8]		MPIPORGX[9:8]		00h
2E8	MPIP_VSPACE[3:0]				MPIP_HSPACE[3:0]				00h
2E9	MPIP_YMAX[1:0]		MPIP_XMAX[1:0]		MPIP_WINXY1:0]		MPIP_WINX[1:0]		00h
2EA		MPIP_BORDERW[2:0]			MPIP_HLY[1:0]		MPIP_HLX[1:0]		00h
2EB	MPIP_FRMCOLOR1[7:0]								1Ch
2EC	MPIP_FRMCOLOR2[7:0]								E0h
2ED									00h
2EE		DTVDE			PIP_INMX_SEL[1:0]		MPIP_INMX_SEL[1:0]		00h
2EF	PIPAB_EN	MD565	KEY_INV	ALPHA1					00h
2F0	RKEY								00h
2F1	GKEY								00h
2F2	BKEY								00h
2F3	KEY_RANGE								00h

LCDC – Power Management

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
2F4	DIVDE_DOWN_COUNTER_MSB								00h
2F5	PCLK_PDN	clksel_fppwr	PWR_STATE		MANPWR	EDPMS	PWR_STATE_WT		00h
2F6	SUSPEND_STDBY_CNT				ON_SUSPEND_CNT				00h
2F7	OFF_STDBY_CNT				STDBY_OFF_CNT				00h
2F8	STDBY_SUSPEND_CNT				SUSPEND_ON_CNT				00h

=== PAGE 3 : TCON/ PLL ===

LCDC – TCON

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
300	SIG_OFF	TCCK_PH	ROE_EN	*				DIV_CK	20h
301	*				REV_EN	*	INV_SEL		00h
302	*				TOP_BTM		LFT_RHT		05h
303	*				ROE_P	RSP_P	CLP_P	CSP_P	0Fh
304	PGM_SHARP	SP_CTRL	PGM_RCK	PGM_ROE	PGM_RSP	PGM_POL	PGM_CLP	PGM_CSP	00h
305	*							INV_SW	00h
306							REV_SEL	ANAL_LCD	02h
30A	*		RSP_WIDTH		*		COMPANY		02h
30B	REVV_REVC								4Dh
30C	*				V_ST[11:8]				00h
30D	V_ST[7:0]								06h
30E	*				V_ED[11:8]				01h
30F	V_ED[7:0]								E2h
310					CP_SW[11:8]				02h
311	CP_SW[7:0]								D0h
312	*				CLP_ST[11:8]				02h
313	CLP_ST[7:0]								D0h
314	*				CLP_ED[11:8]				00h
315	CLP_ED[7:0]								06h
31A	*				CSP_ST[11:8]				00h
31B	CSP_ST[7:0]								C8h
31C	*				CSP_ED[11:8]				00h
31D	CSP_ED[7:0]								01h
320	*				RCK_ST[11:8]				00h
321	RCK_ST[7:0]								00h
322	*				RCK_ED[11:8]				02h
323	RCK_ED[7:0]								30h
324	*				RSP_ST[11:8]				00h
325	RSP_ST[7:0]								06h
326	*				RSP_ED[11:8]				00h
327	RSP_ED[7:0]								01h
32C	*				ROE_ST[11:8]				00h
32D	ROE_ST[7:0]								0Ah
32E	*				ROE_ED[11:8]				00h
32F	ROE_ED[7:0]								40h
334	*				SHARP_STR_H				00h
335	SHARP_STR_L								20h
336	*				SHARP_END_H				01h
337	SHARP_END_L								E2h
338	*		CLPW	CSYNC_MODE	CLPSEL		CSPSEL		00h
339	*				POL_STEP[3:0]				00h

LCDC – PLL & DAC

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
3A0	IP_P			FREQ_P[19:15]					40h
3A1	FREQ_P[14:7]								00h
3A2	FREQ_P[6:0]							*	00h
3A3	SSFREQ_P[7:0]								00h
3A4	SSG_P				VCO_P		POST_P		00h
3A5	IP_M			FREQ_M[19:15]					40h
3A6	FREQ_M[14:7]								00h
3A7	FREQ_M[6:0]							*	00h
3A8	SSFREQ_M[7:0]								00h
3A9	selpadpclk	selpadmclk	pd_p	pd_m	PllInSel	SSD			00h
3AA	SSG_M				VCO_M		POST_M		00h
3AB	*	*	*	DA_RGAIN					
3AC	*	*	*	DA_GGAIN					
3AD	*	*	*	DA_BGAIN					
3AE	DacPd	TEST_CLK_SEL		Dac_iref	*				00h
3F0			HSWID						10h
3F1									
3FF	Page_Num								00h

TW8811 Register Description

0x000 – Product ID Code Register (ID)

Bit	Function	R/W	Description	Reset
7-3	ID	R	The TW8811 Product ID code is 00101.	00101b
2-0	Revision	R	Revision number	000b

0x001 – Chip Status Register (CSTATUS)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in a number of consecutive video lines specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x002 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	YSEL[2]	R/W	MSB of YSEL. (see description below)	0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	10 = Component video decoding 01 = S-video decoding 00 = Composite video decoding	00
3-2	YSEL[1:0]	R/W	These three bits control the Y input video selection Mux. 000 : YOUT = YIN0 001 : YOUT = YIN1 010 : YOUT = YIN2 011 : YOUT = YIN3 1xx : NA	00
1	CSEL	R/W	This bit controls the C input source selection. 0 = CIN0 1 = CIN1	0
0	Reserved	R/W		0

0x003 – QCLAMP

Bit	Function	R/W	Description	Reset
7-0	QCLAMP	R/W	Reserved	20h

0x004 – CKHY

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	0
6-5	CKHY	R/W	Color killer time constant 0: fast 3: slow	0
4-0	Reserved	R/W	Reserved for test.	

0x005 – Reserved

Bit	Function	R/W	Description	Reset
7-0	SAGCGAIN	R/W		AFh

0x006 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	W	A 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6		R/W	Reserved	0
5	FBYP	R/W	1 = Anti-alias Filter Bypass 0 = Enable	0
4	AGC_ENB	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = 27 MHz clock in power down mode.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power down mode.	1
0	V_PDN	R/W	0 =V channel ADC in normal operation. 1 = V channel ADC in power down mode.	1

0x007 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	0
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	10b

0x008 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	15h

0x009 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0h

0x00A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	84h

0x00B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0h

0x00C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Color killer sensitivity. 1= low 0 = high	0
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC/PAL 0 = Notch filter	1
2	HCOMP	R/W	1 = Operation mode 1. (recommended) 0 = Operation mode 0.	1
1	YCOMB	R/W	This bit controls the Comb operation in the case of monochrome video. 1 = Comb enabled. 0 = Comb disabled.	0
0	PDLY	R/W	PAL delay line. 0 = enabled. 1 = disabled.	0

0x010 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00h

0x011 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CONTRAST	R/W	These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 1 (`100_0000`) has no effect on the video data.	60h

0x012 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	Reserved	1
5-4	CTI	R/W	Color transient improvement level control. There are 4 enhancement levels with 0 being the lowest and 3 being the highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with '15' being the strongest.	1

0x013 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h

0x014 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h

0x015 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue. They have value from +96^{o} (7Fh) to -96^{o} (80h) with an increment of 0.75^{o}. The default value is 0 (00h).	00h

0x016 – Reserved

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		C
3-0	Reserved	R/W		8

0x017 – Vertical Peaking Control I

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	3
3	Reserved		Reserved	0
2-0	VSHP	R/W	These bits control the vertical peaking level with '0' being the minimum and '7' being the maximum.	0

0x018 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring function for the CTI. It has internal step size of 2.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0h
3-2	VCOR	R/W	These bits control the coring function of the vertical peaking logic. It has an internal step size of 2.	1h
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5 dB 2 = 3 dB 3 = 6 dB (Secam)	0h

0x019 – Reserved

Bit	Name	R/W	Description	Reset
7-0	Reserved		Reserved	

0x01A – CC/EDS Status Register (CC_STATUS)

Bit	Function	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	0

0x01B – CC/EDS Data Register (CC_DATA)

Bit	Function	R/W	Description	Reset
7-0	Reserved	R	Reserved	00h

0x01C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	Standard	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	0h

0x01D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	0
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	0
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	0
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	0
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	0
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	0
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	0

0x01E – Component Video Format (CVFMT)

Bit	Name	R/W	Description	Reset
7	RSV	R	Reserved	0
6-4	CVSTD	R	Component video input format detection. 0 = 480i, 1 = 576i, 2 = 480p, 3 = 576p	0h
3-0	CVFMT	R/W	Component video format selection. 0 = 480i, 1 = 576i, 2 = 480p, 3 = 576p, 8 = Auto	8h

0x01F – Control Register

Bit	Name	R/W	Description	Reset
7-3		R	Reserved	0
2	VREF	R/W	Video ADC voltage reference control. 0=normal operation	0
1	IREF	R/W	Video ADC bias control, 0=normal operation	0
0	SAVE	R/W	Video ADC reference current control, 0=normal current, 1=2/3 of normal current	0

0x020 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0x021 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	4
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN[8]	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x022 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN[7:0]	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0h

0x023 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold.	D8h

0x024– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3Ch

0x025– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38h

0x026 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits set the size for the horizontal sync detection window.	4

0x027 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	2Ah

0x028 – Vertical Control Register

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special switching application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = long 0 = normal	0

0x029 – Vertical Control II

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control. (Reserved)	0
4-0	VSHT	R/W	Vsync output delay control in the increment of half line length (Reserved)	15h

0x02A – Color Killer Level Control

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	2
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	20h

0x02B – Comb Filter Control

Bit	Function	R/W	Description	Reset
7-4	HTL	R/W	Adaptive Comb filter combing control.	4
3-0	VTL	R/W	Adaptive Comb filter combing control.	4

0x02C – Luma Delay and HSYNC Control

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = Normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HFLT	R/W	Peaking control 2. The peaking curve is controlled by SCURVE bit.	000

0x02D – Miscellaneous Control Register I (MISC1)

Bit	Function	R/W	Description	Reset
7	HPLC	R/W	Reserved for internal use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation.	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A "1" is recommended.	1
3	TBC_EN	R/W	Reserved.	0
2	BYPASS	R/W	Debug use	1
1	SYOUT	R/W	Reserved.	0
0	HADV	R/W	Reserved.	0

0x02E – Miscellaneous Control Register II (MISC2)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 0 = slow 1 = auto1 2 = auto 3 = Fast	2
5-4	ACCT	R/W	ACC time constant 00 = No ACC 01 = slow 10 = medium 11 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. 0 = Low 1 = Medium 2 = High 3 = Extended	1

0x02F – Miscellaneous Control III (MISC3)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Bluer. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0x030 – Macrovision Detection

Bit	Function	R/W	Description	Reset
7	SID_FAIL	R	Secam status	
6	PID_FAIL	R	PAL status	
5	FSC_FAIL	R	FSC status	
4	SLOCK_FAIL	R	PLL status	
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	
2	MCVSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	
0	CTYPE2	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	

0x031 – CSTATUS III

Bit	Function	R/W	Description	Reset
7	VCR	R	1 = VCR mode	
6	WKAIR	R	1= Weak Signal 0 = Normal	
5	WKAIR1	R	Weak signal indicator.	
4	VSTD	R	1= Standard Signal 0 = non – standard signal	
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	
2	WSSDET	R	1 = WSS data detected. 0 = Not detected.	
1	EDSDET	R	1 = EDS data detected. 0 = Not detected.	
0	CCDET	R	1 = CC data detected. 0 = Not detected.	

0x032 – HFREF

Bit	Function	R/W	Description	Reset
7-0	Reserved	R	HREF[9:2] / GVAL[8:1] / PHERRDO / CGAINO / BAMPO / MINAVG / SYTHRD / SYAMP	-

0x033 – Miscellaneous Control Register

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode. 0X = Auto mode 10 = 60 Hz 11 = 50 Hz	00
5-4	YNR	R/W	Y HF Noise Reduction. 0 = None 1 = smallest 2 = small 3 = medium	00
3-2	CLMD	R/W	Clamping mode control. 00 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	01
1-0	PSP	R/W	Slice level for sync top mode. 0 = Low 1 = Medium 2 = High 3=highest	01

0x034 – NSEN/SSEN/PSEN/WKTH

Bit	Function	R/W	Description	Reset
7-6	Index	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	00
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDS = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 2A

0x035 – Clamp Cntl2

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debug use.	0
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled.	0
5	CCLEN	R/W	1 = C channel clamp disabled 0 = Enabled.	0
4	VCLEN	R/W	1 = V channel clamp disabled 0 = Enabled.	1
3	GTEST	R/W	1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control	0
1	CKLY	R/W	Clamping current control for Y.	0
0	CKLC	R/W	Clamping current control for C/V.	0

0x038 – Analog Cntl

Bit	Function	R/W	Description	Reset
7-6	Reserved			
0	SY_C	R/W	YOUT control 0 = Y 1 = Y+C	0

0x03A – 0x03E Reserved

0x03F – DAC Current Reference

Bit	Function	R/W	Description	Reset
7-4	FBSTUS	R	Reserved	-
3	SYSEL	R/W	Y(CVBS) input selection 0 = G ADC Input Selection 1 = Y ADC Input selection	0
2	FBTYP	R/W	Reserved	0
1-0	FBTHD	R/W	Reserved	00

3D Comb Control (0x060 to 0x06F)

0x060 – MDTH

Bit	Function	R/W	Description	Reset
7-0	MDTH	R/W	Motion detection Threshold (Smaller value yields more 2D)	08h

0x062 – 3D_MODE

Bit	Function	R/W	Description	Reset
7	3D_EN	R/W	1 : 3D Comb enable, 0 : Disable (2D only and no SDRAM access)	0
6	MIXMD1	R/W	1: Fixed mode (chosen by bit 5), 0 : Adaptive mode	0
5	MIXMD2	R/W	When 0x72 bit 6 is "1", this bit defines fixed mode selection 1: 2D, 0 : 3D	0
4-3	Reserved	-		00
2	TEST3D	R/W	1: 3D Comb test mode enable. Should be "0" for normal operation	0
1-0	TM_3D	R/W	3D-Comb test mode. According to the setting of these bits, vd[15:0] will output following signals. 0: Frame delay test 1 (F0 and F1), 1: Frame delay test 2 (F1 and F2), 2: Frame-combed Y and Motion test, 3: Frame-combed Y and C test	0h

0x065 – STR

Bit	Function	R/W	Description	Reset
7-0	M_STRCH	R/W	Stretch of detected motion	4Ch

0x067 – NRLEVEL

Bit	Function	R/W	Description	Reset
7	TESTNR	R/W	1: 3D-NR test mode enable. vd[15:8] will output current Y and vd[7:0] will output 1 frame delayed Y. Should be "0" for normal operation.	0
6	NR_EN	R/W	1: 3D-NR enable, 0: Disable In some mode, 3D-NR is not available with 3D-coymb. Please refer the description of "Memory controller" in the previous section for detail.	0
5-4	NRGAIN	R/W	Noise reduction correction gain 0: ¾ , 1: ½, 2: ¼, 3: 1/8	1h
3-0	NRLEVEL	R/W	Noise identification level (bigger value will correct bigger noise but may induce obvious tailing)	4h

0x068 – NSMODE

Bit	Function	R/W	Description	Reset
7	NONSTD	R	1: Non-standard signal, 0: Standard signal	
6-3	Reserved	R/W		0
2	NS_LNUM	R/W	1: Check line number per frame, 0: Ignore line number	1
1	NS_LLEN	R/W	1: Check line length error, 0: Ignore length error	1
0	NS_FLEN	R/W	1: Check frame length error, 0: Ignore frame length error	1

0x069 – NSLEVEL1

Bit	Function	R/W	Description	Reset
7-0	NSTH1	R/W	Non standard detection threshold 1	02h

0x06A – NSLEVEL2

Bit	Function	R/W	Description	Reset
7-0	NSTH2	R/W	Non standard detection threshold 2	03h

0x06B – NSHYS

Bit	Function	R/W	Description	Reset
7-4	NSON	R/W	Non standard detection hysteresis for ON point	Ch
3-0	NSOFF	R/W	Non standard OFF point	1h

0x0C0 to 0x0CF – Internal Test

Address	Bit	R/W	Description	Reset
0x0C0 0x0C1 0x0C2 0x0C3	7 - 0	R	These four index addresses provide real time data read out of some internal counters. The index of these counters is set by 0x22B[7:4]. Index 0x0C0 0x0C1 0x0C2 0x0C3 0 LVPCNT_ODD[7:0] LVPCNT_ODD[15:8] LVPCNT_ODD[23:16] 1 LVPCNT_EVN[7:0] LVPCNT_EVN[15:8] LVPCNT_EVN[23:16] 2 LIVCNT_ODD[7:0] LIVCNT_ODD[11:8] 3 LIVCNT_EVN[7:0] LIVCNT_EVN[11:8] 4 LHPCNT[7:0] LHPCNT[13:8] LBOVFC[7:0] LBOVFC[10:8]	0000
Address	Bit	R/W	Description	Reset
0x0C4	7 - 4	R/W	Index for simulation initialization of internal auto calculation counters. 0: VPCNT[23:0] Pixel counter for 1 VSYNC period 1: LVPCNT_ODD[23:0] Pixel counter for 1 Odd field VSYNC period 2: LVPCNT_EVN[23:0] Pixel counter for 1 Even field VSYNC period 3: IVCNT[11:0] Line counter for 1 VSYNC period 4: LIVCNT_ODD[11:0] Line counter for 1 Odd field VSYNC period 5: LIVCNT_EVN[11:0] Line counter for 1 Even field VSYNC period 6: GOCNT[23:0] Pixel counter from VSYNC to the beginning of output display 7: LGOOCNT[23:0] Pixel counter from VSYNC to the beginning of output display (odd) 8: LGOECNT[23:0] Pixel counter from VSYNC to the beginning of output display (even)	0000
	3	R/W	1: Force auto calculation to treat input as two fields.	0
	2	R/W	1: Force auto calculation to treat input as one field.	0
	1 - 0	R/W	Sub index for the above counters, providing byte wide data read/write from/to 0x0C1. 00: Bits [7:0] of the counter pointed by the index 01: Bits [15:8] of the counter pointed by the index 10: Bits [23:16] of the counter pointed by the index	00
Address	Bit	R/W	Description	Reset
0x0C5	7 - 0	R/W	Data port for those counters mentioned in index 0x0C0.	-
Address	Bit	R/W	Description	Reset
0x0C6	7	R/W	Chip test usage only. Data output selection for analog circuit test. 0: V data 1: C data	0
	6	R/W	When set, gray scale data replace the normal data output to panel. The content of index 61 is used as the first pixel data.	0
	5	R/W	If this bit is set to "1", the scaler output is forced to all 0's.	0
	4	R/W	Load CHMAX counter (for debugging).	0
	3-2	R/W	Gray scale data selection.	0
	1	R/W	Start OSD ROM self test.	0
	0	R/W	Start OSD RAM self test.	0
Address	Bit	R/W	Description	Reset
0x0C7	7 - 0	R	BWYMIN	
Address	Bit	R/W	Description	Reset
0x0C8	7 - 0	R	BWYMAX	
Address	Bit	R/W	Description	Reset
0x0C9	7 - 0	R	BWFMIN	
Address	Bit	R/W	Description	Reset
0x0CA	7 - 0	R	BWFMAX	
Address	Bit	R/W	Description	Reset
0x0CB	7 - 0	R	BWBTILT	

Address	Bit	R/W	Description	Reset
0x0CC	7 - 0	R	BWWTILT	
Address	Bit	R/W	Description	Reset
0x0CD	7 - 0			
Address	Bit	R/W	Description	Reset
0x0CE	7 - 0	WR	TEST_MODE This register is reserved for testing purpose. In normal operation, only 0 should be written into this register. 03h = Digital video decoder & RGB mix direct input test This test mode allows digital data to be input from DTVD[23:0] pins to the input of the digital logic of the video decoder (replaces YCADC output) as the case when the contents of this register is 04h. Besides this, the FPG1/FPB1/FPR1 pins become inputs and provide data in place of RGBADC data output. 04h = Digital video decoder direct input test This test mode allows digital data to be input from DTVD pins to the input of the digital logic of the video decoder. (Replaces ADC output) DTVD(23-16) > "Y" decoder input data, DTVD(15-8) > "U" decoder input data DTVD(7-0) > "V" decoder input data 05h = Closed caption test mode. 06h = YCADC test mode (DTVD pins become outputs) YCADC digital output is made available externally. "Y" ADC output data > DTVD(15-8), "C" & "FB" ADC output data > DTVD(7-0) Index-63-bit-7 = 1 > "C" data Index-63-bit-7 = 0 > "FB" data. 07h = Digital video decoder output test (DTVD pins become outputs) The output of the digital video decoder output is available externally. "R" decoder out data > DTVD(23-16), "G" decoder out data > DTVD(15-8) "B" decoder out data > DTVD(7-0) "Vsync" > CLAMP "Hsync" > GPIO[1] "Hactive" > GPIO[0] 08h = RGBADC test mode (DTVD pins become outputs) RGBADC digital output is made available externally. "G" ADC output data > DTVD(15-8), "B" & "R" ADC output data > DTVD(7-0) Index-63-bit-7 = 1 > "B" data Index-63-bit-7 = 0 > "R" data. 09h = DAC test mode. DTVD[7:0] inputs are routed to the DAC data input "DIN". 11h = TW88 internal node to flat panel output	
Address	Bit	R/W	Description	Reset
0x0CF	7-0	R/W	Reserved	0

0x100 to 0x12F – OSD1

Address	Bit	R/W	Description	Reset
0X100	7 - 6	--	Reserved.	0
	5 - 4	R/W	OSD Window0 Horizontal Zoom Up Control 00: X1, 01: X2, 10: X3, 11: X4	01
	3 - 2	--	Reserved	0
	1 - 0	R/W	OSD Window0 Vertical Zoom Up Control 00: X1, 01: X2, 10: X3, 11: X4	01
Address	Bit	R/W	Description	Reset
0x101	7 - 4	R/W	OSD Window blinking background color	0000
	3 - 0	R/W	OSD Window auto fill color	0000
Address	Bit	R/W	Description	Reset
0x102	7 - 5	--	Reserved.	000
	4	R/W	Bitmap Color Write Assign Mode2 0: 1pixel/8bits, 1: 1pixel/4bits (4bits color max)	0
	3 - 2	R/W	Bitmap Color Write Assign Mode3 (0x102 bit[1:0]=2'b11, 8-bit mode case) 00: 1pixel/8bits, 01: 1pixel/4bits, 10: 1pixel/2bit, 11: 1pixel/1bit	00
	1 - 0	R/W	Bitmap Color Write Assign Mode1 00: 1pixel/4bits, 01: 1pixel/2bits, 10: 1pixel/1bit, 11: 1pixel/8bit (8-bit mode selection)	00
Address	Bit	R/W	Description	Reset
0x103	7 - 5	--	Reserved.	000
	4	R/W	Block Fill mode enable/disable control (1: Enable)	0
	3 - 1	--	Reserved.	000
	1	R/W	Block Transfer mode enable/disable control (1: Enable)	0
Address	Bit	R/W	Description	Reset
0x104	7 - 1	--	Reserved.	000 0000
	0	R/W	Block Fill/Transfer mode start (1: Start, 0: Auto Clear)	0
Address	Bit	R/W	Description	Reset
0x105	7 - 5	--	Reserved.	000
	4	R/W	Bitmap Data Write Enable	0
	3 - 1	--	Reserved.	000
	0	R/W	Source bitmap Data Write Enable	0
Address	Bit	R/W	Description	Reset
0x106	7 - 0	R/W	Bitmapped Window0 Start Address (7 – 0)	0000 0000
Address	Bit	R/W	Description	Reset
0x107	7 - 0	R/W	Bitmapped Window0 Start Address (15 – 8)	0000 0000
Address	Bit	R/W	Description	Reset
0x108	7 - 5	--	Reserved.	000
	4 - 0	R/W	Bitmapped Window0 Start Address (20 – 16)	0 1010
Address	Bit	R/W	Description	Reset
0x109	7 - 0	R/W	Bitmap Window0 V- Start Location (lower 8 bits) : 1 scanline per step	0001 0100
Address	Bit	R/W	Description	Reset
0x10A	7 - 0	R/W	Bitmap Window0 H – Start Location (1 pixel per step)	0010 0000
Address	Bit	R/W	Description	Reset
0x10B	7 - 4	R/W	Bitmap Window0 V- Start Location (upper 4 bits)	0000
	3 - 0	R/W	Bitmap Window0 H- Start Location (upper 4 bits)	0011
Address	Bit	R/W	Description	Reset
0x10C	7 - 0	R/W	Bitmap Window0 V – Length (1 line per step)	1000 0000

Address	Bit	R/W	Description	Reset
0x10D	7 - 0	R/W	Bitmap Window0 H - Length (1 pixel per step)	1000 0000
Address	Bit	R/W	Description	Reset
0x10E	7 - 4	R/W	Bitmap Window0 V - Length (upper 4 bits)	0000
	3 - 0	R/W	Bitmap Window0 H - Length (upper 4 bits)	0000
Address	Bit	R/W	Description	Reset
0x10F	7 - 0	R/W	Source Window V - Start Location (lower 8 bits) : 1 scanline per step	0000 0000
Address	Bit	R/W	Description	Reset
0x110	7 - 0	R/W	Source Window H - Start Location (1 pixel per step)	0000 0000
Address	Bit	R/W	Description	Reset
0x111	7 - 4	R/W	Source Window V - Start Location (upper 4 bits)	0000
	3 - 0	R/W	Source Window H - Start Location (upper 4 bits)	0000
Address	Bit	R/W	Description	Reset
0x112	7 - 0	R/W	Source/Destination Window V- Length (lower 8 bits) : 1 scanline per step	0000 0000
Address	Bit	R/W	Description	Reset
0x113	7 - 0	R/W	Source/Destination Window H – Length (1 pixel per step)	0000 0000
Address	Bit	R/W	Description	Reset
0x114	7 - 4	R/W	Source/Destination Window V- Length (upper 4 bits)	0000
	3 - 0	R/W	Source/Destination Window H- Length (upper 4 bits)	0000
Address	Bit	R/W	Description	Reset
0x115	7 - 0	R/W	Destination Window V- Start Location (lower 8 bits) : 1 scanline per step	0000 0000
Address	Bit	R/W	Description	Reset
0x116	7 - 0	R/W	Destination Window H – Start Location (1 pixel per step)	0000 0000
\Address	Bit	R/W	Description	Reset
0x117	7 - 4	R/W	Destination Window V- Start Location (upper 4 bits)	0000
	3 - 0	R/W	Destination Window H- Start Location (upper 4 bits)	0000
Address	Bit	R/W	Description	Reset
0x118	7 - 0	R/W	Write Data from Host Interface to OSD The internal write enable signal is generated automatically when 0x118 is accessed.	0000 0000
Address	Bit	R/W	Description	Reset
0x119	7 - 1	--	Reserved.	000 0000
	0	R/W	Bitamp OSD window0 Enable/Disable (1: Enable)	0
Address	Bit	R/W	Description	Reset
0x11A	7 - 0	R/W	Special Color Look-up table selection Address[7:0]	0000 0000
Address	Bit	R/W	Description	Reset
0x11B	7	R/W	Special Color Look-up table operation ON/OFF 1: ON , 0: OFF	0
	6	R/W	Special Color Look-up table Select	0
	5 - 4	R/W	Color Look-up Table Data Select 00: R 01: G 10: B 11: Color Attribute Data	00
	3 - 0	R/W	Color Look-up Table Select 0000: Table0 ~ 1111: Table15	0000
Address	Bit	R/W	Description	Reset
0x11C	7 - 0	R/W	Color Look-up Table Write Data When 0x11B[5:4] Attr. = 11, bit[5] : Blink, bit[4:0] : Alpha Blending 0 ~10000(Maximum)	0000 0000

Address	Bit	R/W	Description	Reset
0x11D	7	R/W	Look-up table Write Window Selection. (0x11A, 0x11B, 0x11C : control by this bit) 0: Window 0 1: Window 1	0
	6 - 5	--	Reserved.	00
	4	R/W	Color Look-up Table Conversion Enable 0: Disable, 1: Enable	0
	3	--	Reserved.	0
	2 - 0	R/W	Color Look-up Table Conversion Selection For 4 bit display, 000: Conversion[1:0] 001: Conversion[3:2] 010: Conversion[5:4] 011: Conversion[7:6] 100: Conversion[9:8] 101: Conversion[b:a] 110: Conversion[d:c] 111: Conversion[f:e] For 8 bit display, 000 : Table0 ~ 111 : Table 7	000
Address	Bit	R/W	Description	Reset
0x11E	7 - 0	R/W	Color Look-up Table Conversion Value Write.	0001 0000
Address	Bit	R/W	Description	Reset
0x11F	7 - 3	--	Reserved.	0 0000
	2	R	For every end of active window, this signal is toggled.	-
	1	R	For every end of Bitmap window active, this signal is toggled.	-
	0	R	For every end of Teletext window active, this signal is toggled.	-
Address	Bit	R/W	Description	Reset
0x120	7 - 6	--	Reserved.	00
	5	R/W	Window 1, 8-bit Mode Case : 16 color table or 256 color table selection	0
	4	R/W	Window 0, 8-bit Mode Case : 16 color table or 256 color table selection	0
	3	R/W	Color 8-bit Table Write Window Selection 0: Window 0 1: Window 1	0
	2	R/W	Color 8-bit Table Write enable/disable 0: Disable 1: Enable	0
	1 - 0	R/W	Color 8-bit Table Write Select 00: All Table 01: R Table 10: G Table 11: B Talbe	00
Address	Bit	R/W	Description	Reset
0x121	7 - 0	R/W	Color 8-bit Table Write Address[7:0]	0000 0000
Address	Bit	R/W	Description	Reset
0x122	7 - 0	R/W	Color 8-bit Table Write Data[7:0]	0000 0000
Address	Bit	R/W	Description	Reset
0x123	7 - 5	--	Reserved.	000
	4	R/W	RLC Packet Enable 0: Disable 1: Enable	0
	3 - 2	--	Reserved.	00
	1	R/W	RLC Reset 0: Normal 1: Reset	0
	0	R/W	RLC Bypass Mode 0: Disable 1: Bypass Enable	1
Address	Bit	R/W	Description	Reset
0x124	7 - 4	R/W	Data Count bit	0000
	3 - 0	R/W	Counter count bit	0000
Address	Bit	R/W	Description	Reset
0x125	7 -1	--	Reserved.	000 0000
	0	R/W	Bitamp OSD window1 Enable/Disable (1: Enable)	0

Address	Bit	R/W	Description	Reset
0X126	7 - 6	--	Reserved.	0
	5 - 4	R/W	OSD Window1 Horizontal Zoom Up Control 00: X1, 01: X2, 10: X3, 11: X4	01
	3 - 2	--	Reserved	0
	1 - 0	R/W	OSD Window1 Vertical Zoom Up Control 00: X1, 01: X2, 10: X3, 11: X4	01
Address	Bit	R/W	Description	Reset
0x127	7 - 0	R/W	Bitmapped Window1 Start Address (7 – 0)	0000 0000
Address	Bit	R/W	Description	Reset
0x128	7 - 0	R/W	Bitmapped Window1 Start Address (15 – 8)	0000 0000
Address	Bit	R/W	Description	Reset
0x129	7 - 5	--	Reserved.	000
	4 - 0	R/W	Bitmapped Window1 Start Address (20 – 16)	0 1010
Address	Bit	R/W	Description	Reset
0x12A	7 - 0	R/W	Bitmap Window1 V- Start Location (lower 8 bits) : 1 scanline per step	0000 0000
Address	Bit	R/W	Description	Reset
0x12B	7 - 0	R/W	Bitmap Window1 H – Start Location (1 pixel per step)	0000 0000
Address	Bit	R/W	Description	Reset
0x12C	7 - 4	R/W	Bitmap Window1 V- Start Location (upper 4 bits)	0000
	3 - 0	R/W	Bitmap Window1 H- Start Location (upper 4 bits)	0000
Address	Bit	R/W	Description	Reset
0x12D	7 - 0	R/W	Bitmap Window1 V – Length (1 line per step)	0000 0000
Address	Bit	R/W	Description	Reset
0x12E	7 - 0	R/W	Bitmap Window1 H - Length (1 pixel per step)	0000 0000
Address	Bit	R/W	Description	Reset
0x12F	7 - 4	R/W	Bitmap Window1 V - Length (upper 4 bits)	0000
	3 - 0	R/W	Bitmap Window1 H - Length (upper 4 bits)	0000
Address	Bit	R/W	Description	Reset
0x130	7 - 4	R/W	Bitmap Window0 H Zoom fraction control	0000
	3 - 0	R/W	Bitmap Window0 V Zoom fraction control	0000
Address	Bit	R/W	Description	Reset
0x131	7 - 4	R/W	Bitmap Window1 H Zoom fraction control	0000
	3 - 0	R/W	Bitmap Window1 V Zoom fraction control	0000
Address	Bit	R/W	Description	Reset
0x132	7-4	R/W	Reserved	0000
	3-0	R/W	Select OSD Logic color table 0~0x0F	0000
Address	Bit	R/W	Description	Reset
0x133	7-0	R/W	Data for Logic operation, It can be one of color look up table number.	00h
Address	Bit	R/W	Description	Reset
0x134	7	R/W	Enable Logical Operation table 15	0
	6	R/W	Enable Logical Operation table 14	0
	5	R/W	Enable Logical Operation table 13	0
	4	R/W	Enable Logical Operation table 12	0
	3	R/W	Enable Logical Operation table 11	0
	2	R/W	Enable Logical Operation table 10	0
	1	R/W	Enable Logical Operation table 9	0
	0	R/W	Enable Logical Operation table 8	0

Address	Bit	R/W	Description	Reset
0x135	7	R/W	Enable Logical Operation table 7	0
	6	R/W	Enable Logical Operation table 6	0
	5	R/W	Enable Logical Operation table 5	0
	4	R/W	Enable Logical Operation table 4	0
	3	R/W	Enable Logical Operation table 3	0
	2	R/W	Enable Logical Operation table 2	0
	1	R/W	Enable Logical Operation table 1	0
	0	R/W	Enable Logical Operation table 0	0
Address	Bit	R/W	Description	Reset
0x136	7 -5	R/W	Reserved	0000
	4	R/W	Double width Control during Block Transfer. 1: Enable	0
	3-1	R/W	Reserved	000
	0	R/W	Double Height Control during Block Transfer. 1: Enable	0

0x138 – CCFL/LED Control I

Bit	Function	R/W	Description	Reset
7	OVEN	R/W	Over voltage feedback control 0 = disable 1 = enable	1
6	OIEN	R/W	Over current feedback control 0 = disable 1 = enable	1
5	UIEN	R/W	Under current feedback control 0 = disable 1 = enable	1
4	FBEN	R/W	CCFL feedback loop control 0 = open loop 1 = close loop	1
3	LOCKV	R/W	0 = Dimming frequency set by FDIM 1 = Dimming frequency locked to panel vertical sync.	0
2	LOCkH	R/W	0 = PWM frequency set by FPWM 1 = PWM frequency locked to panel horizontal frequency	0
1	CCFLENB	R/W	0 = analog sense power down 1 = analog sense power up.	1
0	CCFLDEN	R/W	0 = CCFL out disable. 1 = CCFL out enable.	0

0x139 – CCFL/LED Sense Threshold

Bit	Function	R/W	Description	Reset
7-6	LVT	R/W	Lamp voltage threshold	2h
5-4	LILT	R/W	Lamp low current threshold	2h
3-0	LIT	R/W	Lamp normal current threshold	Dh

0x13A – CCFL/LED Control II

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W		00
5-4	CC_LED_ST	R/W	CCFL or LEDC status	-
3-0	LSTP	R/W	Feedback gain control with 1 being the smallest gain.	4h

0x13B – CCFL/LED PWM

Bit	Function	R/W	Description	Reset
7-0	FPWM	R/W	PWM control frequency. In CCFL mode, Freq = 6.75MHz / Fpwm. In LED mode, Freq = 27MHz / Fpwm and Fpwm[7:6] should be 0.	80h

0x13C – CCFL/LED Dim Frequency

Bit	Function	R/W	Description	Reset
7-0	FDIM	R/W	Dimming frequency control. Freq = 13.18KHz / Fdim	84h

0x13D – CCFL/LED Dim Control

Bit	Function	R/W	Description	Reset
7	LED_DIG_EN	R/W	0 = LEDC disable, 1 = LEDC enable	0
4-0	DDIM	R/W	dimming control. 0=full brightness, 1F=lowest brightness	00h

0x13E – PWMTOP

Bit	Function	R/W	Description	Reset
7-0	PWMTOP	R/W	Reserved	20h

0x151 to 0x15F – External OSD & Misc.

Address	Bit	R/W	Description	Reset
0x151	7 - 5	--	Reserved.	000
	4	R/W	OSD Wait Mask Signal 0: Mask Enable, 1: Mask Disable	1
	3 - 2	--	Reserved.	00
	1	R	OSD Wait Signal (Active High)	-
	0	--	Reserved.	0
Address	Bit	R/W	Description	Reset
0x152	7	R/W	External OSD Clock mode 0: free-run, 1: triggered osd_clk	1
	6	R/W	External OSD VS polarity control	0
	5	R/W	External OSD Horizontal active polarity control	0
	4	R/W	External OSD Clock polarity control	0
	3 - 1	R/W	External OSD Access Latency control	000
	0	R/W	External OSD Port Enable/Disable 0: Disable, 1: Enable	0
Address	Bit	R/W	Description	Reset
0x153	7 - 2	--	Reserved.	00 0000
	1	R/W	External OSD Horizontal Active Signal mode Selection 0: Fontmap Window type, 1: Internal H-active Window type	0
	0	R/W	External OSD Sync mode Selection 0: Hactive style, 1: Hsync, Vsync style	0
Address	Bit	R/W	Description	Reset
0x154	7	--	Reserved.	0
	6 - 4	R/W	External OSD clock EOCLK delay time selection. 000: No delay time inserted. Each increment increases the delay by 1 ns.	000
	3	--	Reserved.	0
	2 - 0	R/W	Bitmap Window OSD Gain Value Control Gain[2:0] OSD Value 0 1.000 1 0.953 2 0.906 3 0.859 4 0.797 5 0.750 6 0.703 7 0.656	000
Address	Bit	R/W	Description	Reset
0x155	7 - 0	R/W	OSD Test Mode	0000 0000
Address	Bit	R/W	Description	Reset
0x156	7	R/W	Reserved.	0
	6	--	Reserved.	0
	5 -4	R/W	Sub Path OSD Selection 00: No OSD, 01: Bitmap0 & Ext, 10: Bitmap1, 11: All OSD	00
	3	--	Reserved.	0
	2	--	Reserved.	0
	1 - 0	R/W	Main Path OSD Selection 00: No OSD, 01: Bitmap0 & Ext, 10: Bitmap1, 11: All OSD	00
Address	Bit	R/W	Description	Reset
0x157	7 - 5	--	Reserved.	000
	4 - 0	R/W	External OSD Alpha-Blending Level Control.	

Address	Bit	R/W	Description	Reset
0x158	7 - 5	--	Reserved.	000
	4	R/W	DMA Interface Wait Mask Signal 0: Mask Enable, 1: Mask Disable	0
	3 - 1	--	Reserved.	000
	0	R	DMA Interface Wait Signal	0
Address	Bit	R/W	Description	Reset
0x159	7	R/W	Analog External Osd Input Enable	0
	6:4	R/W	External Osd Input Data Enable signal Delay : 0 ~ 7 clock cycle delay	000
	3	R/W	Analog External Osd Vsync polarity Inversion	0
	2	R/W	Analog External Osd Hsync polarity Inversion	0
	1	R/W	*	0
	0	R	RLC Wait Signal (Active High)	-

Host Parallel Interface / DMA Configuration Registers

0x1A0 – Mode Setting Register

Bit	Function	R/W	Description	Reset
7-2		R/W	Reserved	---
1	WAIT	R/W	Generation wait signal 0 : Wait signal doesn't working (Always off) 1 : Wait signal working depend on status	1
0	DMA_SEL	R/W	Select data transfer type 0 : Host parallel path 1 : DMA	0

0x1A1– Total Transfer Count High Byte Register

Bit	Function	R/W	Description	Reset
7-0	XFER_CNT	R/W	It is indicate that how many bytes data transfer base on four bytes unit either read or write to/from chip per command. It's support up to 64KBbytes a command so bit[15:8].	00h

0x1A2– Total Transfer Count Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	XFER_CNT	R/W	It is indicate that how many bytes data transfer base on four bytes unit either read or write to/from chip per command. This is bit 7-0. The data transfer must be multiple of four. (ex) 4Bytes = 04h, 8Bytes = 08h	00h

0x1A3 – Memory Access Address High Byte Register

Bit	Function	R/W	Description	Reset
7-5		R/W	Reserved	---
4-0	MEM_ADR	R/W	Memory access address include in row and column address. Bit[20-16]	00h

0x1A4 – Memory Access Address Medium Byte Register

Bit	Function	R/W	Description	Reset
7-0	MEM_ADR	R/W	Memory access address include in row and column address. Bit[15-8]	00h

0x1A5– Memory Access Address Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	MEM_ADR	R/W	Memory access address include in row and column address. Bit[7-0]	00h

0x1A6– Data Access (Read/Write) Register

Bit	Function	R/W	Description	Reset
7-0	DATA_CH	R/W	Data access channel from/to Memory to/from Microprocessor.	00h

0x1A7 – Command Register

Bit	Function	R/W	Description	Reset
7-1		R/W	Reserved	---
0	RD_WR	R/W	Data transfer direction command bit 0 : read command (data flow : MCU data read from memory) 1 : write command (data flow : MCU data write to memory) *** It'll be write access later than other register setting because of immediately start operation after access this bit.	0

0x1A8– Status Read Register

Bit	Function	R/W	Description	Reset
7-3			Reserved	---
2	RD_MON	R	Read (Microprocessor from Memory) operation done 0 : Still operation 1 : Read data transfer done	0
1	WR_MON	R	Write (Microprocessor to Memory) operation done 0 : Still operation 1 : Write data transfer done	0
0	WAIT_MON	R	Wait status monitoring bit 0 : No wait 1 : Wait	0

0x1B0 to 0x1BF – Status and Interrupt Registers

Address	Bit	R/W	Name	Description	Reset
0X1B0	7	R	Line buffer over flow	This bit is set if the FP clock count exceeds the maximum number in between two consecutive FPHS pulses for the even field, cleared by writing back a "1".	0
	6	R	Line buffer under flow	This bit is set if the FP clock count exceeds the maximum number in between two consecutive FPHS pulses for the odd field, cleared by writing back a "1".	0
	5	R	Input VSYNC Loss status changed	This bit is set when the status bit of "Input VSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
	4	R	Input HSYNC Loss status changed	This bit is set when the status bit of "Input HSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
	3	R/W	Video input status changed indication	Vdloss status bit change (register 1 bit 7) or det50 status bit change (register 1 bit 0) Write a one to this bit to reset.	0
	2	R	Input VSYNC Loss	This bit is set when the input VSYNC pulse is lost, reset by re-appearance of VSYNC. An 11-bit counter is used for VSYNC period measurement. If this counter overflows 4 times, the VSYNC is considered to be lost.	0
	1	R	Input HSYNC Loss	This bit is set when the input HSYNC pulse is lost, reset by re-appearance of HSYNC. An 11-bit counter is used for HSYNC period measurement. If this counter overflows 4 times, the HSYNC is considered to be lost.	0
	0	R	SYNC detect status	Logic function of: Inverted "bit 1" ANDing with inverted "bit 2"	
Address	Bit	R/W	Name	Description	Reset
0X1B1	7	R	Input Measurement Data Ready	This bit is set when the measurement data is ready for readout, reset when a new "startm" is set.	0
	6	R	Power State Changed	This bit is set when the power management state has changed, reset by writing back a "1".	0
	5	R	Input VSYNC Period Change Detected	This bit is set when the input VSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the VSYNC period is measured for every frame. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the VSYNC period is considered to have changed.	0
	4	R	Input HSYNC Period Change Detected	This bit is set when the input HSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the HSYNC period is measured for every scan line. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the HSYNC period is considered to have changed.	0
	3	R	Line buffer Overflow or Underflow		0
	2	R	VDCCDET	High if there is a change in VDLOSS or DET50 or CCVALID	0
	1	R	VLOSS/ HLOSS status changed	This bit reflects the "OR" condition of status bit index B0 bit 5 (VLOSS status changed) and index B0 bit 4 (HLOSS status changed).	0
	0	R	"SYNC Detect Status" Changed	This bit is set when the status bit of "SYNC Detect Status" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
Address	Bit	R/W	Description		Reset
0X1B2	7	R/W	Enable/Disable 0x1B1 bit 7 as an IRQ source 0: Enable 1: Disable		1
	6	R/W	Enable/Disable 0x1B1 bit 6 as an IRQ source 0: Enable 1: Disable		1
	5	R/W	Enable/Disable 0x1B1 bit 5 as an IRQ source 0: Enable 1: Disable		1

Address	Bit	R/W	Name	Description	Reset
	4	R/W	Enable/Disable 0x1B1 bit 4 as an IRQ source 0: Enable 1: Disable		1
	3	R/W	Enable/Disable 0x1B1 bit 3 as an IRQ source 0: Enable 1: Disable		1
	2	R/W	Enable/Disable 0x1B1 bit 2 as an IRQ source 0: Enable 1: Disable		1
	1	R/W	Enable/Disable 0x1B1 bit 1 as an IRQ source 0: Enable 1: Disable		1
	0	R/W	Enable/Disable 0x1B1 bit 0 as an IRQ source 0: Enable 1: Disable		1
Address	Bit	R/W	Description		Reset
0X1B3	7 - 3	R/W	*		00h
	2	R/W	Enable/Disable VDLOSS as an IRQ source 0: Enable 1: Disable		1
	1	R/W	Reserved		1
	0	R/W	Enable/Disable DET50 as an IRQ source 0: Enable 1: Disable		1
Address	Bit	R/W	Name	Description	Reset
0X1B4	7	R	Line buffer over flow	Same as 0x1B0[7]	0
	6	R	Line buffer under flow	Same as 0x1B0[6]	0
	5	R	PIP Input VSYNC Loss status changed	This bit is set when the status bit of "Input VSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
	4	R	PIP Input HSYNC Loss status changed	This bit is set when the status bit of "Input HSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
	3	R/W	Video input status changed indication	Same as 0x1B0[3]	0
	2	R	PIP Input VSYNC Loss	This bit is set when the input VSYNC pulse is lost, reset by re-appearance of VSYNC. An 11-bit counter is used for VSYNC period measurement. If this counter overflows 4 times, the VSYNC is considered to be lost.	0
	1	R	PIP Input HSYNC Loss	This bit is set when the input HSYNC pulse is lost, reset by re-appearance of HSYNC. An 11-bit counter is used for HSYNC period measurement. If this counter overflows 4 times, the HSYNC is considered to be lost.	0
	0	R	PIP SYNC detect status	Logic function of: Inverted "bit 1" ANDing with inverted "bit 2"	
Address	Bit	R/W	Name	Description	Reset
0X1B5	7	R	Input Measurement Data Ready	Same as 0x1B1[7]	0
	6	R	Power State Changed	Same as 0x1B1[6]	0
	5	R	PIP Input VSYNC Period Change Detected	This bit is set when the input VSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the VSYNC period is measured for every frame. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the VSYNC period is considered to have changed.	0
	4	R	PIP Input HSYNC Period Change Detected	This bit is set when the input HSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the HSYNC period is measured for every scan line. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the HSYNC period is considered to have changed.	0

Address	Bit	R/W	Name	Description	Reset
	3	R	Line buffer Overflow or Underflow	Same as 0x1B1[3]	0
	2	R	VDCCDET	Same as 0x1B1[2]	0
	1	R	PIP VLOSS/ HLOSS status changed	This bit reflects the "OR" condition of status bit index B0 bit 5 (VLOSS status changed) and index B0 bit 4 (HLOSS status changed).	0
	0	R	PIP "SYNC Detect Status" Changed	This bit is set when the status bit of "SYNC Detect Status" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
Address	Bit	R/W	Name	Description	Reset
0X1B6	7	R	Line buffer over flow	Same as 0x1B0[7]	0
	6	R	Line buffer under flow	Same as 0x1B0[6]	0
	5	R	MPIP Input VSYNC Loss status changed	This bit is set when the status bit of "Input VSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
	4	R	MPIP Input HSYNC Loss status changed	This bit is set when the status bit of "Input HSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
	3	R/W	Video input status changed indication	Same as 0x1B0[3]	0
	2	R	MPIP Input VSYNC Loss	This bit is set when the input VSYNC pulse is lost, reset by re-appearance of VSYNC. An 11-bit counter is used for VSYNC period measurement. If this counter overflows 4 times, the VSYNC is considered to be lost.	0
	1	R	MPIP Input HSYNC Loss	This bit is set when the input HSYNC pulse is lost, reset by re-appearance of HSYNC. An 11-bit counter is used for HSYNC period measurement. If this counter overflows 4 times, the HSYNC is considered to be lost.	0
	0	R	MPIP SYNC detect status	Logic function of: Inverted "bit 1" ANDing with inverted "bit 2"	
Address	Bit	R/W	Name	Description	Reset
0X1B7	7	R	Input Measurement Data Ready	This bit is set when the measurement data is ready for readout, reset when a new "startm" is set.	0
	6	R	Power State Changed	Same as 0x1B1[6]	0
	5	R	MPIP Input VSYNC Period Change Detected	This bit is set when the input VSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the VSYNC period is measured for every frame. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the VSYNC period is considered to have changed.	0
	4	R	MPIP Input HSYNC Period Change Detected	This bit is set when the input HSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the HSYNC period is measured for every scan line. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the HSYNC period is considered to have changed.	0
	3	R	Line buffer Overflow or Underflow	Same as 0x1B1[3]	0
	2	R	VDCCDET	Same as 0x1B1[2]	0
	1	R	MPIP VLOSS/ HLOSS status changed	This bit reflects the "OR" condition of status bit index B0 bit 5 (VLOSS status changed) and index B0 bit 4 (HLOSS status changed).	0
	0	R	MPIP "SYNC Detect Status" Changed	This bit is set when the status bit of "SYNC Detect Status" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
Address	Bit	R/W	Name	Description	Reset

Address	Bit	R/W	Name	Description	Reset
0X1B8	7-6	R/W	Measurement input selection	0,1: Main, 2: PIP, 3: MPIP	00
	5	R/W		0: Enable 0x1B5[5] as an IRQ source	0
	4	R/W		0: Enable 0x1B5[4] as an IRQ source	0
	3-2	R/W		Reserved	00
	1	R/W		0: Enable 0x1B5[1] as an IRQ source	0
	0	R/W		0: Enable 0x1B5[0] as an IRQ source	0
Address	Bit	R/W	Name	Description	Reset
0X1B9	7-6	R/W		Reserved	00
	5	R/W		0: Enable 0x1B7[5] as an IRQ source	0
	4	R/W		0: Enable 0x1B7[4] as an IRQ source	0
	3-2	R/W		Reserved	00
	1	R/W		0: Enable 0x1B7[1] as an IRQ source	0
	0	R/W		0: Enable 0x1B7[0] as an IRQ source	0

ADC/LLPLL Configuration Registers

0x1C0 – LLPLL Input Control Register

Bit	Function	R/W	Description	Reset
7-6	INP_SEL	R/W	SOG input selection. 0=SOG0, 1=SOG1, 2,3=NA	0
5	CS_INV	R/W	CSYNC Detection Input Polarity, active low needed. 0 : No Inversion 1 : Inversion	0
4	CS_SEL	R/W	PLL Input Selection 0 : Slicer or HS 1 : CS_PAS	0
3	SOG_SEL	R/W	CSYNC Detection Selection 0 : SOG Slicer 1 : HSYNC	0
2	HS_POL	R/W	PLL Input Polarity 0 : Inversion 1 : Normal	0
1	Reserved	R/W		0
0	CK_SEL	R/W	PLL Output Clock selection 0 : Select PLL clock 1 : Select oscillator clock	0

0x1C1 – LLPLL Input Detection Register

Bit	Function	R/W	Description	Reset
7	VS_POL	R	Detected VSYNC polarity, 0 = low active	-
6	HS_POL	R	Detected HSYNC polarity, 0 = low active	-
5	VS_DET	R	VSYNC detection	-
4	HS_DET	R	HSYNC detection	-
3	CS_DET	R	Composite Sync detection	-
2-0	DET_FMT	R	Composite Sync format detection 0 : 480i, 1 : 576i, 2 : 480p, 3 : 576p 4 : 1080i, 5 : 720p 6: 1080p 7: none of above	-

0x1C2 – LLPLL Control Register

Bit	Function	R/W	Description	Reset
7-6	LLC_POST	R/W	PLL post divider 0= 1 1= ½ 2= ¼ 3= 1/8	0
5-4	LLC_VCO	R/W	VCO range select (MHz) 00 = 5 ~ 27 01 = 10 ~ 54 10 = 20 ~ 108 11 = 40 ~ 216	0
3	Reserved			
2-0	LLC_IPMP	R/W	Charge pump currents (uA) 000 = 1.5 001 = 2.5 010 = 5 011 = 10 100 = 20 101 = 40 110 = 80 111 = 160	0

0x1C3 – LLPLL Divider High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	LLC_ACKN[11:8]	R/W	PLL feedback divider.	3h

0x1C4 – LLPLL Divider Low Register

Bit	Function	R/W	Description	Reset
7-0	LLC_ACKN[7:0]	R/W	PLL feedback divider	5Ah

0x1C5 – LLPLL Clock Phase Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	-
4-0	LLC_PHA	R/W	This 5bit value adjusts the sampling phase in 32 steps across on pixel time. Each step represents an 11.25 degree shift in sampling phase.	00h

0x1C6 – LLPLL Loop Control Register

Bit	Function	R/W	Description	Reset
7	LLC_ACPL	R/W	PLL loop control 0: Closed Loop 1: Open Loop	0
6-4	LLC_APG	R/W	PLL loop gain control	2h
3	Reserved	R/W	Reserved	0
2-0	LLC_APZ	R/W	PLL filter control	0h

0x1C7 – LLPLL VCO Control Register

Bit	Function	R/W	Description	Reset
3-0	LLC_ACKI[11-8]	R/W	PLL VCO nominal frequency. Reserved for internal use.	4h

0x1C8 – LLPLL VCO Control Register

Bit	Function	R/W	Description	Reset
7-0	LLC_ACKI[7-0]	R/W	PLL_VCO nominal frequency. Reserved for internal use.	00h

0x1C9 – LLPLL Pre Coast Register

Bit	Function	R/W	Description	Reset
7-0	PRE_COAST	R/W	Sets the number of HSYNC periods that coast is active before VSYNC edge.	06h

0x1CA – LLPLL Post Coast Register

Bit	Function	R/W	Description	Reset
7-0	POST_COAST	R/W	Sets the number of HSYNC periods that coast is active after VSYNC edge.	06h

0x1CB – SOG Threshold Register

Bit	Function	R/W	Description	Reset
7	PUSOG	R/W	SOG power down control, 0 – power down	0
6	PUPLL	R/W	PLL power down control, 0 - power down	0
5	COAST_EN	R/W	PLL Coast control, 1 - Enable	1
4-0	SOG_TH[4:0]	R/W	SOG slicer threshold This bits control the comparator threshold of the SOG slicer at 10mV per every step. The setting value of 5''b00000 equals 330mV and the maximum setting value is 5'11111 which equals 10mV.	10h

0x1CC – Scaler Sync Selection Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	0
4	VSY_SEL	R/W	Active VSYNC select 0 : Composite Sync Separation Output 1 : VSYNC input pin	0
3-2	HSY_SEL	R/W	Active HSYNC select 00 - HSYNC pin 01 – CS_PAS 10 – Sync separator output 11 – HSO	0h
1	VSY_POLC	R/W	VSYNC polarity control 0 – No inversion 1 - Inversion	0
0	HSY_POLC	R/W	HSYNC polarity control 0 – No inversion 1 - Inversion	0

0x1CD – PLL Initialization Register

Bit	Function	R/W	Description	Reset
0	INIT	R/W	PLL initialization, self-resetting	0

0x1CE – RGB ADC Misc. Register

Bit	Function	R/W	Description	Reset
7	ADC_CLK_SEL	R/W	RGB Path Clock selection 1: Select Xtall clock 0: Select Original Line Lock clock	0
6		R/W	Reserved	0
5	DTV	R/W	ADC Input mode selection 1: DTV 0: RGB	0
4		R/W	Reserved	0
3	PDA	R/W	ADC G-channel Power Down 1 : Power Down 0: Normal Operation	0
2		R/W	Reserved	0
1	INREFV	R/W	ADC Reference voltage select 1: Internal Reference Disable 0: Internal Reference Enable	0
0	INREFI	R/W	ADC Bias Reference current select 1: Bias Current Boost 0: Bias Current Normal	0

0x1CF – RGB ADC Misc2. Register

Bit	Function	R/W	Description	Reset
7:6	INP_SEL_ADC	R/W	ADC Data Input pin Select 3: Select input #3 2: Select input #2 1: Select input #1 0: Select input #0	00
5:0	SAVE	R/W	PGA/ADC Power Save Mode [5:3]=: PGA bias current control : Bigger value means Smaller current setting [2:0] = ADC bias current control : Bigger value means Smaller current setting	001001

0x1D0 – Clamp Gain Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3	Reserved	R/W	Reserved	-
2	GAINY[8]	R/W	Y channel gain adjust bit[8]	0
1	GAINC[8]	R/W	C channel gain adjust bit[8]	0
0	GAINV[8]	R/W	V channel gain adjust bit[8]	0

0x1D1 – Y Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINY[7-0]	R/W	Y channel gain adjust bit[7-0]	F0h

0x1D2 – C Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINC[7-0]	R/W	C channel gain adjust bit[7-0]	F0h

0x1D3 – V Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINV[7-0]	R/W	V channel gain adjust bit[7-0]	F0h

0x1D4 – Clamp Mode Control Register

Bit	Function	R/W	Description	Reset
7	RGB_SEL	R/W	RGB or YCV selection 0 : YCV Mode 1 : RGB Mode	0
6	Reserved	R/W	Reserved	-
5	CL_EDGE	R/W	Clamp reference edge	0
4	CLKY	R/W	Clamping current control 1	0
3	CLKC	R/W	Clamping current control 2	0
2	CL_Y_EN	R/W	Green / Y channel clamp 0 : enable, 1 : disable	0
1	CL_C_EN	R/W	Blue / C channel clamp 0 : enable, 1 : disable	0
0	CL_V_EN	R/W	Red / V channel clamp 0 : enable, 1 : disable	0

0x1D5 – Clamp Start Position Register

Bit	Function	R/W	Description	Reset
7-0	CL_ST	R/W	This register sets programmable clamping start position. It is start count value that after the trailing edge of the HSYNC signal.	00h

0x1D6 – Clamp Stop Position Register

Bit	Function	R/W	Description	Reset
7-0	CL_ED	R/W	This register sets programmable clamping stop position. Clamping duration set between start and stop position.	10h

0x1D7 – Clamp Master Location Register

Bit	Function	R/W	Description	Reset
7-0	CL_LOC	R/W	This bit sets the RGB(YCV) clamp position from the H sync edge.	70h

0x1D8 – ADC TEST Register

Bit	Function	R/W	Description	Reset
7	Reserved			0
6-4	LLC_DBG_SEL	R/W	Debugging register for internal use	00h
3	Reserved			
2	RGB_ADC_TEST	R/W	Internal Test Only	0
1	CL_TEST_Y	R/W	Programmable Green / Y select 0: Use default value (G:0x10, U/V:0x3c) 1: Programmable value	0
0	CL_TEST_UV	R/W	Programmable Blue and Red / U and V select 0: Use default value (R/B:0x10, U/V:0x80) 1: Programmable value	0

0x1D9 – Y Clamp Reference Register

Bit	Function	R/W	Description	Reset
7-0	CL_Y_VAL	R/W	Green/ Y channel Clamping reference level in programmable mode.	10h

0x1DA – C Clamp Reference Register

Bit	Function	R/W	Description	Reset
7-0	CL_C_VAL	R/W	Blue and Red/ U and V channel Clamping reference level in programmable mode.	80h

0x1DC – HSYNC Width Register

Bit	Function	R/W	Description	Reset
7-6		R/W	Reserved	00
5-0	HSWID	R/W	Hsync Widith. The unit of HWSID is one clock cycle.	00h

0x1DD – R Channel ADC Offset Register

Bit	Function	R/W	Description	Reset
7-0	OFFSETR	R/W	R Channel ADC Offset Value.	80h

0x1DE – G Channel ADC Offset Register

Bit	Function	R/W	Description	Reset
7-0	OFFSETG	R/W	G Channel ADC Offset Value.	80h

0x1DF – B Channel ADC Offset Register

Bit	Function	R/W	Description	Reset
7-0	OFFSETB	R/W	B Channel ADC Offset Value.	80h

0x1F0 to 0x1FE – LCDC – Gamma

Address	Bit	R/W	Description	Reset
0x1F0	7	R/W	Enable Red gamma correction.	0
	6	R/W	Enable Green gamma correction.	0
	5	R/W	Enable Blue gamma correction.	0
	4	R/W	Reserved.	0
	3-2	R/W	Enable Gamma table address auto increment for reading/writing Gamma data port. 00: Disable, 01: Read Only, 10: Write Only, 11: Read/Write	00
	1 - 0	R/W	Gamma tables access selection: Index address 0x1F1 to 0x1F2 are used for gamma table accesses. There are 3 sets of gamma table, one table for one color, sharing the same address port and data port. These 2 bits identifies which table is accessed. 00: RGB Gamma table 01: Red Gamma table 10: Green Gamma table 11: Blue Gamma table	00
Address	Bit	R/W	Description	Reset
0x1F1	7-4	R/W	Gamma table address port.	0000 0000
Address	Bit	R/W	Description	Reset
0x1F2	7 - 2	R/W	Reserved	00 0000
	1 - 0	R/W	Gamma table data port (upper bits)	00
Address	Bit	R/W	Description	Reset
0x1F3	7 - 0	R/W	Gamma table data port (lower bits)	0000 0000

Flat Panel Display Registers

0x20E to 0x20F – Input Type Registers

Address	Bit	R/W	Description	Reset
0x20E	7		Reserve	
	6		Reserve	
	5		Reserve	
	4		Reserve	
	3		Reserve	
	2		Reserve	
	1		Reserve	
	0	R/W	Dual_656 input enable; 1=Enable, 0=Disable	0
Address	Bit	R/W	Description	Reset
0x20F	7:6	R/W	Sequentiall RGB alternative line data based on RGB input order 3 = G->B->R 2 = R->G->B 1 = B->R->G 0 = G->B->R	0
	5:4	R/W	Sequentiall RGB Input order 3 = R->G->B 2 = B->R->G 1 = G->B->R 0 = R->G->B	0
	3:2	R/W	Sequentiall RGB Input 8 bit selection out of [23:0] 3 = Select 8 bit for [7:0] 2 = Select 8 bit for [23:16] 1 = Select 8 bit for [15:0] 0 = Select 8 bit for [7:0]	0
	1	R/W	0 = Sequential RGB Clock polarity disable 1 = Sequential RGB Clock polarity Inversion	0
	0	R/W	0 = Sequential RGB mode disable 1 Sequential RGB mode enable	0

0x210 to 0x21F – Input and Input Related Registers

Address	Bit	R/W	Description	Reset
0x210	7	R/W	This bit has dual function. It serves as odd field detection method selection or ITU656 progressive/interlaced selection. If bits 3:2 of Index 0x214h does not choose ITU656: Odd Field Detection Method for Digital input port 0: Use internal default method 1: Use Detection method defined by register 0x215 If bits 3:2 selects ITU656, this bit sets the input to interlaced (0) or progressive(1).	0
	6	R/W	Invert internal detected field signal	0
	5	R/W	Field is determined by the leading or trailing edge of input VSYNC when using 0x215 for field determination. 1: Trailing edge.	0
	4	R/W	Enable CSYNC (Composite SYNC); Input pin DTVHS is treated as a CSYNC input.	0
	3	R/W	DE polarity of the digital source. 0: Active High	0
	2	R/W	HSYNC polarity of the digital source. 0: Active High	0
	1	R/W	VSYNC polarity of the digital source. 0: Active High	0
	0	R/W	Invert Digital input port DTVCLK polarity, 0: Rising edge 1: Falling edge	0

Address	Bit	R/W	Description	Reset
0x211	7	R/W	EPDEN	0
	6	R/W	PDEN_POL.	0
	5	R/W	Select Explicit DE (Data Enable also called HA for Horizontal Active); 0: HA is asserted in the input active region defined by registers 0x217 through 0x21D 1: HA is sourced by individual video source	0
	4	R/W	0 = DTVDE is used as the data enable (DE). 1 = DTVDE is used as HSYNC input	0
	3	-	Reserved.	0
	2 - 0	R/W	Input clock DTVCLK delay time selection. 000: No delay time inserted. Each increment increases the delay by 1 ns.	000
Address	Bit	R/W	Description	Reset
0x212	7	R/W	Enable field detection for Digital input port when index 0x214 bit 1 & 0 is 2'b10.	0
	6	R/W	Set this bit to "1" if the DTVVS input is not a pulse but a "field" signal.	0
	5	R/W	ITU656 even field VSYNC delay. 1: Delay the assertion to the falling edge of "ha". 0: No delay	0
	4	R/W	Use filtered HSYNC to maintain constant input HSYNC period.	0
	3	R/W	Set this bit to 1 in 8 bit 601 mode if the Cr data arrives before Cb data.	0
	2 - 0	R/W	Data bus routing selection for Digital input port For 24 bit YpbPr or 24 bit RGB DTVD[23:16] DTVD[15:8] DTVD[7:0] 000: Pr/B Y/R Pb/G 001: Pr/B Pb/G Y/R 010: Pb/G Y/R Pr/B 011: Pb/G Pr/B Y/R 100: Y/R Pb/G Pr/B 101: Y/R Pr/B Pb/G For 16 bit YPb/Pr: Follow the table above with Y and Pb. Example: If Y data is connected to DTVD[23:16] and Pb/Pr data is connected DTVD[7:0], the bus routing selection should be set to "101". If Explicit DE, Inde0x214 bit [4], is set, the very first DTVDE is assumed to have Pb data. On the other hand if Explicit DE is reset, Index 0x210 bit [3] is used to select the order of Pb /Pr. For 8 bit Y/Pb/Pr: Follow the table above with Pr. Example: If Y/Pb/Pr data is connected to DTVD[15:8], the bus routing selection can be set to "011" or "101". Use the table below for the correct data order. Explicit DE Index-0x210-bit-3 Index 0x27A-bit-5 Data Order 1 X 0 Pb-Y-Pr-Y 1 X 1 Pr-Y-Pb-Y 0 0 0 Pb-Y-Pr-Y 0 0 1 Pr-Y-Pb-Y 0 1 0 Y-Pb-Y-Pr 0 1 1 Y-Pr-Y-Pb	100

Address	Bit	R/W	Description	Reset
0x213	7:1	R/W	Internal clock polarity control	000_0000
	0	R/W	RGB color space selection 1: RGB, 0: YUV	0
Address	Bit	R/W	Description	Reset
0x214	7 - 6	R/W	COAST is driven to "enabled" state in the window defined below 00: COAST enabled 1 HSYNC period before VSYNC and 7 HSYNC periods after VSYNC 01: COAST enabled 2 HSYNC periods before VSYNC and 8 HSYNC periods after VSYNC 10: COAST enabled 3 HSYNC periods before VSYNC and 9 HSYNC periods after VSYNC 11: COAST enabled 4 HSYNC periods before VSYNC and10 HSYNC periods after VSYNC	00
	5	R/W	Reserved.	0
	4	R/W	1: Choose 8 bit 601 input mode 0: Choose 8bit 656 input mode	0
	3 - 2	R/W	Input format selection; 00: 422 (16 bit ITU601), 01: ITU656 (8 bits) or ITU601 (8 bit) ; determined by bit 4. 10: 444, 11: RGB	10
	1 - 0	R/W	Input Video source selection; 00: Internal analog video decoder, 01: RGB 10: Digital input 11: PIP	00
Address	Bit	R/W	Description	Reset
0x215	7 - 4	R/W	Horizontal Ending Locations of internal Odd Field Detection for Digital input port	0101
	3 -0	R/W	Horizontal Starting Locations of internal Odd Field Detection for Digital input port	0100

	Start Pixel	End Pixel		Start Pixel	End Pixel
0000	32	64	1000	512	1024
0001	64	128	1001	576	1152
0010	128	256	1010	640	1280
0011	192	384	1011	704	1408
0100	256	512	1100	768	1536
0101	320	640	1101	832	1664
0110	384	768	1110	896	1792
0111	448	896	1111	960	1920

Address	Bit	R/W	Description	Reset
0x216	7 - 0	R/W	Offset amount to re-construct VSYNC from CSYNC input. The L to H transition of CSYNC input provides the L to H transition of HSYNC. This register defines the amount of offset from this transition edge for generating VSYNC.	0010 0000
Address	Bit	R/W	Description	Reset
0x217	7 - 0	R/W	Input Active Window definition: Horizontal Starting Pixel Position - Low Byte.	0000 0000
Address	Bit	R/W	Description	Reset
0x218	7 - 0	R/W	Input Active Window definition: Horizontal Ending Pixel Position - Low Byte	1100 1111

Address	Bit	R/W	Description	Reset
0x219	7 - 4	R/W	Input Active Window definition: Horizontal Ending Pixel Position – High (Total 12 bits). This position is referenced to the rising edge of input HSYNC.	0010
	3	R/W	Reserved.	
	2 - 0	R/W	Input Active Window definition: Horizontal Starting Pixel Position - High (Total 11 bits) This position is referenced to the rising edge of input HSYNC.	000
*Note: The value written in this register does not come into effect until a register write to index 0x217 or 0x218 is followed.				
Address	Bit	R/W	Description	Reset
0x21A	7-0	R/W	Input Active Window definition: Odd Field Vertical Line Start Position - Low Byte	0001 0011
Address	Bit	R/W	Description	Reset
0x21B	7-0	R/W	Input Active Window definition: Even Field Vertical Line Start Position - Low Byte	0001 0011
Address	Bit	R/W	Description	Reset
0x21C	7-0	R/W	Input Active Window definition: Vertical Length - Low Byte	0000 0000
Address	Bit	R/W	Description	Reset
0x21D	7	R/W	Reserved.	0
	6 - 4	R/W	Input Active Window definition: Vertical Length - High (Total 11 bits)* The unit of this length is one input HSYNC.	011
	3 - 2	R/W	Input Active Window definition: Even Field Vertical Line Start Position - High (Total 10 bits)*. This position is referenced to the rising edge of input VSYNC.	00
	1 - 0	R/W	Input Active Window definition: Odd Field Vertical Line Start Position - High (Total 10 bits)*. This position is referenced to the rising edge of VSYNC.	00
*Note: When the Explicit-DE is not used (Register 0x211, bit 5), the input active window is defined by the above H-Active and V-Active registers.				

Address	Bit	R/W	Description	Reset
0x21E	7	R/W	Line Lock PLL output Clock Polarity	0
	6	R/W	Reserved	0
	5	R/W	GPIO[1] input/output selection. 1: Output (see 0x213 for data source). 0 : input	0
	4	R/W	GPIO[0] input/output selection. 1: Output (see 0x213 for data source). 0 : input	0
	3	R/W	Set IRQ Active Low	0
	2	R/W	*	0
	1 - 0	R/W	Line Lock PLL output Clock delay [1:0]	00
Address	Bit	R/W	Description	Reset
0x21F	7	R/W	Invert GPIO[1] output.	0
	6 - 5	R/W	Output source selection GPIO[1]. 00: Data written to bit 4, 01: VDLOSS, 10: HLOCK, 11: BW_ACTIVE	00
	4	R/W	Read: Shows the sampled input value of GPIO[1] Write: Holds the data that can be output to GPIO[1]	0
	3	R/W	Invert GPIO[0] output.	0
	2 - 1	R/W	Output source selection GPIO[0]. 00: Data written to bit 0, 01: FIELD, 10: HZ50, 11:IRQ	000
	0	R/W	Read: Shows the sampled input value from GPIO[0] Write: Holds the data that can be output to GPIO[0]	0

0x220 to 0x22F – Input Format Measurement Registers

Address	Bit	R/W	Description	Reset
0x220	7:0		Reserved	
Address	Bit	R/W	Description	Reset
0x221	7-0	R/W	Input Measurement Window definition: Horizontal Start - Low Byte	0010 0000
Address	Bit	R/W	Description	Reset
0x222	7-0	R/W	Input Measurement Window definition: Horizontal Stop - Low Byte	1111 1111
Address	Bit	R/W	Description	Reset
0x223	7-4	R/W	Input Measurement Window definition: Horizontal Stop - High three bits (Total 12 bits) This Horizontal Stop position if referenced to the rising edge of input HSYNC and the unit is one input pixel.	0001
	3		Reserved	0
	2-0	R/W	Input Measurement Window definition: Horizontal Start - High three bits (Total 11 bits) This Horizontal Start position if referenced to the rising edge of input HSYNC and the unit is one input pixel.	000
Address	Bit	R/W	Description	Reset
0x224	7-0	R/W	Input Measurement Window definition: Vertical Start - Low Byte	0010 0000
Address	Bit	R/W	Description	Reset
0x225	7-0	R/W	Input Measurement Window definition: Vertical Stop - Low Byte	1111 1010
Address	Bit	R/W	Description	Reset
0x226	7		Reserved	0
	6-4	R/W	Input Measurement Window definition: Vertical Stop - High three bits (Total 11 bits) This Vertical Stop position is referenced to the rising edge of input VSYNC and the unit is one input HSYNC.	000
	3		Reserved	0
	2-0	R/W	Input Measurement Window definition: Vertical Start - High three bits (Total 11 bits) This Vertical Start position is referenced to the rising edge of input VSYNC and the unit is one input HSYNC.	000
Address	Bit	R/W	Description	Reset
0x227	7-0	R	Result 0: Data port 0 to read Input Measurement Result (0X22B bits 7-4 specifies which result to read out)	0000 0000
Address	Bit	R/W	Description	Reset
0x228	7-0	R	Result 1: Data port 1 to read Input Measurement Result (0X22B bits 7-4 specifies which result to read out)	0000 0000
Address	Bit	R/W	Description	Reset
0x229	7-0	R	Result 2: Data port 2 to read Input Measurement Result (0X22B bits 7-4 specifies which result to read out)	0000 0000
Address	Bit	R/W	Description	Reset
0x22A	7-0	R	Result 3: Data port 3 to read Input Measurement Result (0X22B bits 7-4 specifies which result to read out)	0000 0000

Address	Bit	R/W	Description	Reset
0x22B	7 - 4	R/W	Select which measurement result to read out from 0x227~0x22A 0000: Phase Measurement Result - Blue (use Result 3-0 registers) 0001: Phase Measurement Result - Green (use Result 3-0 registers) 0010: Phase Measurement Result - Red (use Result 3-0 registers) 0011: Minimum Value (Result2: R, Result1: G, Result 0:B) 0100: Maximum Value (Result2: R, Result1: G, Result 0:B) 0101: VSYNC Period (Result3, 2) HSYNC Period (Result 1, 0) 0110: HSYNC Rise to HSYNC Fall Interval (Result 1, 0) and HSYNC Rise to HACTIVE Fall Interval (Result 3, 2). 0111: VSYNC pulse width (Result 1,0), Horizontal pixel counter value at the leading edge of VSYNC (Result 3, 2). 1000: Min Horizontal Active Starting Pixel (Results 1 & 0) Max Horizontal Active Starting Pixel (Results 3 & 2) 1001: Min Horizontal Active Ending Pixel (Results 1 & 0) Max Horizontal Active Ending Pixel (Results 3 & 2) 1010: Vertical Active Starting Line recorded with a. the first Horizontal Active Starting Pixel (Results 1 & 0) b. the first Horizontal Active Ending Pixel (Results 3 & 2) 1011: Vertical Active Ending Line recorded with a. the last Horizontal Active Starting Pixel (Results 1 & 0) b. the last Horizontal Active Ending Pixel (Results 3 & 2) 1100: Horizontal counter value when buffer read pointer starts to toggle. (Results 1 & 0) 1101: Luminance values. Minimum luminance (Result 0) Maximum luminance (Result 1) Average luminance (Result2) 1110: VSYNC Period measured with 27 MHz clock (Result 2, 1 & 0).	0000
	3 - 2	R/W	Field Select for Input Measurement 00: Odd field only 01: Even field only 1x: Disregard field	00
	1	R/W	Reserved.	0
	0	R/W	STARTM Start Input Measurement. This bit is self-cleared after the measurement is done.	0
Address	Bit	R/W	Description	Reset
0x22C	7	R/W	Use 27MHz clock for input HSYNC period measurement.	0
	6 - 4	R/W	Noise mask bits for each of the 3 LSB input signals.	000
	3 - 1	R/W	Error Tolerance before asserting "Change Detected" status 000: Exact match 001: Up to 4 counts 0 10: Up to 8 counts 011: Up to 16 counts 100: Up to 32 counts 101: Up to 64 counts 110: Up to 128 counts 111: Up to 256 counts.	000
	0	R/W	ENDET Enable Input VSYNC, HSYNC Period Change/Loss Detection. When this bit is set, the internal circuitry will perform new measurements. The new results are compared against the results retained in the registers obtained by the most recent "startm" measurement.	0
Address	Bit	R/W	Description	Reset
0x22D	7 - 4	R/W	Threshold value for input active region detection. Each increment increases the threshold value by 16.	0011
	3	R/W	Enable luminance measurement.	0
	2 - 1	R/W	Noise filter selection for luminance measurement.	000
	0	R/W	DE Measurement Enable.	0
Address	Bit	R/W	Description	Reset
0x22F	7 - 0		*	

0x230 to 0x23F – Scaling/Zoom Control

Address	Bit	R/W	Description	Reset
0x230	7 – 0	R/W	Horizontal (X-Direction) Scale Up Factor – Higher Fraction Byte (Coarse adjustment) 65536 * (Input Horizontal Active Pixel Number) / (Flat Panel Horizontal Active Pixel Number) Example: VGA 640x480 , Panel Resolution: 1024x768 65536 * 640 / 1024 = 40960 = 0A000h Example: Decoder 720x240, Panel Resolution: 1024x768 65536 * 720 / 1024 = 46080 = 0B400h	1011 0100
Address	Bit	R/W	Description	Reset
0x231	7 – 0	R/W	Horizontal (X-Direction) Scale Down Factor - Fraction Byte 128 * (Input Horizontal Active Pixel Number) / (Flat Panel Horizontal Active Pixel Number) Example: Decoder 720x240, Panel Resolution: 640x480 128 * 720 / 640 = 144 = 090h	1000 0000
Address	Bit	R/W	Description	Reset
0x232	7 – 0	R/W	Vertical (Y-Direction) Scale Up Factor – Higher Fraction Byte (Coarse adjustment) 65536 * (Input Vertical Active Pixel Number) / (Flat Panel Vertical Active Pixel Number) Example: VGA 640x480 , Panel Resolution: 1024x768 65536 * 480 / 768 = 40960 = 0A000h Example: Decoder 720x240, Panel Resolution: 1024x768 65536 * 240 / 768 = 20480 = 05000h	0101 0000
Address	Bit	R/W	Description	Reset
0x233	7	R/W	Enable Panorama / Water-glass scaling.	0
	6	R/W	1: Line doubling, 0: Normal vertical scaling	0
	5	R/W	1: Pixel doubling, 0: Normal horizontal scaling	0
	4	R/W	Set Zoom by-pass. When this bit is set, the Horizontal and Vertical scale up factors has no effects.	0
	3 - 2	R/W	Integer portion of Vertical (Y-Direction) Scale factor (Total 18 bits). For vertical scale up, maximum value is 0x10000. For vertical Y-direction scale down, the value should be larger than 0x100. Vertical Scale Factor < 0x10000 : Up scaling Vertical Scale Factor = 0x10000 : No scaling Vertical Scale Factor > 0x10000 : Down scaling The max vertical down scaling factor that the scaler can handle is 0x20000.	00
	1	R/W	Horizontal (X-Direction) Scale Down Factor – High bit (Total of 9 bits)	0
	0	R/W	Horizontal (X-Direction) Scale Up Factor – Integer portion bit (Total 17 bits)	0
Address	Bit	R/W	Description	Reset
0x234	7 - 0	R/W	Horizontal (X-Direction) Scale Up Offset This offset is used to adjust the initial value for the X-Direction scale up operation.	0000 0000
Address	Bit	R/W	Description	Reset
0x235	7 - 0	R/W	Vertical (Y-Direction) Scale Up Offset for Odd field This offset is used to adjust the initial value for the Y-Direction scale up operation.	1000 0000
Address	Bit	R/W	Description	Reset
0x236	7 - 0	R/W	Horizontal non-display pixel number applied to both left and right sides. This is useful when displaying 4:3 image on wide screen 16:9 panel. Example: A wide screen panel with 1024 horizontal pixels. If this register has a value of 100, the active horizontal display will be 824 pixels. Each side is "blacked" out by 100 pixels. This register also serves as the panorama horizontal width definition.	0000 0000
Address	Bit	R/W	Description	Reset
0x237	7	R/W	Line buffer SRAMs' CE are always active.	0000 0000
	6 - 2	R/W	*	0000 0000
	1 - 0	R/W	High 2 bits of 0x246 register.	0000 0000
Address	Bit	R/W	Description	Reset
0x238	7 – 0	R/W	Horizontal scale at the side of display in panorama scaling mode.	0000 0000
Address	Bit	R/W	Description	Reset
0x239	7 - 0	R/W	Horizontal (X-Direction) Scale Up Factor – Lower Fraction Byte (Fine adjustment)	0000 0000

Address	Bit	R/W	Description	Reset
0x23A	7 - 0	R/W	Vertical (Y-Direction) Scale Up Factor – Lower Fraction Byte (Fine adjustment)	0000 0000
Address	Bit	R/W	Description	Reset
0x23B	7 - 0	R/W	Vertical (Y-Direction) Scale Up Offset for Even field This offset is used to adjust the initial value for the Y-Direction scale up operation.	0000 0000

0x240 to 0x26F – Image Adjustment

Address	Bit	R/W	Description	Reset
0x240	7	R/W	*	0
	6	R/W	There are 2 sets of registers for index 0x241 ~ 0x246. 0: Select the 1st set, R/G/B Contrast and R Brightness 1: Select the 2nd set, Y/Cb/Cr Contrast and Y Brightness	0
	5 - 0	R/W	Hue Adjustment for Main path. These bits control the color hue. The range is +45 degrees to –45 degrees in 1.4 degree increments. 0 degrees is the default (xx10 0000)	10 0000
Address	Bit	R/W	Description	Reset
0x241	7 - 0	R/W	Red (or Y) Contrast Adjustment for Main path 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x242	7 - 0	R/W	Green (or Cb) Contrast Adjustment for Main path 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x243	7 - 0	R/W	Blue (or Cr) Contrast Adjustment for Main path 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x244	7 - 0	R/W	Red (or Y) Brightness Adjustment for Main path 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x245	7 - 0	R/W	Green Brightness Adjustment for Main path 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x246	7 - 0	R/W	Blue Brightness Adjustment for Main path 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x247	7 - 4	R/W	Coring function for sharpness control of Main path.	0011
	3 - 0	R/W	Sharpness Adjustment for Main path	1111
Address	Bit	R/W	Description	Reset
0x248	7	R/W	Main path Sharpness frequency select. 0 = Low freq. 1 = High freq.	0
	6	R/W	Reserved.	000
	5 - 4	R/W	Main path YNR.	000
	3	R/W	Reserved.	000
	2 - 0	R/W	Main path Hflt.	000
Address	Bit	R/W	Description	Reset
0x249	7	R/W	*	0
	6	R/W	There are 2 sets of registers for index 71 ~ 76. 0: Select the 1st set, R/G/B Contrast and R Brightness 1: Select the 2nd set, Y/Cb/Cr Contrast and Y Brightness	0
	5 - 0	R/W	Hue Adjustment for Sub path. These bits control the color hue. The range is +45 degrees to –45 degrees in 1.4 degree increments. 0 degrees is the default (xx10 0000)	10 0000

Address	Bit	R/W	Description	Reset
0x24A	7 - 0	R/W	Red (or Y) Contrast Adjustment for Sub path 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x24B	7 - 0	R/W	Green (or Cb) Contrast Adjustment for Sub path 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x24C	7 - 0	R/W	Blue (or Cr) Contrast Adjustment for Sub path. 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x24D	7 - 0	R/W	Red (or Y) Brightness Adjustment for Sub path. 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x24E	7 - 0	R/W	Green Brightness Adjustment for Sub path. 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x24F	7 - 0	R/W	Blue Brightness Adjustment for Sub path 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x250	7 - 4	R/W	Coring function for sharpness control of Sub path.	0011
	3 - 0	R/W	Sharpness Adjustment for Sub path	1111
Address	Bit	R/W	Description	Reset
0x251	7	R/W	Sub path Sharpness frequency select. 0 = Low freq. 1 = High freq.	0
	6	R/W	Reserved.	000
	5 - 4	R/W	Sub path YNR.	000
	3	R/W	Reserved.	000
	2 - 0	R/W	Sub path Hflt.	000
Address	Bit	R/W	Description	Reset
0x252	7 - 4	R/W	Edge enhancement parameter	0100
	3	R/W	Disable edge enhancement.	0
	2 - 0	R/W	Index for registers sharing the address space 0x25A	000
Address	Bit	R/W	Description	Reset
0x253 (252[2:0]=0)	7 - 0	R/W	2D edge enhancement register threshold #0	0011 0000
0x253 (252[2:0]=1)	7 - 0	R/W	2D edge enhancement register threshold #1	0011 0000
0x253 (252[2:0]=2)	7 - 0	R/W	2D edge enhancement register threshold #2	0011 0000
0x253 (252[2:0]=3)	7 - 0	R/W	2D edge enhancement register threshold #3	0000 0000
0x253 (252[2:0]=4)	7 - 0	R/W	2D edge enhancement register threshold #4	0000 0000
Address	Bit	R/W	Description	Reset
0x254	7 - 4	R/W	Reserved.	0000
	3 - 0	R/W		0100

Address	Bit	R/W	Description	Reset
0x255	7	R/W	Test BW. Should be 0 for normal operation.	0
	6	R/W	Reserved	0
	5	R/W	Black level selection. 0: 0 1: 16d	0
	4	R/W	White level selection. 0: 235d 1: 255d	1
	3	R/W	Reserved	1
	2	R/W	Reserved	1
	1	R/W	Reserved.	00
	0	R/W	1: BW stretch enable, 0: BW disable	0
Address	Bit	R/W	Description	Reset
0x256	7 - 0	R/W	Black/White stretch line start for detection window, lower 8 bits (total 10 bits).	0000 1000
Address	Bit	R/W	Description	Reset
0x257	7 - 0	R/W	Black/White stretch line end for detection window, lower 8 bits (total 10 bits).	1111 0110
Address	Bit	R/W	Description	Reset
0x258	7 - 4	R/W	Reserved.	0000
	3 - 2	R/W	Black/White stretch line end for detection window, upper 2 bits.	10
	1 - 0	R/W	Black/White stretch line startfor detection window, upper 2 bits.	00
Address	Bit	R/W	Description	Reset
0x259	7 - 0	R/W	BWHDLY, Black/White stretc horizontal distance from Start/End pixel of HACTIVE.	0001 0000
Address	Bit	R/W	Description	Reset
0x25A	7 - 6	R/W	Reserved	00
	5 - 0	R/W	Y Min/Max Horizontal filter gain.	00 1011
Address	Bit	R/W	Description	Reset
0x25B	7 - 0	R/W	Tilt point for black stretch.	0110 0111
Address	Bit	R/W	Description	Reset
0x25C	7 - 0	R/W	Tilt point for white stretch.	1001 0100
Address	Bit	R/W	Description	Reset
0x25D	7 - 0	R/W	Black stretch Limit	0010 1010
Address	Bit	R/W	Description	Reset
0x25E	7 - 0	R/W	White stretch Limit	1101 0000
Address	Bit	R/W	Description	Reset
0x25F	7 - 0	R/W	See PIP register explanation	1100 1010
Address	Bit	R/W	Description	Reset
0x260	7	R/W	Reserved.	0
	6 - 0	R/W	Black/White Stretch Field recursive filter gain.	000 0010
Address	Bit	R/W	Description	Reset
0x261	7	R/W	1: MPIP write height reduction enable, 0: Normal operation (write and read height are same)	0
	6 - 0	R/W	MPIP write height reduction amount	0000000
Address	Bit	R/W	Description	Reset
0x262	7 - 0	R/W	Reserved.	0001 1000
Address	Bit	R/W	Description	Reset
0x263	7 - 0	R/W	Color Enhancement Center Color phase for color 1. The range for center color phase is –180° ~ + 180°	3Dh
Address	Bit	R/W	Description	Reset
0x264	7 - 0	R/W	Color Enhancement Center Color phase for color 2. The range for center color phase is –180° ~ + 180°	C3h
Address	Bit	R/W	Description	Reset
0x265	7 - 0	R/W	Color Enhancement Center Color phase for color 3. The range for center color phase is –180° ~ + 180°	FCh
Address	Bit	R/W	Description	Reset
0x266	7	R/W	1: Color Enhancement Enable, 0: Disable	0

Address	Bit	R/W	Description	Reset
0x255	7	R/W	Test BW. Should be 0 for normal operation.	0
	6	R/W	Reserved	0
	5	R/W	Black level selection. 0: 0 1: 16d	0
	4	R/W	White level selection. 0: 235d 1: 255d	1
	3	R/W	Reserved	1
	2	R/W	Reserved	1
	1	R/W	Reserved.	00
	0	R/W	1: BW stretch enable, 0: BW disable	0
Address	Bit	R/W	Description	Reset
0x256	7 - 0	R/W	Black/White stretch line start for detection window, lower 8 bits (total 10 bits).	0000 1000
Address	Bit	R/W	Description	Reset
0x257	7 - 0	R/W	Black/White stretch line end for detection window, lower 8 bits (total 10 bits).	1111 0110
Address	Bit	R/W	Description	Reset
	6 - 5	R/W	Color Enhancement Gain Spread Range for color 1 00 : no enhance 01 : -8° ~ +8° of center color phase 10 : -16° ~ +16° of center color phase 11 : -32° ~ + 32° of center color phase	00
	4 - 0	R/W	Color Enhancement Gain for color 1. The minimum Gain value is 00000 and maximum is 11111 from 0 to 0.484 with 31 step of 1/64.	0h
Address	Bit	R/W	Description	Reset
0x267	7	R/W	Reserved	
	6 - 5	R/W	Color Enhancement Gain Spread Range for color 2	00
	4 - 0	R/W	Color Enhancement Gain for color 2	0h
Address	Bit	R/W	Description	Reset
0x268	7	R/W	Reserved	
	6 - 5	R/W	Color Enhancement Gain Spread Range for color 3	00
	4 - 0	R/W	Color Enhancement Gain for color 3	0h

0x270 to 0x28F – DISPLAY CONTROL

Address	Bit	R/W	Description	Reset
0x270	7	R/W	Set Double Pixel output to flat panel. 0: Single Pixel	0
	6	R/W	Set FPDE Active High 0: Active Low	1
	5	R/W	Set FPHS Active High 0: Active Low	0
	4	R/W	Set FPVS Active High 0: Active Low	0
	3	R/W	Invert FPCLK polarity 0: Output signals to flat panel (FPVS, FPHS, … etc.) are referenced to the falling edge of FPCLK.	0
	2	R/W	Reverse the pixel order on panel data bus for dual pixel output. 0: First pixel is out on FPR0/FPG0/FPB0. 1: First pixel is out on FPR1/FPG1/FPB1	0
	1	R/W	Reverse the bit order on panel data bus. 0: MSB is on FPR0[7], FPR1[7], FPG0[7], FPG1[7], FPB0[7], and FPB1[7]. 1: MSB is on FPR0[0], FPR1[0], FPG0[0], FPG1[0], FPB0[0], and FPB1[0].	0
	0	R/W	Set this bit to 1 making FPCLK become inactive during vertical blanking time.	0
Address	Bit	R/W	Description	Reset
0x271	7	R/W	TCON output. 1: Set panel output pins to TCON interface signals.	00
	6	R/W	When this bit is set, the internal circuitry uses the programmed value of index B6[3:0] and index B2[7:0] as the FPHS period disregarding the setting of "Auto Calculation", bit 1 of index BE.	0
	5	R/W	DE mode selection. 1: FPVS and FPHS are forced to inactive state.	0
	4	R/W	FP data outputs shift down 2 bits. When set, FPR0, FPR1, FPG0, FPG1, FPB0, FPB1 bus signals are shifted down by 2 bits.	0
	3	R/W	Tri-state all the output signals to flat panel.	0
	2 - 0	R/W	Panel clock FPCLK delay time selection. 000: No delay time inserted. Each increment increases the delay by 1 ns.	000
Address	Bit	R/W	Description	Reset
0x272	7 - 0	R/W	FPHS Period - Low Byte	0011 1010
Address	Bit	R/W	Description	Reset
0x273	7 - 0	R/W	FPHS Active Pulse Width This register is usually filled in with the minimum FPHS pulse width requirement from the flat panel specification	0001 0000
Address	Bit	R/W	Description	Reset
0x274	7 - 0	R/W	Flat Panel Horizontal Back Porch Width --- The duration from the trailing edge of FPHS to the leading edge of FPDE. This register is usually filled in with the minimum horizontal back porch requirement from the flat panel specification.	00011011
Address	Bit	R/W	Description	Reset
0x275	7 - 0	R/W	FPDE Horizontal Active Length	0000 0000

Address	Bit	R/W	Description	Reset
0x276	7 - 4	R/W	FPDE Horizontal Active Length – High three bits (Total 11 bits) This horizontal active length is equivalent to the panel horizontal resolution. For example, the horizontal resolution of an XGA panel is 1024.	100
	3 - 0	R/W	FPHS Period – High three bits (Total 12 bits) The following formula gives the correct number to fill in for FPHS period. FPHS_Period = *F*_pllcki / (*F*_ihsync * VSUR) Where *F*_pllcki is the frequency of PCLK, *F*_ihsync is the frequency of input HSYNC, and VSUR is the vertical scale up ratio. VSUR = (Panel Vertical Resolution) / (Input Vertical Resolution) Example: Input is VGA with HSYNC frequency 31.5KHz with 60 Hz refresh rate to be displayed on an XGA panel. VSUR = 768/480 = 1.6 Choose *F*_pllcki = 69 MHz FPHS_Period = 69000000 / (31500 * 1.6) = 1369.05 → 1369 = 559h	0101

Note: The unit for Index 0x272 through 0x276 is one panel pixel clock, which is either the output of internal PLL or PCLK.
The FPHS Period should be larger than the sum of 1) FPHS Active Pulse Width, 2) FPHS Back Porch Width, and 3) FPDE Horizontal Active Length.

Address	Bit	R/W	Description	Reset
0x277	7 - 0	R/W	FPVS Period - Low Byte	0010 0110
Address	Bit	R/W	Description	Reset
0x278	7 - 0	R/W	FPVS Active Pulse Width The unit of this pulse width is one FPHS. This register is usually filled in with the minimum FPVS pulse width requirement from the flat panel specification.	0000 0110
Address	Bit	R/W	Description	Reset
0x279	7 - 0	R/W	Flat Panel Vertical Back Porch Width The unit of this pulse width is one FPHS. The following formula gives the correct number to fill in for FPVS back porch. FPVS_Back_Porch = (VAS–VSYNC_pw+2)* VSUR–FPVS_Pulse_Width Where VAS is the input Vertical active starting line number, VSYNC_pw is the input VSYNC pulse width, VSUR is the Vertical Scale Up ratio. VSUR = (Panel Vertical Resolution) / (Input Vertical Resolution)	0001 1111
Address	Bit	R/W	Description	Reset
0x27A	7 - 0	R/W	Flat Panel Vertical Active Length - Low Byte	0000 0000
Address	Bit	R/W	Description	Reset
0x27B	7	R/W	Early start. Start to output data earlier in non auto calculation mode.	0
	6 - 4	R/W	Flat Panel Vertical Active Length - High three bits (Total 11 bits) The unit of this active length is one FPHS This vertical active length is equivalent to the panel vertical resolution. For example, the vertical resolution of an XGA panel is 768.	011
	3		Reserved	0
	2 - 0	R/W	FPVS Period – High three bits (Total 11 bits) The unit of this period is one FPHS.	011

Note: The unit for Index 0x277 through 0x27B is one FPHS, i.e. whenever there is an active FPHS, the count is incremented by 1. The FPVS Period should be larger than the sum of 1) FPVS Active Pulse Width, 2) FPVS Back Porch Width, and 3) Flat Panel Vertical Active Length.

Note: The value written in this register does not come into effect until it is followed by a register write to index 0x277 or 0x27A.

Address	Bit	R/W	Description	Reset
0x27C	7		Reserved	0
	6 - 4	R/W	Dither Option Code "010" is recommended for 6:6:6 output	000
	3	R/W	Reserved	0
	2 - 0	R/W	Dither Output Format Selection "001" is recommended for 6:6:6 output	000

Table 6 Dither Output Selection and Calculations

Dither Output Format Selection	Flat Panel RGB Bit Format Output	Dither Option Code	Input LSBs Used in Dither Calculation	Dither Method
000	8:8:8	**000**	n/a	none
001	6:6:6	**001**	(3) (3) (3)	2x2
		010	(3,2) (3,2)(3,2)	2x2
		011	(3,2,1) (3,2,1)(3,2,1)	2x2
		100	(3,2,1,0) (3,2,1,0)(3,2,1,0)	4x4
010	5:6:5	**001**	(4) (3) (4)	2x2
		010	(4,3) (3,2) (4,3)	2x2
		011	(4,3,2) (3,2) (4,3,2)	2x2
		100	4,3,2,1) (3,2,1) (4,3,2,1)	4x4
011	5:5:5	**001**	(4) (4) (4)	2x2
		010	(4,3) (4,3) (4,3)	2x2
		011	(4,3,2) (4,3,2) (4,3,2)	2x2
		100	(4,3,2,1) (4,3,2,1) (4,3,2,1)	4x4
100	4:4:4	**001**	(5) (5) (5)	2x2
		010	(5,4) (5,4) (5,4)	2x2
		011	(5,4,3) (5,4,3) (5,4,3)	2x2
		100	(5,4,3,2) (5,4,3,2) (5,4,3,2)	4x4
101	3:3:3	**001**	(6) (6) (6)	2x2
		010	(6,5) (6,5) (6,5)	2x2
		011	(6,5,4) (6,5,4) (6,5,4)	2x2
		100	(6,5,4,3) (6,5,4,3) (6,5,4,3)	4x4
110	3:3:2	**001**	(6) (6) (7)	2x2
		010	(6,5) (6,5) (7,6)	2x2
		011	(6,5,4) (6,5,4) (6,5,4)	2x2
		100	(6,5,4,3) (6,5,4,3) (7,6,5,4)	4x4

Address	Bit	R/W	Description	Reset
0x27D	7 - 0	R/W	Output Vsync delay from Input Vsync	0000 1000
Address	Bit	R/W	Description	Reset
0x27E	7	R/W	Force long. In auto calculation with this bit set, the FPHS period assumes the next higher integer value if the calculated FPHS contains fractional part.	0
	6	R/W	Force short. In auto calculation with is bit set, the FPHS period assumes the integer part; i.e. the fractional part of the calculated FPHS period is discarded.	0
	5	R/W	Tri-State PWM pin.	0
	4	R/W	PWM polarity. 1: Active low	0
	3	R/W	When set, the input "HACTIVE" or "DE" is forced to inactive if either VSYNC or HSYNC is active.	0
	2	R/W	Force into free run mode.	0
	1	R/W	Enable auto calculation. When this bit is set, an internal circuitry calculates the optimum FPHS period, and then adjusts the FPHS period dynamically so that for one vsync (FPVS) period it has integer multiples of FPHS. The internal circuitry also adjust the FPHS active position to minimize the line buffer overflow/underflow.	0
	0	R/W	When this bit is set, the input VSYNC is delayed by the amount specified by index 0x27D in the unit of input HSYNC. The regular meaning of index 0x27D -- "Output VSYNC delay from Input VSYNC" is fixed at 2.	0

Address	Bit	R/W	Description	Reset
0x27F	7 - 6	R/W	Display single field on flat panel. 0x : Function disabled. 10 : Display odd field. 11 : Display even field.	00
	5	R/W	When set the field signal is reversed in the auto calculation circuitry.	000
	4	R/W	Select different vertical sync source in single field input.	000
	3	R/W	No even field initialization	0
	2 - 0	R/W	Even field delay. 001= +1, 010= +2, … 101= +5, 110= -1, 111= -2	000
Address	Bit	R/W	Description	Reset
0x280	7	R/W	Bits 8 to 1 of 13 bit counter – 0x282(3-0), 0x280(7-0)	
Address	Bit	R/W	Description	Reset
0x281	7	R/W	Bits 8 to 1 of 13 bit counter – 0x282(7-4), 0x281(7-0)	
Address	Bit	R/W	Description	Reset
0x282	7 - 4	R/W	Upper 4 bits (bits 13 to 9) of 13 bit counter – 0x282(7-4), 0x281(7-0) For non-Free-Run mode, this specifies the upper 12-bits of the initial value of a 13-bit counter for the even field. For Free-Run with Calibrate bit set, this specifies the value for the vertical line counter to load at the falling edge of input VSYNC.	
	3 - 0	R/W	Upper 4 bits (bits 13 to 9) of 13 bit counter – 0x282(3-0), 0x280(7-0) For non-Free-Run mode, this specifies the upper 12-bits of the initial value of a 13-bit counter for the odd field. For Free-Run with Calibrate bit set, this specifies the value for pixel counter to load at the falling edge of input VSYNC.	0
Address	Bit	R/W	Description	Reset
0x283	7 - 6	R/W	Even field vertical start point adjustment. 00 : Even field start with the same line count specified in 0x27D as odd field. 01 : Even field start with one extra line count specified in 0x27D. 10 : Even field start with one less line count specified in 0x27D.	0
	5 - 0	R/W	Number of lines to be black out from top and the bottom of the display.	00 0000
Address	Bit	R/W	Description	Reset
0x284	7	R/W	PWM clock selection 0: 27 MHz (XTAL27I input frequency) 1: 27/2 MHz	0
	6 - 0	R/W	Positive pulse width of the PWM. If this register has an “N” value, the positive pulse width duration is “N+1” PWM clocks.	100 0000
Address	Bit	R/W	Description	Reset
0x285	7 – 0	R/W	Reserved	0000 0000
Address	Bit	R/W	Description	Reset
0x286	7 – 0	R/W	Reserved	
Address	Bit	R/W	Description	Reset
0x287	7	R/W	0: Dual output selection lower 24 of 48 bits 1: Dual output selection upper 24 of 48 bits	0
	6 - 0	R/W	Reserved	00h

0x2A0 to 0x2AF – Memory Control

Address	Bit	R/W	Description	Reset
0x2A0	7	R/W	Memory read phase control.	0
	6-4	R/W	This is for the control of clock phase of memory clock output.	0
	3	R/W	nomcst	0
	2	R/W	Test Enable for Memory Controller.	0
	1-0	R/W	Memory configuration type.	10
Address	Bit	R/W	Description	Reset
0x2A1	7-0	R/W	This is for the refresh request timing setting. The values that written in registers uses to calculate the refresh request period.	07h
Address	Bit	R/W	Description	Reset
0x2A2	7-0	R/W	This is for the control of the RAS max timing setting.	20h
Address	Bit	R/W	Description	Reset
0x2A3	7-4	R/W	RAS Pre-charge time for memory operation.	0010
	3-0	R/W	RAS to CAS delay time for memory operation.	0010
Address	Bit	R/W	Description	Reset
0x2A4	7	R/W	This bit indicates bit21 of the address.	0
	6-4	R/W	*	0
	3-0	R/W	Refresh back time for memory operation.	0111
Address	Bit	R/W	Description	Reset
0x2A5	7	R/W	*	0
	6-4	R/W	Data read time adjustor based on memory clock period.	100
	3-0	R/W	Minimum time for mode register setting.	0011
Address	Bit	R/W	Description	Reset
0x2A6	7	R/W	Reserved.	0
	6-4	R/W	Data Delay	001
	3	R/W	Reserved.	0
	2-0	R/W	CAS Latency timing for mode register setting.	011
Address	Bit	R/W	Description	Reset
0x2A7	7	R/W	*	0
	6	R/W	*	0
	5	R/W	*	0
	4	R/W	*	0
	3	R/W	*	0
	2	R/W	*	0
	1-0	R/W	*	0

0x2AE to 0x2C9 – PIP Control

Address	Bit	R/W	Description	Reset
0x25F	7	R/W	1: PIP down scaler offset enable (Interlace input), 0: offset disabled (Progressive input)	0
	6 - 0	R/W	PIP down scaler offset	
Address	Bit	R/W	Description	Reset
0x2AE	7 - 0	R/W	PIP horizontal position offset adjustment	20h
Address	Bit	R/W	Description	Reset
0x2AF	7 - 0	R/W	PIP vertical position offset adjustment	2Ch
Address	Bit	R/W	Description	Reset
0x2B0	7 - 0	R/W	Horizontal input cropping start[7:0]. These bits indicate the start point of the cropping window of the PIP data which is going to be written into memory.	10h
Address	Bit	R/W	Description	Reset
0x2B1	7 - 0	R/W	Horizontal input cropping window width[7:0]. These bits indicate the width of the cropping window of the PIP data which is going to be written into memory.	60h
Address	Bit	R/W	Description	Reset
0x2B2	7	R/W	1: Down scaler pre-filter manual selection enable. 0: Auto selection (default)	00
	6 - 4	R/W	Horizontal input cropping window width[10:8]. These bits indicate the width of the cropping window of the PIP data which is going to be written into memory.	010
	3 – 2	R/W	Down scaler pre-filter manual selection. 0: No filter, 1: Weak filter, 2: Strong filter, 3: Medium filter	00
	1 - 0	R/W	Horizontal input cropping start[9:8]. These bits indicate the start point of the cropping window of the PIP data which is going to be written into memory.	00
Address	Bit	R/W	Description	Reset
0x2B3	7 - 0	R/W	Vertical input cropping start[7:0]. These bits indicate the start point of the cropping window of the PIP data which is going to be written into memory.	02h
Address	Bit	R/W	Description	Reset
0x2B4	7 - 0	R/W	Vertical input cropping window height[7:0]. These bits indicate the height of the cropping window of the PIP data which is going to be written into memory.	E0h
Address	Bit	R/W	Description	Reset
0x2B5	7	R/W	Vertical input cropping start[8].	0
	6 - 4	R/W	Vertical input cropping window height[10:8].	000
	3 - 2	R/W	Even field offset for the cropping window.	00
	1 - 0	R/W	Odd field offset for the cropping window.	00
Address	Bit	R/W	Description	Reset
0x2B6	7 - 0	R/W	PIP horizontal down scaling ratio [7:0]. 100h for no down scaling.	00h
Address	Bit	R/W	Description	Reset
0x2B7	7 - 0	R/W	PIP vertical down scaling ratio [7:0]. 100h for no down scaling	00h
Address	Bit	R/W	Description	Reset
0x2B8	7 - 4	R/W	PIP vertical down scaling ratio [11:8].	0001
	3 - 0	R/W	PIP horizontal down scaling ratio [11:8].	0001
Address	Bit	R/W	Description	Reset
0x2B9	7 - 0	R/W	PIP window write buffer base address. It defines start address of PIP memory area.	00h
Address	Bit	R/W	Description	Reset
0x2BA	7 - 0	R/W	PIP window write width[7:0]. These bits indicate the width of the PIP window written into the memory.	30h
Address	Bit	R/W	Description	Reset
0x2BB	7 - 0	R/W	PIP window write height[7:0]. These bits indicate the height of the PIP window written into the memory.	70h

Address	Bit	R/W	Description	Reset
0x2BC	7	R/W	1 : PIP window write enable. When disabled read-out image will freeze.	0
	6	R/W	Write Data Color Phase control.	0
	5	R/W	Reserved	0
	4	R/W	Reserved	0
	3	R/W	PIP window write height[8].	0
	2 - 0	R/W	PIP window write width[10:8]. These bits indicate the width of the PIP window written into the memory. Maximum width is 400h.	00
Address	Bit	R/W	Description	Reset
0x2BD	7	R/W	1 : PIP window read enable.	0
	6	R/W	1: PIP write power down (image will freeze), 0: Normal	0
	5	R/W	PIP mode enable.	0
	4	R/W	1: PIP blending single field mode, 0: Normal	0
	3	R/W	PIP read buffer field polarity.	0
	2	R/W	1: Pixel doubling when up scaling, 0: Normal.	0
	1	R/W	Reserved.	0
	0	R/W	1: Force Black, 0: Normal.	0
Address	Bit	R/W	Description	Reset
0x2BE	7 - 0	R/W	PIP horizontal Up scaling ratio [7:0]. 800h for no up scaling.	00h
Address	Bit	R/W	Description	Reset
0x2BF	7 - 0	R/W	PIP vertical Up scaling ratio [7:0]. 800h for no up scaling.	00h
Address	Bit	R/W	Description	Reset
0x2C0	7 - 4	R/W	PIP vertical Up scaling ratio [11:8].	1000
	3 - 0	R/W	PIP horizontal Up scaling ratio [11:8].	1000
Address	Bit	R/W	Description	Reset
0x2C1	7 - 0	R/W	PIP Window position base x start[7:0]. These bits indicate the origin of the PIP Window.	80h
Address	Bit	R/W	Description	Reset
0x2C2	7 - 0	R/W	PIP Window position base y start[7:0]. These bits indicate the origin of the PIP Window.	80h
Address	Bit	R/W	Description	Reset
0x2C3	7	R/W	1: PIP clock inverse, 0: Normal.	0
	6 – 4	R/W	PIP Window position base y start[10:8]. These bits indicate the origin of the PIP Window.	1h
	3 - 0	R/W	PIP Window position base x start[11:8]. These bits indicate the origin of the PIP Window.	2h
Address	Bit	R/W	Description	Reset
0x2C4	7 – 4	R/W	PIP Window position base y start offset. These bits indicate the base position of the PIP Window.	2h
	3 - 0	R/W	PIP Window position base x start offset. These bits indicate the base position of the PIP Window.	Ch
Address	Bit	R/W	Description	Reset
0x2C5	7 – 0	R/W	PIP Window width[7:0]. These bits indicate the display width of the PIP Window.	30h
Address	Bit	R/W	Description	Reset
0x2C6	7 – 0	R/W	PIP Window height[7:0]. These bits indicate the display height of the PIP Window.	E0h
Address	Bit	R/W	Description	Reset
0x2C7	7	R/W	PIP Window Color Phase Control for 16 to 24 Conversion.	0
	6 – 4	R/W	PIP Window height[10:8]. These bits indicate the display height of the PIP Window.	0h
	3 – 0	R/W	PIP Window width[11:8]. These bits indicate the display width of the PIP Window.	1h
Address	Bit	R/W	Description	Reset
0x2C8	7 - 0	R/W	MPIP frame horizontal position offset adjustment	2Ch
Address	Bit	R/W	Description	Reset
0x2C9	7 - 0	R/W	MPIP frame vertical position offset adjustment	2Eh

0x2CA to 0x2EC – MPIP Control Registers

Address	Bit	R/W	Description	Reset
0x2CA	7 - 0	R/W	Horizontal input cropping start[7:0]. These bits indicate the start point of the cropping window of the MPIP data which is going to be written into memory.	10h
Address	Bit	R/W	Description	Reset
0x2CB	7 - 0	R/W	Horizontal input cropping window width[7:0]. These bits indicate the width of the cropping window of the MPIP data which is going to be written into memory.	60h
Address	Bit	R/W	Description	Reset
0x2CC	7	R/W	1: Down scaler pre-filter manual selection enable. 0: Auto selection (default)	00
	6 - 4	R/W	Horizontal input cropping window width[10:8]. These bits indicate the width of the cropping window of the MPIP data which is going to be written into memory.	010
	3 – 2	R/W	Down scaler pre-filter manual selection. 0: No filter, 1: Weak filter, 2: Strong filter, 3: Medium filter	00
	1 - 0	R/W	Horizontal input cropping start[9:8]. These bits indicate the start point of the cropping window of the MPIP data which is going to be written into memory.	00
Address	Bit	R/W	Description	Reset
0x2CD	7 - 0	R/W	Vertical input cropping start[7:0]. These bits indicate the start point of the cropping window of the MPIP data which is going to be written into memory.	02h
Address	Bit	R/W	Description	Reset
0x2CE	7 - 0	R/W	Vertical input cropping window height[7:0]. These bits indicate the height of the cropping window of the MPIP data which is going to be written into memory.	E0h
Address	Bit	R/W	Description	Reset
0x2CF	7	R/W	Vertical input cropping start[8].	0
	6 - 4	R/W	Vertical input cropping window height[10:8].	000
	3 - 2	R/W	Even field offset for the cropping window.	00
	1 - 0	R/W	Odd field offset for the cropping window.	00
Address	Bit	R/W	Description	Reset
0x2D0	7 - 0	R/W	MPIP horizontal down scaling ratio [7:0]. 100h for no down scaling.	00h
Address	Bit	R/W	Description	Reset
0x2D1	7 - 0	R/W	MPIP vertical down down scaling ratio [7:0]. 100h for no down scaling.	00h
Address	Bit	R/W	Description	Reset
0x2D2	7 - 4	R/W	MPIP vertical down down scaling ratio [11:8].	0001
	3 - 0	R/W	MPIP horizontal down down scaling ratio [11:8].	0001
Address	Bit	R/W	Description	Reset
0x2D3	7 - 0	R/W	MPIP window write buffer base address. It defines start address of MPIP memory area	00h
Address	Bit	R/W	Description	Reset
0x2D4	7 - 0	R/W	MPIP window write width[7:0]. These bits indicate the width of the single MPIP sub-window.	30h
Address	Bit	R/W	Description	Reset
0x2D5	7 - 0	R/W	MPIP window write height[7:0]. These bits indicate the height of the single MPIP sub-window.	70h
Address	Bit	R/W	Description	Reset
0x2D6	7	R/W	1 : MPIP window write enable. When disabled read-out image will freeze..	0
	6	R/W	Write Data Color Phase control.	0
	5	R/W	Reserved	0
	4	R/W	Reserved	0
	3	R/W	MPIP window write height[8].	0
	2 - 0	R/W	MPIP window write width[10:8]. These bits indicate the width of the MPIP window written into the memory. Maximum width is 400h.	00

Address	Bit	R/W	Description	Reset
0x2D7	7	R/W	MPIP window read enable.	0
	6	R/W	1: MPIP write power down (Live window will freeze), 0: Normal	0
	5	R/W	MPIP mode enable.	0
	4	R/W	Reserved.	0
	3	R/W	MPIP read buffer field polarity.	0
	2	R/W	1: Pixel doubling when up scaling, 0: Normal.	0
	1	R/W	Reserved.	0
	0	R/W	1: Force Black, 0: Normal.	0
Address	Bit	R/W	Description	Reset
0x2D8	7 - 0	R/W	MPIP horizontal Up scaling ratio [7:0]. 800h for no up scaling. Should not be changed.	00h
Address	Bit	R/W	Description	Reset
0x2D9	7 - 0	R/W	MPIP vertical Up scaling ratio [7:0]. 800h for no up scaling. Should not be changed.	00h
Address	Bit	R/W	Description	Reset
0x2DA	7 - 4	R/W	MPIP vertical Up scaling ratio [11:8]. Should not be changed.	1000
	3 - 0	R/W	MPIP horizontal Up scaling ratio [11:8]. Should not be changed.	1000
Address	Bit	R/W	Description	Reset
0x2DB	7 - 0	R/W	MPIP image position base x start[7:0]. These bits indicate the origin of the MPIP Window.	20h
Address	Bit	R/W	Description	Reset
0x2DC	7 - 0	R/W	MPIP image position base y start[7:0]. These bits indicate the origin of the MPIP Window.	2Ch
Address	Bit	R/W	Description	Reset
0x2DD	7 - 0	R/W	PIP vertical scaling offset.	80h
Address	Bit	R/W	Description	Reset
0x2DE	7 – 4	R/W	MPIP Window position base y start offset. These bits indicate the base position of the MPIP Window.	0h
	3 - 0	R/W	MPIP Window position base x start offset. These bits indicate the base position of the MPIP Window.	0h
Address	Bit	R/W	Description	Reset
0x2DF	7 – 0	R/W	MPIP Window width[7:0]. These bits indicate the display width of the combined MPIP Windows.	00h
Address	Bit	R/W	Description	Reset
0x2E0	7 – 0	R/W	MPIP Window height[7:0]. These bits indicate the display height of the combined MPIP Windows.	00h
Address	Bit	R/W	Description	Reset
0x2E1	7	R/W	1: MPIP clock inverse, 0: Normal	0
	6 – 4	R/W	MPIP Window height[10:8]. These bits indicate the display height of the combined MPIP Windows.	0h
	3 – 0	R/W	MPIP Window width[11:8]. These bits indicate the display width of the combined MPIP Windows.	0h
Address	Bit	R/W	Description	Reset
0x2E2	7	R/W	MPIP Window Color Phase Control for 16 to 24 Conversion.	0
	6 - 1	R/W	Reserved	00h
	0	R/W	1 : MPIP Image memory initialization enable. (Color is defined by 0x2E5). After initialization, should be return to 0 for normal operation.	0
Address	Bit	R/W	Description	Reset
0x2E3	7 - 0	R/W	MPIP window origin X [7:0]	00h
Address	Bit	R/W	Description	Reset
0x2E4	7 - 0	R/W	MPIP window origin Y [7:0]	00h
Address	Bit	R/W	Description	Reset
0x2E5	7 - 0	R/W	MPIP Image memory initialization color	24h

Address	Bit	R/W	Description	Reset
0x2E6	7	R/W	PIP overlay key color position for Test.	0
	6-5	R/W	Reserved	00
	4 - 0	R/W	Alpha2 of PIP alpha blending (Main dimming) 10h : Full Main – 00h : Black	10h
Address	Bit	R/W	Description	Reset
0x2E7	7	R/W	Reserved	0
	6 - 4	R/W	PIP/MPIP horizontal border width (0 dot – 7 dots)	0h
	3	R/W	MPIP window origin Y [8]	0
	1 - 0	R/W	MPIP window origin X [9:8]	0h
Address	Bit	R/W	Description	Reset
0x2E8	7 - 4	R/W	MPIP window vertical spacing [3:0]	0h
	3 - 0	R/W	MPIP window horizontal spacing [3:0]	0h
Address	Bit	R/W	Description	Reset
0x2E9	7 - 6	R/W	MPIP maximum window number Y [1:0]. It's value plus 1 defines the column number of window array.	0h
	5 - 4	R/W	MPIP maximum window number X [1:0]. It's value plus 1 defines the row number of window array.	0h
	3 - 2	R/W	MPIP active window number Y [1:0]. It's value plus 1 defines the column number of the sub-window which receives write image.	0h
	1 - 0	R/W	MPIP active window number X [1:0]. It's value plus 1 defines the row number of the sub-window which receives write image.	0h
Address	Bit	R/W	Description	Reset
0x2EA	7	R/W	Reserved	0
	6 - 4	R/W	PIP/MPIP vertical border width [2:0] (0 line – 7 lines)	0h
	3 - 2	R/W	MPIP highlight window number Y [1:0]. It's value plus 1 defines the column number of the sub-window which has highlight frame color defined by 0x2EC.	0h
	1 - 0	R/W	MPIP highlight window number X [1:0]. It's value plus 1 defines the row number of the sub-window which has highlight frame color defined by 0x2EC.	0h
Address	Bit	R/W	Description	Reset
0x2EB	7 - 0	R/W	PIP/MPIP standard window frame color	1Ch
Address	Bit	R/W	Description	Reset
0x2EC	7 - 0	R/W	MPIP highlight window frame color	E0h
Address	Bit	R/W	Description	Reset
0x2EE	7	R/W	PIP data sampling control 1: Ignore DE	1
	6	R/W	PIP data cropping 1: Base on H/V Sync 0: Base on DE	1
Address	Bit	R/W	Description	Reset
0x2EF	7	R/W	1: PIP alpha blending enable, 0: Disable	0
	6	R/W	1: 565 mode (4:4:4 color space) for PIP, 0: 888 mode (4:2:2 color space) Default	0
	5	R/W	1: PIP alpha blending key detection reverse	0
	4 - 0	R/W	Alpha1 of PIP alpha blending (Main/Sub mixing ratio), 10h : Full PIP – 00h : Full Main	10h
Address	Bit	R/W	Description	Reset
0x2F0	7 - 0	R/W	Red key color level for PIP alpha blending	00h
Address	Bit	R/W	Description	Reset
0x2F1	7 - 0	R/W	Green key color level for PIP alpha blending	00h
Address	Bit	R/W	Description	Reset
0x2F2	7 - 0	R/W	Blue key color level for PIP alpha blending	00h
Address	Bit	R/W	Description	Reset
0x2F3	7 - 0	R/W	Key color range	00h

0x2ED – PIP/MPIP Control Registers

Address	Bit	R/W	Description	Reset
0x2ED	7	R/W	Reserved	00
	6	R/W	Reserved	0
	5	R/W	Reserved	0
	3 - 2	R/W	Reserved	00
	1	R/W	Reserved	0
	0	R/W	Reserved	0
Address	Bit	R/W	Description	Reset
0x2EE	7	R/W	Reserved	0
	6	R/W	1: Use DTV input DE, 0: Do not use input DE, use input HS/VS instead	0
	5 - 4	R/W	Reserved	0h
	3 - 2	R/W	PIP input selection. 0 : Decoder, 1 : Analog RGB/YUV, 2 : DTV	0h
	1 - 0	R/W	MPIP input selection. 0 : Decoder, 1 : Analog RGB/YUV, 2 : DTV	0h

0x2F4 to 0x2F8 – Power Management Registers

Address	Bit	R/W	Description	Reset
0x2F4	7-0	R/W	MSB of an internal 23 bit divide down counter. The 27 MHz clock from pin#33 XTAL27I is divided by this counter to serve as the clock for the Power State Transition timer.	0000 0000
Address	Bit	R/W	Description	Reset
0x2F5	7	R/W	Force the internal PCLK to "0".	0
	6	R/W	clksel_fppwr	0
	5-4	R	Show current power management state. These power states determine the states of pins #40 FPPWC, #39 FPBIAS & FP interface signals which includes #55 FPVS, #56 FPHS, #57 FPDE, #53 FPCLK and all data signals. FPPWC FPBIAS FP Interface Signals 00: Off "0" "0" "0" 01: Standby "1" "0" "0" 10: Suspend "1" "0" "1" or "0" 11: On "1" "1" "1" or "0" The transition between the power states does not occur right away. It takes place after the timer expiration by the corresponding timer counts defined in 0x275-0x277	00
	3	R/W	Manual power sequencing control. When this bit is set, bits [2:0] control #39 FPBIAS, FP Interface Signals, and #40 FPPWC directly.	0
	2	R/W	If bit 3 is "0" and this bit is "1", this enable auto power sequencing. VSYNC loss & HSYNC loss ---> Off VSYNC loss & HSYNC active ---> Standby VSYNC active & HSYNC loss ---> Suspend VSYNC active & HSYNC active ---> On	0
	1-0	R/W	Power state steering. When these 2 bits are written, assuming both bit 3 and bit 2 are 0's, and the current power state is different from the value written, the power state will be sequencing to the state that matches the value written. For example, current power state is 11. A 01 value is written. The power state will be steered to "01" and stay in "01. 00: Off State, 01: Standby, 10: Suspend, 11: ON state	00
Address	Bit	R/W	Description	Reset
0x2F6	7-4	R/W	Timer Counts for Suspend State to Standby State Transition	0000
	3-0	R/W	Timer Counts for On State to Suspend State Transition	0000
Address	Bit	R/W	Description	Reset
0x2F7	7-4	R/W	Timer Counts for Power Off State to Standby State Transition	0000
	3-0	R/W	Timer Counts for Standby State to Power Off State Transition	0000
Address	Bit	R/W	Description	Reset
0x2F8	7-4	R/W	Timer Counts for Standby State to Suspend Sate Transition	0000
	3-0	R/W	Timer Counts for Suspend to On State Transition	0000

Timing Controller Configuration Registers

0x300 – Output Mode Control Register

Bit	Function	R/W	Description	Reset
7	SIG_OFF	R/W	LCD Panel signals off control during power off 0 : Disable 1 : All signals and data keep zero after GPIO[0] was zero. (Between Back light off and LCD power OFF)	0
6	TCCK_PH	R/W	TCCLK phase control if reg0x300[0] set is high. (Divide Clock Mode) 0 : No clock phase shift 1 : Clock phase 90 degree shift *** It's set reg0x270[3] (invert clock polarity) high and this bit set high also then TCCLK is 270 degree shift.	0
5	ROE_EN	R/W	ROE (Row Driver) Output Enable 0 : Disable 1 : Enable	1
4 -1		R/W	Reserved	--
0	DIV_CK	R/W	Output mode selection 0 : One pixel data out per TCCLK 1 : Two pixel data out per TCCLK (Rising and Falling both)	0

0x301 – Display Control Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3	REV_EN	R/W	Pixel data reverse control 0 : Data no reverse (Don't case TCREV signal) 1 : Data reverse if TCREV signal is high period	0
2		R/W	Reserved	---
1-0	INV	R/W	Inversion mode selection 2'b00 : Disable 2'b01 : Disable 2'b10 : Line Inversion 2'b11 : Frame Inversion	00

0x302 – Display Direction Control Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-2	TOP_BTM	R/W	Top/Bottom display direction select 2'b00 : Top low active (Normal) 2'b01 : Top high active (Normal) 2'b10 : Bottom low active (Flip) 2'b11 : Bottom high active (Flip)	01
1-0	LFT_RHT	R/W	Left/Right display direction select 2'b00 : Left low active (Normal) 2'b01 : Left high active (Normal) 2'b10 : Right low active (Mirror) 2'b11 : Right high active (Mirror)	01

0x303 – Control Signal Polarity Selection Register

Bit	Function	R/W	Description	Reset
7-4			Reserved	----
3	ROE_P	R/W	Row Driver Output Enable signal 0 : Active low 1 : Active high	1
2	RSP_P	R/W	Row Driver Start Pulse signal 0 : Active low 1 : Active high	1
1	CLP_P	R/W	Column Driver Latch Pulse signal 0 : Active low 1 : Active high	1
0	CSP_P	R/W	Column Driver Start Pulse signal 0 : Active low 1 : Active high	1

0x304 – Control Signal Generation Method Register

Bit	Function	R/W	Description	Reset
7	PGM_SHARP	R/W	0 : Sharp same polarity start point follow TRSP pulse 1 : Sharp same polarity start point follow SHARP_STR register	
6	SP_CTRL	R/W	Unused Output Start Pulse Pin Control 0 : Zero 1: Hi-Z	
5	PGM_RCK	R/W	Row Driver Clock signal	0
4	PGM_ROE	R/W	Row Driver Output Enable signal 0 : This is generate during horizontal display enable. 1 : It's generated that set TCON register address 0x32C though 0x32F. Also, this is relative to vertical active register 0x30C though 0x30F.	0
3	PGM_RSP	R/W	Row Driver Start Pulse signal 0 : This signal immediately generate and then keep one horizontal period activation received from vertical active signal. 1 : It's generated that set TCON register address 0x324 though 0x327. Also, this is relative to vertical back porch register 0x279.	0
2	PGM_POL	R/W	0 : This Signal toggles when hsync toggle. 1: It's generated that set TCON register 0x310 through 0x311	1
1	PGM_CLP	R/W	Column Driver Latch Pulse signal 0 : This signal generate after horizontal display enable done a every scan line. 1 : It's generated that set TCON register address 0x312 though 0x315.	0
0	PGM_CSP	R/W	Column Driver Start Pulse signal 0 : This signal generate after horizontal display enable. 1 : It's generated that set TCON register address 0x31A though 0x31D. Also, this is relative to horizontal back porch register 0x274.	0

0x305 – Inversion signal operating period register

Bit	Function	R/W	Description	Reset
7-1		R/W	Reserved	----
0	INV_SW	R/W	Inversion signal (Column Driver) working period selection 0 : Inversion signal working within display enable period 1 : Inversion signal working whole(display enable and blanking time) period	0

0x306 – Panel type Select Register

Bit	Function	R/W	Description	Reset
7-2		R/W	Reserved	---
1	REV_INV	R/W	Signal output selection 0 : TCINV signal output select 1 : TCREV output select	1
0	LINE_INV	R/W	Analog panel data swapping 0 : No data inversion 1 : Every line data inversion	0

0x30A – Special LCD Module Control Register

Bit	Function	R/W	Description	Reset
7-6		R/W	Reserved	--
5-4	RSP_WIDTH	R/W	Row Driver Start Pulse width (period) selection 0 : One horizontal period 1 : Two horizontal period 2 : Three horizontal period 3 : Four horizontal period	00
3-2		R/W	Reserved	--
1-0	COMPANY	R/W	LCD module company selection 2'b00 : LG-Philips LCD module 2'b01 : Sharp LCD module 2'b10, 2'b11 : Other companies LCD module	10

0x30B – REVV(TCPOLP) / REVC(TCPOLN) Control Registers

Bit	Function	R/W	Description	Reset
7-0	REVV_REVC	R/W	REVV_REVC[7 :0] for Sharp	4Dh

0x30C – Vertical Active Start High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	V_ST[11:8]	R/W	VER_ASH[11:8]	0h

0x30D – Vertical Active Start Low Register

Bit	Function	R/W	Description	Reset
7-0	V_ST[7:0]	R/W	VER_ASL[7:0]	06h

0x30E – Vertical Active End High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	V_ED[11:8]	R/W	VER_AEH[11:8]	1h

0x30F – Vertical Active End Low Register

Bit	Function	R/W	Description	Reset
7-0	V_ED[7:0]	R/W	VER_AEL[7:0]	E2h

Column Driver Chip Control Signals Relative Registers

0x310 – Polarity Control High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	CP_SW[11:8]	R/W	Programmable polarity period high[11:8] value.	2h

0x311 – Polarity Control Low Register

Bit	Function	R/W	Description	Reset
7-0	CP_SW[7:0]	R/W	Programmable polarity period low[7:0] value.	D0h

0x312 – Load/Latch Pulse Start High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	CLP_ST[11:8]	R/W	LP_HSH[11:8]	2h

0x313 – Load/Latch Pulse Start Low Register

Bit	Function	R/W	Description	Reset
7-0	CLP_ST[7:0]	R/W	LP_HSL[7 :0]	D0h

0x314 – Load/Latch Pulse Width High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	CLP_ED[11:8]	R/W	LP_HEH[11:8]	0h

0x315 – Load/Latch Pulse Width Low Register

Bit	Function	R/W	Description	Reset
7-0	CLP_ED[7:0]	R/W	LP_HEL[7:0]	06h

0x31A – Column Driver Start Pulse High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	CSP_ST[11:8]	R/W	SP_HSH[11:8]	0h

0x31B – Column Driver Start Pulse Low Register

Bit	Function	R/W	Description	Reset
7-0	CSP_ST[7:0]	R/W	SP_HSL[7 :0]	C8h

0x31C – Column Driver Start Pulse Width High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	CSP_ED[11:8]	R/W	SP_HEH[11 :8]	0h

0x31D – Column Driver Start Pulse Width Low Register

Bit	Function	R/W	Description	Reset
7-0	CSP_ED[7:0]	R/W	SP_HEL[7 :0]	01h

Row Driver Chip Control Signals Relative Registers

0x320 – Clock Start Pulse High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	RCK_ST[11:8]	R/W	RCK_HSH[11:8]	0

0x321 – Clock Start Pulse Low Register

Bit	Function	R/W	Description	Reset
7-0	RCK_ST[7:0]	R/W	RCK_HSL[7 :0]	00h

0x322 – Clock Start Pulse Width High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	RCK_ED[11:8]	R/W	RCK_HEH[11 :8]	2h

0x323 – Clock Start Pulse Width Low Register

Bit	Function	R/W	Description	Reset
7-0	RCK_ED[7:0]	R/W	RCK_HEL[7 :0]	30h

0x324 – Row Start Pulse High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	RSP_ST[11:8]	R/W	RSP_VSH[11:8]	0h

0x325 – Row Start Pulse Low Register

Bit	Function	R/W	Description	Reset
7-0	RSP_ST[7:0]	R/W	RSP_VSL[7 :0]	06h

0x326 – Row Start Pulse Width High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	RSP_ED[11:8]	R/W	RSP_VEH[11 :8]	0h

0x327 – Row Start Pulse Width Low Register

Bit	Function	R/W	Description	Reset
7-0	RSP_ED[7:0]	R/W	RSP_VEL[7 :0]	01h

0x32C – Row Output Enable High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	ROE_ST[11:8]	R/W	ROE_HSH[11:8]	0

0x32D – Row Output Enable Low Register

Bit	Function	R/W	Description	Reset
7-0	ROE_ST[7:0]	R/W	ROE_HSL[7 :0]	0Ah

0x32E – Row Output Enable Width High Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	ROE_ED[11:8]	R/W	ROE_HEH[11 :8]	0

0x32F – Row Output Enable Width Low Register

Bit	Function	R/W	Description	Reset
7-0	ROE_ED[7:0]	R/W	ROE_HEL[7 :0]	36h

0x334 – Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	
3-0	SHARP_STR_H	R/W	Sharp same polarity start point high bits	0h

0x335 –Register

Bit	Function	R/W	Description	Reset
7-0	SHARP_STR_L	R/W	Sharp same polarity start point low bits	20h

0x336 –Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	SHARP_END_H	R/W	Sharp same polarity end point high bits	1h

0x337 –Register

Bit	Function	R/W	Description	Reset
7-0	SHARP_END_L	R/W	Sharp same polarity end point low bits	E2h

0x338 –Register

Bit	Function	R/W	Description	Reset
7-6		R/W	Reserved	---
5	CLPW	R/W	TCLP direct mode pulse width control. { 1`b0 => 1 clk, 1'b1 => 2 clks }	0
4	CSYNC_MODE	R/W	Enable csync mode	0
3-2	CLPSEL	R/W	Direct tcsp pulse adjust register	00
1-0	CSPSEL	R/W	Direct tclp pulse adjust register	00

0x339 –Register

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved	---
3-0	POL_STEP	R/W	TCPOL direct mode 16 step control	0h

0x3A0 to 0x3A0 – PLL Control Registers

The frequency of the Flat Panel Clock Output (FPCLK) pin can be controlled by an internal frequency multiplier based on the video decoder clock source (XTAL27I), or by an external oscillator connected to the PCLK pin. When the internal frequency multiplier is being used, the frequency of the Flat Panel Clock Output signal is determined by the following formula.

Address	Bit	R/W	Description	Reset
0x3A0	7-5	R/W	Charge Pump Current Control for PCLK	40h
	4-0	R/W	PCLK Oscillation frequency calculation FREQ_P[19:15] PCLK PLL Oscillation frequency = 108MHz * FREQ_P / 2 ^ 17 / 2^ POST_P	
Address	Bit	R/W	Description	Reset
0x3A1	7-0	R/W	FREQ_P[14:7]	00h
Address	Bit	R/W	Description	Reset
0x3A2	7-1	R/W	FREQ_P[6:0]	0000000
	0	R/W	Reserved	0
Address	Bit	R/W	Description	Reset
0x3A3	7-0	R/W	It control PCLK spread spectrum modulation frequency. SSFREQ_P[7:0] Spread spectrum modulation frequency = 27MHz * SSFREQ_P / 2^16	00h
Address	Bit	R/W	Description	Reset
0x3A4	7-4	R/W	This bit control PCLK variance of spread spectrum. SSG_P[3:0] Frequency Deviation Control for PCLK : The Max percentage of frequency deviation is given by following equation. DEV = 2^8 * SSG_P / 2^SSD / 2^FREQ_P * 100 %	00h
	3-2	R/W	PCLK VCO[1:0] 00 : 13.5 ~ 27MHz, 01 : 27 ~ 54 MHz 10 : 54 ~ 108MHz, 11 : 108 ~ 133MHz	
	1-0	R/W	POST_P: PCLK POST[1:0]	
Address	Bit	R/W	Description	Reset
0x3A5	7-5	R/W	Charge Pump Current Control for MCLK	40h
	4-0	R/W	MCLK Oscillation frequency calculation FREQ_M[19:15] MCLK PLL Oscillation frequency = 108MHz * FREQ_M / 2 ^ 17 / 2^ POST_P	
Address	Bit	R/W	Description	Reset
0x3A6	7-0	R/W	FREQ_M[14:7]	00h
Address	Bit	R/W	Description	Reset
0x3A7	7-1	R/W	FREQ_M[6:0]	0000000
	0	R/W	Reserved	0
Address	Bit	R/W	Description	Reset
0x3A8	7-0	R/W	It control MCLK spread spectrum modulation frequency. SSFREQ_M[7:0] Spread spectrum modulation frequency = 27MHz * SSFREQ_M / 2^16	00h
Address	Bit	R/W	Description	Reset
0x3A9	7	R/W	SS-PLL output clock select. 0 : 27MHz XTAL input 1 : PCLK select	0
	6	R/W	SS-PLL output clock select. 0 : 27MHz XTAL input 1 : MCLK select	0
	5	R/W	Freq. Synthesizer Power down for PCLK 0 : Normal Operation, 1 : Off	0
	4	R/W	Freq. Synthesizer Power down for MCLK 0 : Normal Operation, 1 : Off	0
	3	R/W	PLL input select. 0 : 27MHz XTAL 1 : PCLK	0
	2-0	R/W	SS-PLL gain divider for MCLK, MDGAIN[2:0]	000

Address	Bit	R/W	Description	Reset
0x3AA	7-4	R/W	This bit control MCLK variance of spread spectrum. SSG_M[3:0] Frequency Deviation Control for MCLK : The Max percentage of frequency deviation is given by following equation. DEV = 2^8 * SSG_M / 2^SSD / 2^FREQ_M * 100 %	00
	3-2	R/W	MCLK VCO[1:0] 00 : 13.5 ~ 27MHz, 01 : 27 ~ 54 MHz 10 : 54 ~ 108MHz, 11 : 108 ~ 133MHz	
	1-0	R/W	POST_M : MCLK POST[1:0]	
Address	Bit	R/W	Description	Reset
0x3AB	7-5	R/W	SS-PLL gain divider for PCLK, PDGAIN[2:0]	
	4-0	R/W	DA_RGAIN	
Address	Bit	R/W	Description	Reset
0x3AC	7-5	R/W	Reserved	
	4-0	R/W	DA_GGAIN	
Address	Bit	R/W	Description	Reset
0x3AD	7-5	R/W	Reserved	
	4-0	R/W	DA_BGAIN	
Address	Bit	R/W	Description	Reset
0x3AE	7	R/W	DAC power down	0
	6-5	R/W	Reserved for internal test.	0
	4	R/W	DAC IREF	0
	3-0	R/W	Reserved	0h
Address	Bit	R/W	Description	Reset
0x3F0	7-6	R/W	Reserved	0
	5-0	R/W	HSWID, Hsync Widith. The unit of HWSID is one clock cycle.	10h
Address	Bit	R/W	Description	Reset
0x3FF	7 - 6	R/W	Page Register	00

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Revision History

Date	Revision Note
10/19/2007	Revision B Datasheet
01/21/2008	Revision C Datasheet -ADD RoHS Label -Remove Font base teltext OSD feature, VBI Slicer, SCART RGB support -OSD support dual window bitmap -Pin 30, 31, 37 description updated -Register 0x00D, 0x00E, 0x00F, 0x036, 0x037, 0x038[7] 0x1B3[1] remove -Updated register 0x006[6][5], 0x01F, 0x102[4], 0x1B8, 0x1B9, 0x1C0, 0x1CE, 0x1F0[3:0],0x21F[2:1], 0x1CC[3:2] -Add register 0x131~0x136, 0x2E6[7], 0x2EE[7][6], 0x13A[5:4], 0x13D[7], 0x3F0[5:0]
02/07/2008	Updated temperature spec