

## KB22688

## TV SOUND MPS FOR TWO CARRIER SYSTEM

### ONE-CHIP TV SOUND MPX ( TWO - CARRIER SYSTEM )

The KB22688 is a monolithic integrated circuit designed for demodulating two carrier TV-MPX broadcast.

### FEATURES

- 1st & 2nd Sound IF
- Double-PLL FM Detection
- AGC for CCA part
- Matrix for Multi - Sound Broadcasts
- Pilot Detector
- External Control Interface
- ID Indicators ( Stereo , Bilingual )

### FEATURES

- Available for Korea standard
- Non-clipping Output up to 400% modulation with AGC
- Available in DC control, Normal u-COM control or IIC bus control systems
- ID output : Direct LED drive or IIC serial data output
- Non-adjust

32-SDIP-400



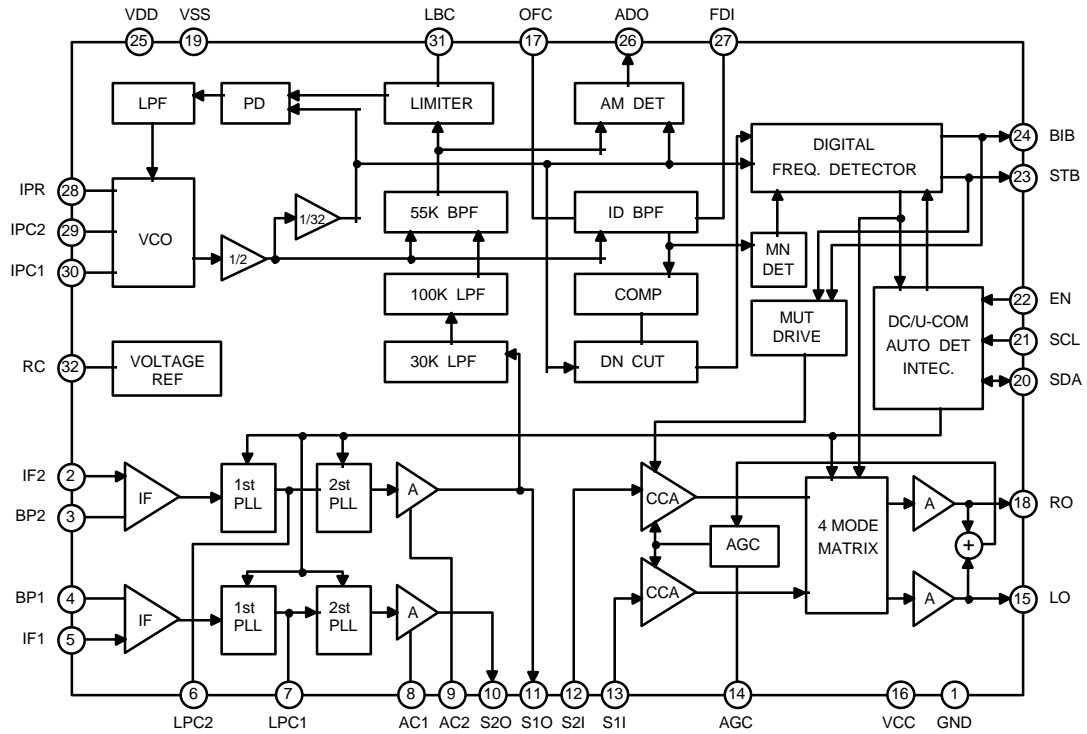
### ORDERING INFORMATION

Device	Package	Operating Temperature
KB22688	32-SDIP-400	-10°C ~ + 70°C

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## BLOCK DIAGRAM



**KB22688**
**TV SOUND MPS FOR TWO CARRIER SYSTEM**
**ABSOLUTE MAXIMUM RATINGS ( Ta = 25°C )**

Characteristics	Symbol	Condition	Value	Unit
Maximum Supply Voltage	VCCmax		6	V
Power Dissipation	Pd	Vi = 0	1000	mW
Operating Temperature	Topr		- 10 ~ + 70	°C
Storage Temperature	Tstg		- 40 ~ + 125	°C

**RECOMMENDED OPERATING CONDITIONS**

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	Vopr	4.5	5	5.5	v

**ELECTRICAL CHARACTERISTICS**

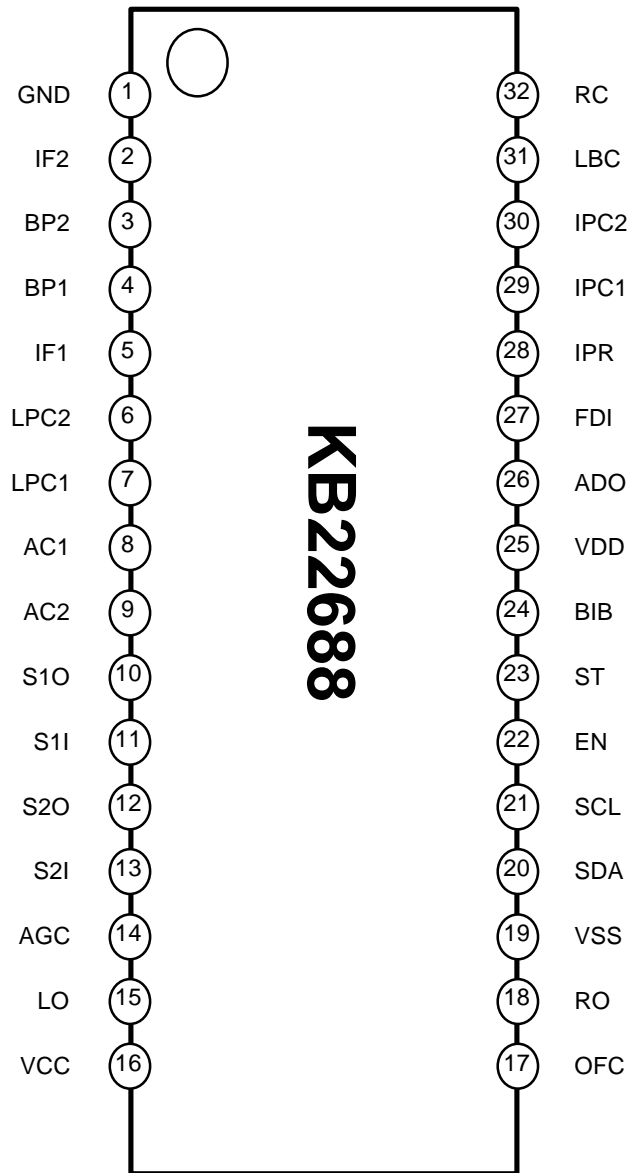
(VCC = VDD = 5V, fm = 1KHz, Vi = 80dBu, Ta = 25°C, Δf = ± 25KHz, unless otherwise specified )

Characteristics	Symbol	Condition	Min	Typ	Max	Unit	
Total Circuit 1	ICC	Vi = 0	35	60	80	mA	
Total Circuit 2	IDD	Vi = 0	-	-	5	mA	
SIF	Input Limitng Voltage	Vlim	-	-	50	dBu	
	AM Rejection Ratio	AMRR	AM 30 % Mod.	40	45	-	dB
	Input Impedence	Zin	-	-	1	-	Kohm
PILOT	Pilot Input Sensitivity	Vps	-	-	50	dBu	
	ID ON time	Ton	MONO → ST, BI	-	1.0	1.5	SEC
	ID OFF time	Toff	ST, BI → MONO	-	-	0.3	SEC
MATRIX	Output Level	Vo	-	280	370	500	mVrms
	Matrix THD	THDm1	-	-	0.2	1.0	%
		THDm2	Δ f = ± 100KHz	-	0.5	10	%
	Noise Output (RF off)	Voff	Carrier OFF	-	50	370	mVrms
	Output Impedence	Zout	-	-	-	50	ohm
	Separation Ratio	SEP	Δ f = ± 25 KHz	40	45	-	dB
	Cross Talk	CT	Δ f = ± 25Khz	50	55	-	dB
	Matrix S/N Ratio	S/N	Δ f = ± 25Khz	55	60	-	dB
S/N(st)		Δ f = ± 25 KHz (ST)	50	55	-	dB	
MUTE Attenuation ratio	Amute	Δ f = ± 25KHz	-	-66	-55	dB	

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**PIN CONFIGURATION**



**KB22688****TV SOUND MPS FOR TWO CARRIER SYSTEM****PIN CONFIGURATION**

<b>Pin No.</b>	<b>Description</b>	<b>Pin No.</b>	<b>Description</b>
1	Analog GND	17	ID Filter Offset Canceling Cap.
2	SIF 2 Input	18	R Output
3	SIF 2 Bypass	19	Digital VSS
4	SIF 1 Bypass	20	Data Input / Output ( SDA )
5	SIF1 Input	21	Clock Input ( SCL )
6	SIF 2 LPF Capacitor	22	Enable Input ( EN )
7	SIF 1 LPF Capacitor	23	ID Indicator ( Stereo )
8	SIF 1 Amplifier Capacitor	24	ID Indicator ( Bilingual )
9	SIF 2 Amplifier Capacitor	25	Digital VDD
10	SIF 1 DET Output	26	AM DET Output
11	SIF 1 CCA Input	27	Freq. DET Input
12	SIF 2 DET Output	28	ID PLL VCO Resistor
13	SIF 2 CCA Input	29	ID PLL VCO Capacitor pin 1
14	AGC Detect Capacitor	30	ID PLL VCO Capacitor pin 2
15	L output	31	Limiter Bypass Capacitor
16	Analog VCC	32	Voltage Reference Capacitor

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**INTERNAL PIN DESCRIPTION**

Pin No	Symbol	Function	Description	Equivalent Circuit
1	GND	ANALOG GROUND	-	-
2, 5	SIF 2, SIF 1	SIF input pin	SIF signal input through a SIF filter	
3, 4	BP 2, BP 1	IF bypass pin	IF Bypass pin is Grounded with a capacitor	
6, 7	LPC 2, LPC 1	PLL LPF pin	The external capacitor extracts DC level from the 1st PLL output of FM DET	
8, 9	AC 1, AC 2	DET AMP NF Pin	Negative feedback pin of FM DET amplifier Grounded with a capacitor	

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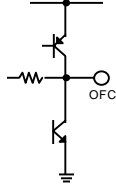
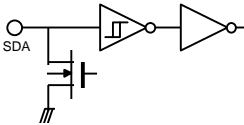
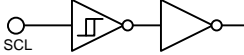
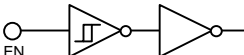
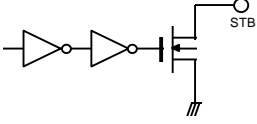
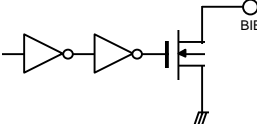
**INTERNAL PIN DESCRIPTION**

Pin No	Symbol	Function	Description	Equivalent Circuit
10, 12	S1O, S2O	FM DET Output	FM DET output pin Connected with a De-emphasis circuit	
11, 13	S1I S2I	FM detected signal Input pin	Input pin of current control amplifier (CCA). FM detected output signal is added to this pin	
14	AGC	AGC DET PIN	AGC detect pin is grounded through a capacitor. If the signal level is over the predetermined value, this terminal's voltage will be raisen. AGC function can be deactivated by connect this terminal to GND.	
15, 18	LO, RO	MATRIX Output pin	Audio output signal is provided from this terminal	

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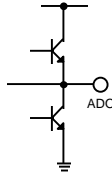
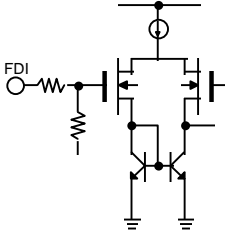
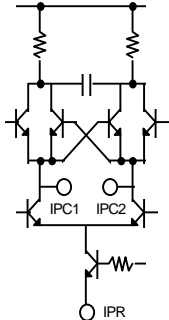
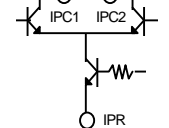
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**INTERNAL PIN DESCRIPTION**

Pin No	Symbol	Function	Description	Equivalent Circuit
16	VCC	ANALOG POWER	-	-
17	OFC	ID BPF OFFSET Cancel pin	The external capacitor is used to eliminate offset of ID filter .	
19	VSS	DIGITAL GROUND	-	-
20	SDA	SERIAL DATA IN & DATA OUT	It is the data communication line of IIC bus used to exchange the u-COM data and IC internal data .	
21	SCL	CLOCK SIGNAL	CLOCK line of IIC bus.	
22	EN	Enable Select PIN	It is always "H" in DC control system, always "L" in IIC bus system, and used as strobe port in normal u-COM system.	
23	STB	STEREO Indicator pin	When ID is detected as "STEREO", this pin will remain "L" ( OPEN DRAIN)	
24	BIB	BILINGUAL Indicator pin	When ID is detected as "Bilingual", this pin will remain "L" ( OPEN DRAIN)	



## INTERNAL PIN DESCRIPTION

Pin No	Symbol	Function	Description	Equivalent Circuit
26	ADO	AM DET Output pin	AM detected signal will output from this terminal.	
27	FDI	Frequency DET IN	AM detected signal goes into this terminal coupled with a capacitor to remove DC offset.	
28	IPR	ID PLL VCO Resistor pin	Connected external resistor. This resistor is used to set VCO current .	
29, 30	IPR	ID PLL VCO Resistor pin	Connected external capacitor. This capacitor determines the oscillation freq. of VCO	

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**INTERNAL PIN DESCRIPTION**

Pin No	Symbol	Function	Description	Equivalent Circuit
31	LBC	Limiter bypass capacitor pin	Ground through capacitor to extract DC level of output signal from the SC BPF output amplifier to the PD (Phase Detector ) of ID PLL.	
32	RC	Voltage Reference Capacitor pin	Connect to capacitor to stabilize the reference voltage	
25	VDD	Power Supply (Digital)	-	-



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### ⑥ ID DET

ID signal is FM modulated to second carrier (SIF2) with a  $\pm 2.5\text{KHz}$  FM modulation after AM modulated to 55KHz PILOT sub-carrier with a 50% AM modulation. ID DET part consists of 3 blocks : that is filter block for extracting pilot carrier, AM detector block for AM detection of ID signal and digital block for detecting the frequency of provided ID signal logically. In the filter block, audio signal is removed by HPF and pilot signal is extracted by the automatically adjusted switch - capacitor BPF(band pass filter) with a center frequency of 55KHz. ID signal is extracted from the pilot carrier in the AM detector block , then Digital block detects the frequency of ID signal, The ID signal can be detected in the range shown as follow:

ID	LOW OFF	LOW ON	HIGH ON	HIGH OFF
STEREO ( 150Hz )	125Hz	140Hz	160Hz	176Hz
BILINGUAL ( 276Hz )	237Hz	255Hz	300Hz	312Hz

For ID detector, the transition time from MONO to multi sound mode ( STEREO or BILINGUAL ) is about 1 SEC and from multi sound mode to MONO transition is about 0.3 SEC as to avoid detection error.

KB22688 has 2 types of ID output ; one is serial data out in IIC BUS u-COM control mode, the other is open drain type DC output, it can drive LED directly.

### ⑦ u-COM

KB22688 is available in DC control, normal u-COM control, and IIC BUS u-COM control system, and it can distinguish the control type automatically by monitoring PIN 22(EN) status. The relation of control source type and PIN 22 status is shown as follows.

	IIC BUS	NORMAL U-COM	DC CONTROL
EN ( PIN 22 )	always "L"	u -COM STROBE	always "H"

#### a) Protocol of IIC BUS u-COM control ( PIN 22: L )

The KB22688 can be controlled via the 2-line IIC BUS by the u-COM. The two lines ( SDA - serial data. SCL - serial clock ) exchange information between the devices connected to the IIC bus. Both SDA and SCL are bidirectional lines which is connected to a positive supply voltage via a pull up resistor.

When the bus is free both lined are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW data can only change when the clock signal line is LOW. A

HIGH -to -LOW transition of the SDA line while SCL is HIGH is defined as a start condition. A LOW- to -

HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition. The bus receiver will be reset by the reception of a start condition and is considered to be busy after the start condition. After a stop

condition the bus is considered as free again.



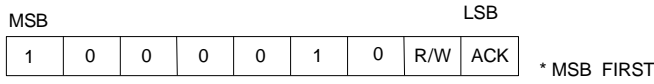
1st Byte : 1 ~ 7th bit } SLAVE Address : WRITE 84H, READ 85H  
 8th bit - R/W }  
 9th , 18th, 27th bit ---- Acknowledge

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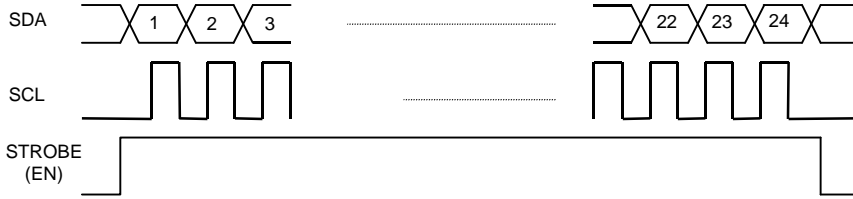
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2nd byte : 10th ~ 17th bit ---- SUB address ( function )  
 3rd byte : 19th ~ 26th bit ---- DATA ( D1 ~ D8 )

Data transmitted to the KB22688 starts with the module address as follows:

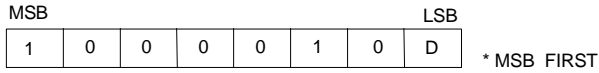


b) Protocol of normal u-COM control ( PIN 22: STROBE )



1st Byte : 1 ~ 7th bit ---- chip select code ( 1000010B )  
           8th bit ---- NOT USE ( don't care )  
 2nd Byte : 9th ~ 16th bit ---- function assignment  
 3rd Byte : 17th ~ 24th bit ---- DATA ( D1 ~ D8 )

The module address of KB22688 in normal u-COM control mode is as follows.



The maximum STROBE pulse width in normal u-COM control mode should be under 6.0 mSEC. If the STROBE pulse width excess the limit, KB22688 will be changed to DC control mode.

c) Control item in each control mode

In each control mode, control items is limited as follows.

CONTROL	MODE CHANGE	MUTE	PRE-SET	PRE-ADJUST SET	DATA TRANSMISSION	RECEIVE ACKNOWLEDGE
IIC BUS	O	O	O	O	O	O
NORMAL u-COM	O	O	O	X	X	X
DC CONTROL	O	X	X	X	X	X

\*\*\* DEFINITIONS \*\*\*

\* PRE-SET : When power is ON, u-COM initials the status of KB22688 to pre-set status. ( All IC has same pre-set status data )

\* PRE-ADJUST SET : When power is ON, u-COM initials the status of KB22688 to pre-measured and stored status. ( Different each IC )

\* DATA TRANSMISSION : Transmit stored data to u-COM when u-COM requests.

\* RECEIVE ACKNOWLEDGE : Return Acknowledge signal to u-COM after DATA receipt.

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d) u-COM control map

\*\* In IIC BUS mode, SLAVE Address = WRITE : 84H, READ : 85H

\*\* In normal u-COM mode, chip select code = 1000010B

SUB address (2nd Byte) (MSB <-> LSB)	DATA (3rd Byte)								Function	Remark
	MSB	DATA (3rd Byte)						LSB		
	D1	D2	D3	D4	D5	D6	D7	D8		
000XXXXX (MODE CONTROL)	0	0	X	X	X	X	X	X	MONO	END USER CONTROL
	1	0	X	X	X	X	X	X	STEREO	
	0	1	X	X	X	X	X	X	BILINGUAL	
	1	1	X	X	X	X	X	X	SUB	
001XXXXX (MUTE CONTROL)	0	X	X	X	X	X	X	X	MUTE OFF	
	1	X	X	X	X	X	X	X	MUTE ON	
010XXXXX (TEST MODE)	0	0	X	X	X	X	X	X	KOREA	IC MARKER TEST
	1	0	X	X	X	X	X	X	NOT USE	
	X	1	X	X	X	X	X	X	NOT USE	
011XXXXX	X	X	X	X	X	X	X	X	NOT USE	
100XXXXX	D1	D2	D3	D4	D5	X	X	X	SEP. ADJUST*	SET MAKER SETTING
101XXXXX	X	X	X	X	X	X	X	X	NOT USE	
110XXXXX (TEST MODE)	0	0	X	X	X	X	X	X	OPERATING	IC MAKER TEST
	1	0	X	X	X	X	X	X	NOT USE	
	X	1	X	X	X	X	X	X	NOT USE	
111XXXXX	X	X	X	X	X	X	X	X	NOT USE	

\* MSB FIRST

\* When power is ON, all latch datas are '0', so, KB22688 is set to MONO OFF, MUTE OFF, SEPARATION ADJUST DEFAULT (00001XXX).

\* Separation Adjust Data

D1D2D3D4D5                      D1D2D3D4D5                      D1D2D3D4D5  
 0 0 0 0 0 (MIN) <-- -      0 0 0 0 1 (TYP)              ---->      1 1 1 1 1 (MAX)

e) Control Function Description

\* MODE CONTROL : Control the MATRIX structure according to broadcast status and end user's setting.

KB22688 has 4 modes (MONO, STEREO, BILINGUAL and SUB)

\* MUTE CONTROL : When MUTE CONTROL is on, the audio output of KB22688 is off.

\* SEP. ADJUST : The separation characteristic of KB22688 in STEREO mode can be controlled by IIC BUS.

This option controls S2 FM demodulated output signal level so as to make the separation characteristic in best status.

\* TEST MODE : IC maker's test item.

f) DC Control Map (PIN22: H)

DC ( LOGIC ) INPUT		Function
SCL	SDA	
0	0	MONO
1	0	STEREO
0	1	BILINGUAL
1	1	SUB

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g) READ mode in IIC BUS u-COM control mode

KB22688 can transmit the data which is registered inside IC to the u-COM in IIC BUS control system.

If the 8th bit of module address is "H", it means u-COM requests the data stored in the IC and KB22688 enter data transmission mode. During the read mode, KB22688 ignores the data the data of 2nd byte ( SUB address ) and transmits the internal data within the period of 3rd byte. The SDA line of u-COM should be maintain "H" to accept transmitted data from IC. The format of read data is as follows.

Bit of 3rd Byte	1	2	3	4	5	6	7	8
Transmit Data	BI	ST	$\overline{BI}$	$\overline{ST}$	ZC	$\overline{ZC}$	0	1
	0011 : MONO 1001 : BILINGUAL 0110 : STEREO 1100 : used in ST → BI mode transition other case : transmission error				Option for IC marker. (ZC : IC test option )			

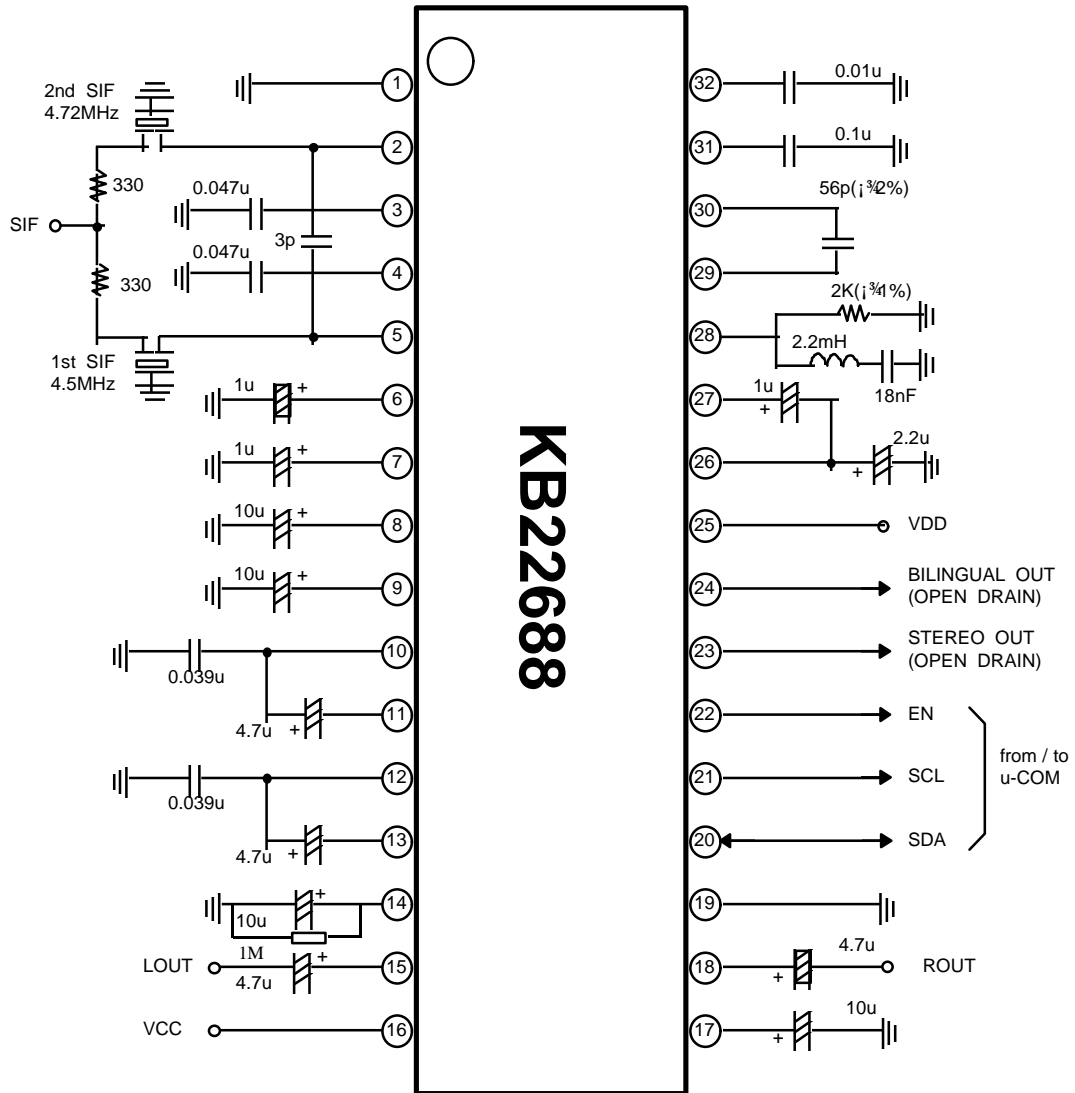
h) Others

In IIC BUS control system, if the SLAVE address is correct, the acknowledge signal will be generated by KB22688 nomatter the sub address is right or wrong , When sub address is wrong IC will do nothing.

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**APPLICATION CIRCUIT 1 (RLC TYPE, NON-ADJUSTMENT)**

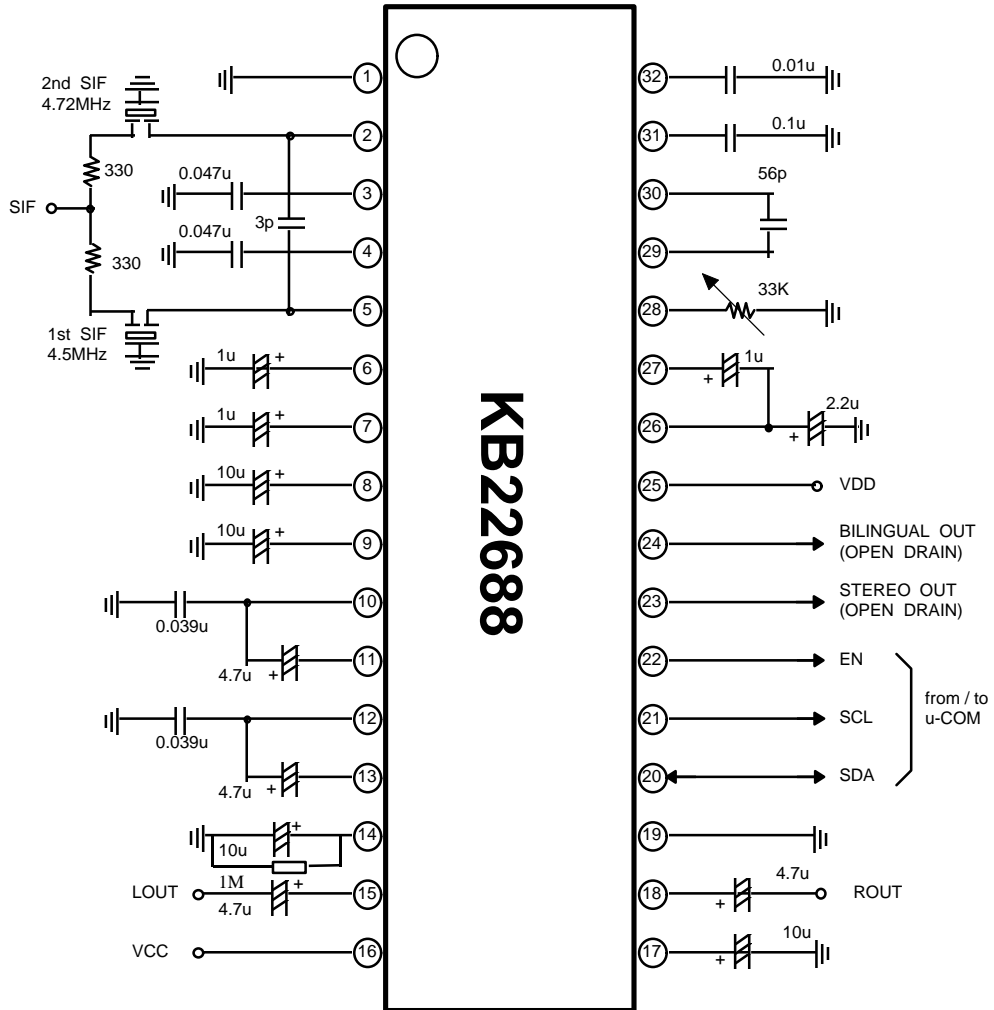




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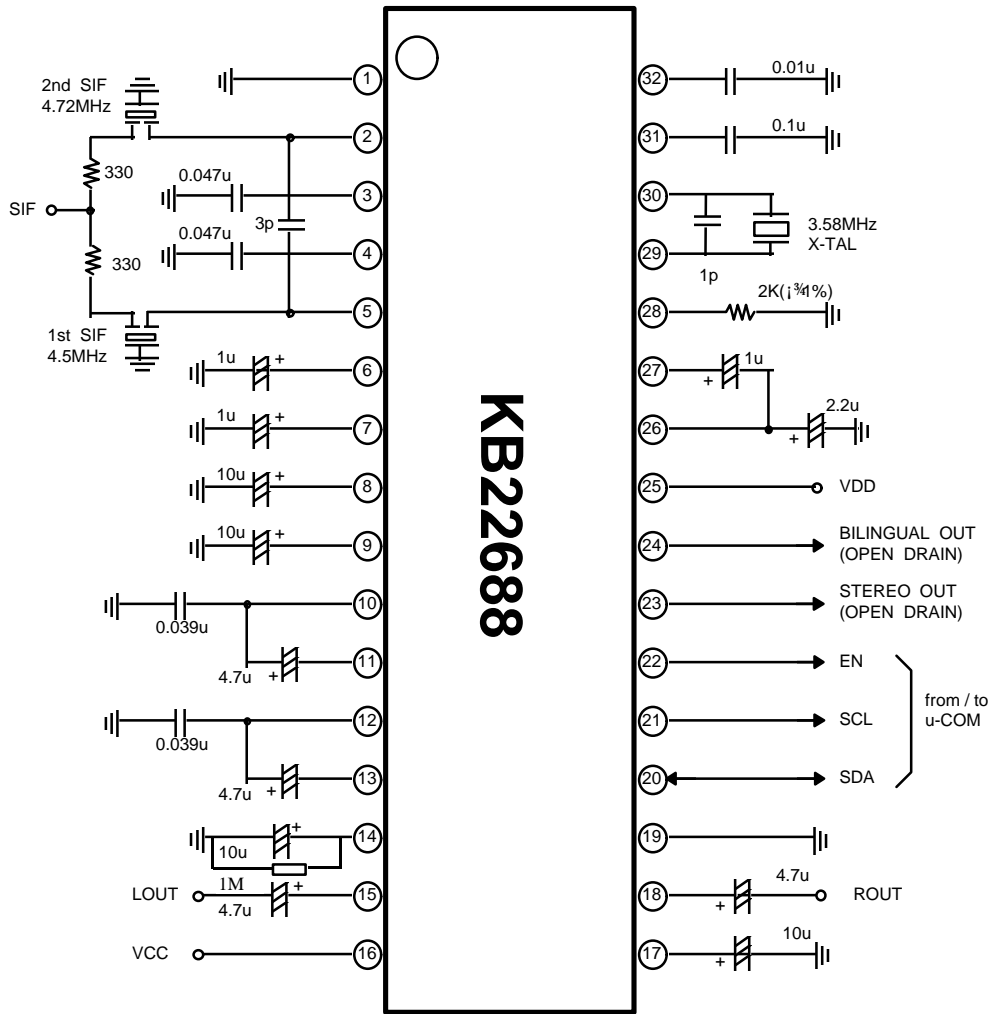
**APPLICATION CIRCUIT 2 (VR TYPE,LOW COST)**



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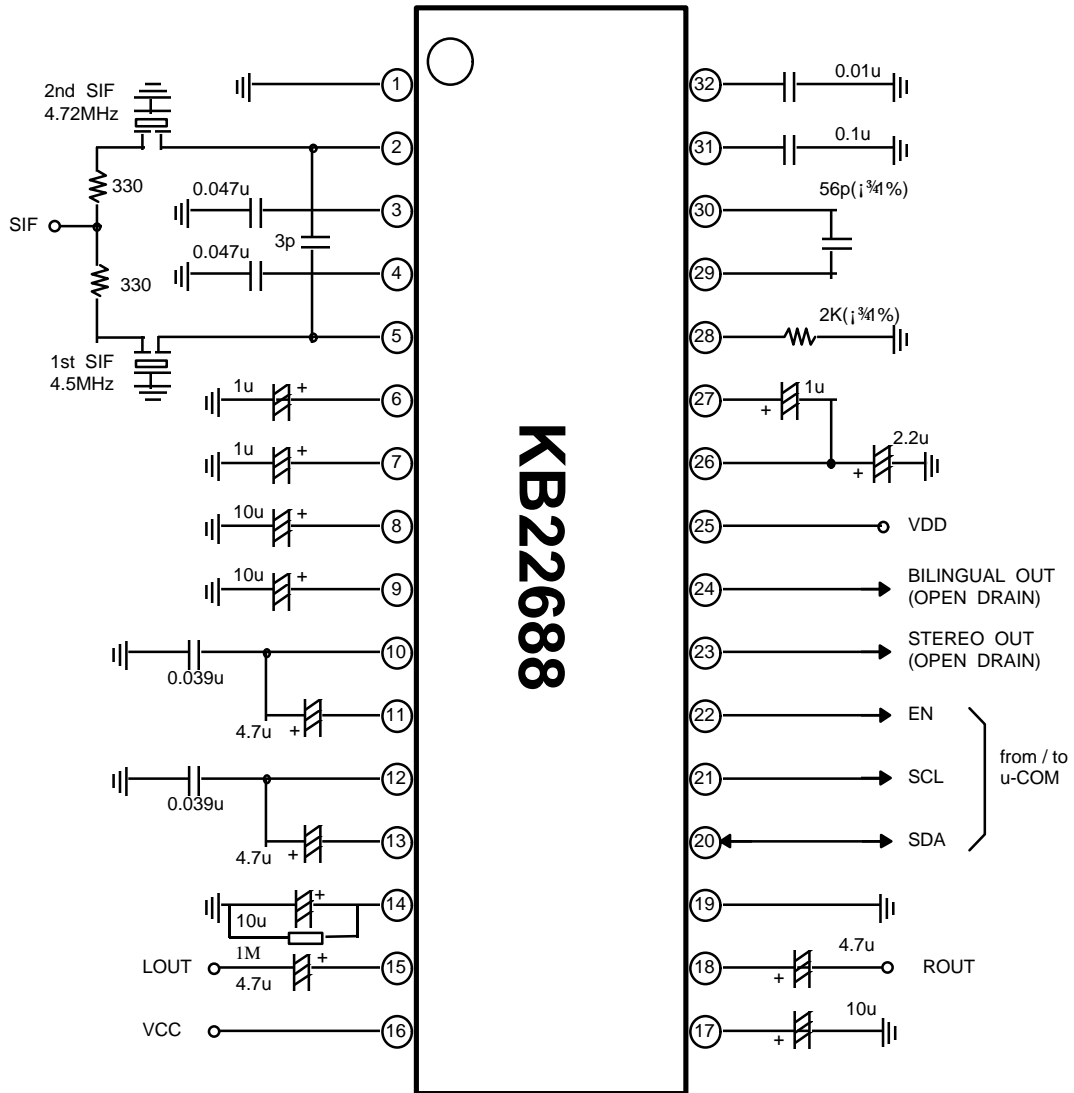
APPLICATION CIRCUIT 3 (CRYSTAL TYPE, HIGH STABILITY)



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**APPLICATION CIRCUIT 4 (RC TYPE, NON-ADJUSTMENT)**

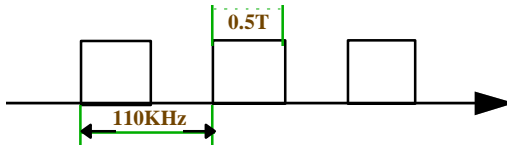


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### NOTE:

1. The characteristic of SIF FILTER should be suitable to MPX sound system.  
We suggest to use MURATA Co. products: SFSH4.5MCB and SFSH4.72MCB.
2. For VR type , we can adjust the variable resistor by testing the waveform of pin28,  
It is not fine adjusted until the duty ratio of square wave is just 50%.



3. You can select the PLL OSC external components among 4 type:

ITEM \ TYPE	PLC	VR	CRYSTAL	RC
STABILITY	middle	low	high	middle
COST	middle	middle	high	low
AJUSTMENT	no	need	no	no
EXT. COMPONENTS	3	2	3	2

### 4. PROGRAM CONTROL METHOD:

- 1) INSTALL: RUN KB22688.EXE
- 2) KEYBOARD SETUP:  
[NUMBER LOCK] --- OFF , [CAPS LOCK] --- ON
- 3) CONTROL MODE SELECT:  
I: iIC BUS MODE , N: u-COM MODE , D: DC CONTROL MODE
- 4) CONTROL ITEM:  
MODE SELECT , MUTE SET UP , SEPERATION ADJUST.
- 5) EXIT:

CAP OLCK OFF , CTL+ C

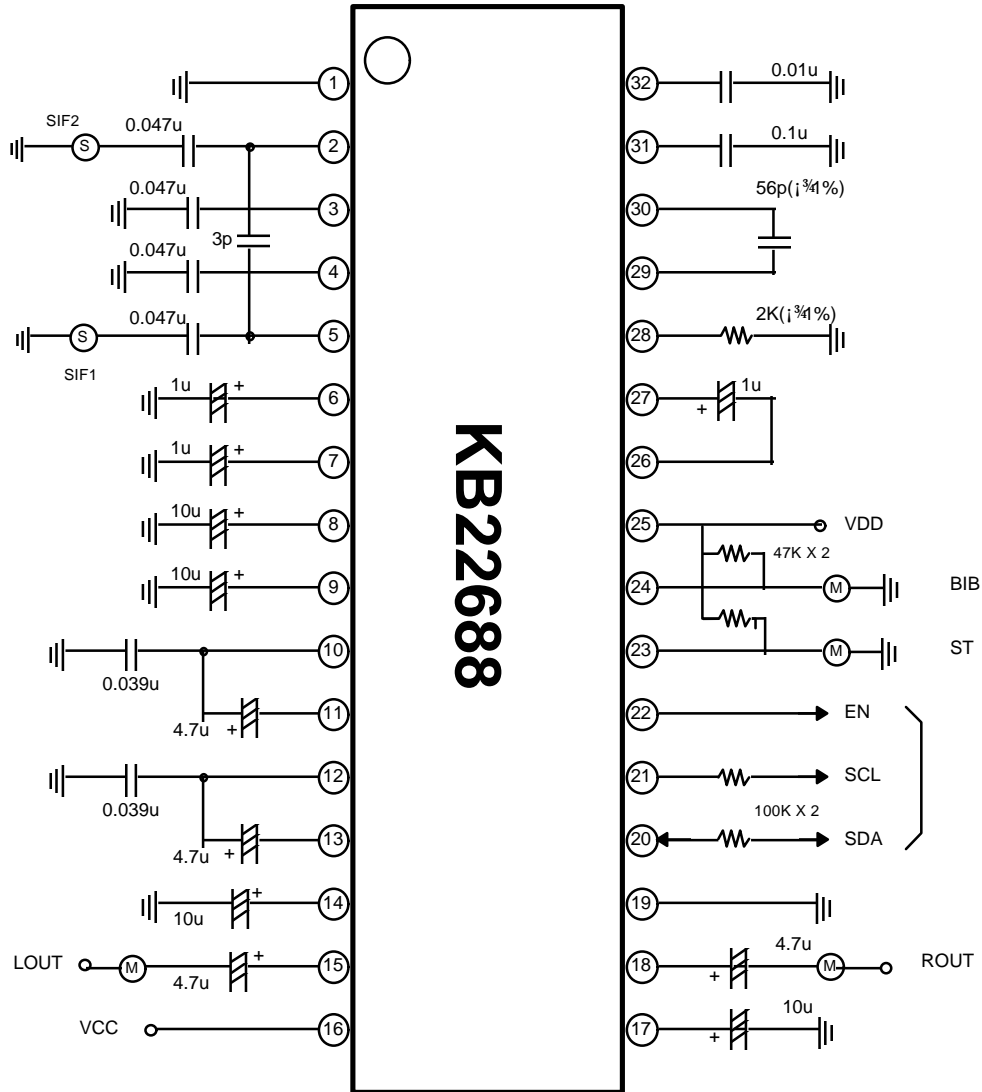
### 5. PC Parallel prot PIN Description:

PIN	2	3	4	18
SIGNAL	SCK	SDA	EN	END

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**TEST CIRCUIT**



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## PACKAGE DIMENSION

