

## FQP45N03L

### N-Channel Logic Level PWM Optimized Power MOSFET

#### General Description

This device employs a new advanced MOSFET technology and features low gate charge while maintaining low on-resistance.

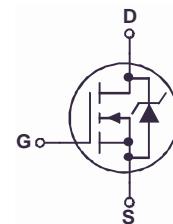
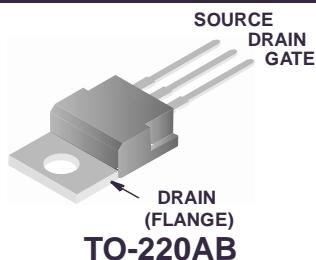
Optimized for switching applications, this device improves the overall efficiency of DC/DC converters and allows operation to higher switching frequencies.

#### Applications

- DC/DC converters

#### Features

- Fast switching
- $r_{DS(ON)} = 0.014\Omega$  (Typ),  $V_{GS} = 10V$
- $r_{DS(ON)} = 0.020\Omega$  (Typ),  $V_{GS} = 5V$
- $Q_g$  (Typ) = 13nC,  $V_{GS} = 5V$
- $Q_{gd}$  (Typ) = 4.5nC
- $C_{iss}$  (Typ) = 1450pF



#### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 16$	V
$I_D$	Drain Current Continuous ( $T_C = 25^\circ C$ , $V_{GS} = 10V$ )	41	A
	Continuous ( $T_C = 100^\circ C$ , $V_{GS} = 4.5V$ )	22	A
	Continuous ( $T_C = 25^\circ C$ , $V_{GS} = 10V$ , $R_{\theta JA} = 43^\circ C/W$ )	8.1	A
	Pulsed	Figure 4	A
$P_D$	Power dissipation Derate above $25^\circ C$	53	W
		0.43	$W/\text{ }^\circ C$
$T_J$ , $T_{STG}$	Operating and Storage Temperature	-55 to 150	$^\circ C$

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220	2.31	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220	62	$^\circ C/W$

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQP45N03L	FQP45N03L	TO-220AB	Tube	N/A	50

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 25\text{V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{V}$	$T_C = 150^\circ\text{C}$	-	-	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 16\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	-	3	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 41\text{A}, V_{GS} = 10\text{V}$	-	0.014	0.018	$\Omega$
		$I_D = 22\text{A}, V_{GS} = 4.5\text{V}$	-	0.020	0.025	

**Dynamic Characteristics**

$C_{ISS}$	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	1450	-	pF
$C_{OSS}$	Output Capacitance		-	300	-	pF
$C_{RSS}$	Reverse Transfer Capacitance		-	120	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{DD} = 15\text{V}$ $I_D = 22\text{A}$ $I_g = 1.0\text{mA}$	-	25	38	nC
$Q_{g(5)}$	Total Gate Charge at 5V		-	13	20	nC
$Q_{g(TH)}$	Threshold Gate Charge		-	1.5	2.3	nC
$Q_{gs}$	Gate to Source Gate Charge		-	4.3	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	4.5	-	nC

**Switching Characteristics** ( $V_{GS} = 4.5\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 11\text{A}$ $V_{GS} = 5\text{V}, R_{GS} = 11\Omega$	-	-	115	ns
$t_{d(ON)}$	Turn-On Delay Time		-	15	-	ns
$t_r$	Rise Time		-	60	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	25	-	ns
$t_f$	Fall Time		-	30	-	ns
$t_{OFF}$	Turn-Off Time		-	-	83	ns

**Switching Characteristics** ( $V_{GS} = 10\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 11\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 11\Omega$	-	-	57	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
$t_r$	Rise Time		-	30	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	45	-	ns
$t_f$	Fall Time		-	30	-	ns
$t_{OFF}$	Turn-Off Time		-	-	115	ns

**Unclamped Inductive Switching**

$t_{AV}$	Avalanche Time	$I_D = 2.9\text{A}, L = 3.0\text{mH}$	195	-	-	$\mu\text{s}$
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**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 22\text{A}$	-	-	1.25	V
		$I_{SD} = 20\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 22\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	65	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 22\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	100	nC

**Typical Characteristic**  $T_C = 25^\circ\text{C}$  unless otherwise noted

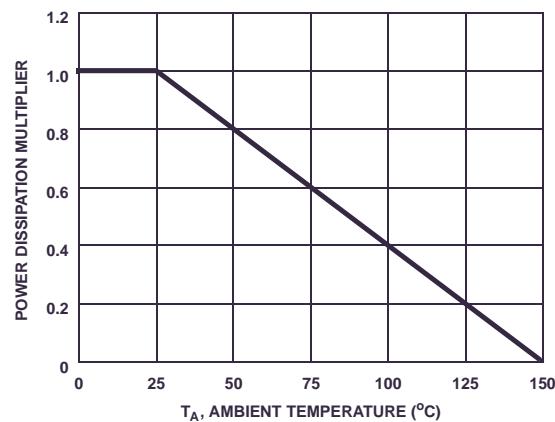


Figure 1. Normalized Power Dissipation vs Ambient Temperature

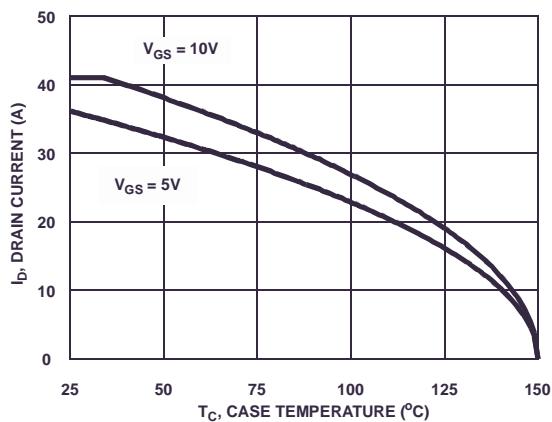


Figure 2. Maximum Continuous Drain Current vs Case Temperature

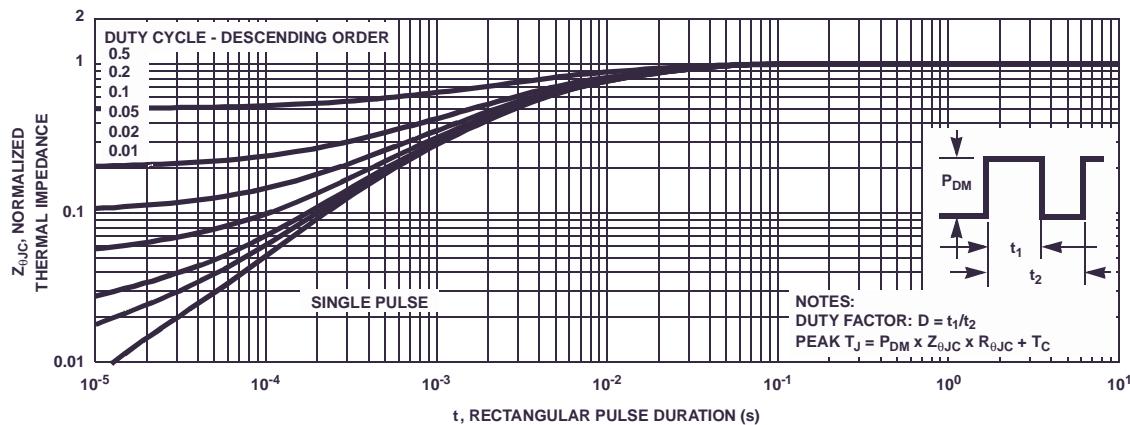


Figure 3. Normalized Maximum Transient Thermal Impedance

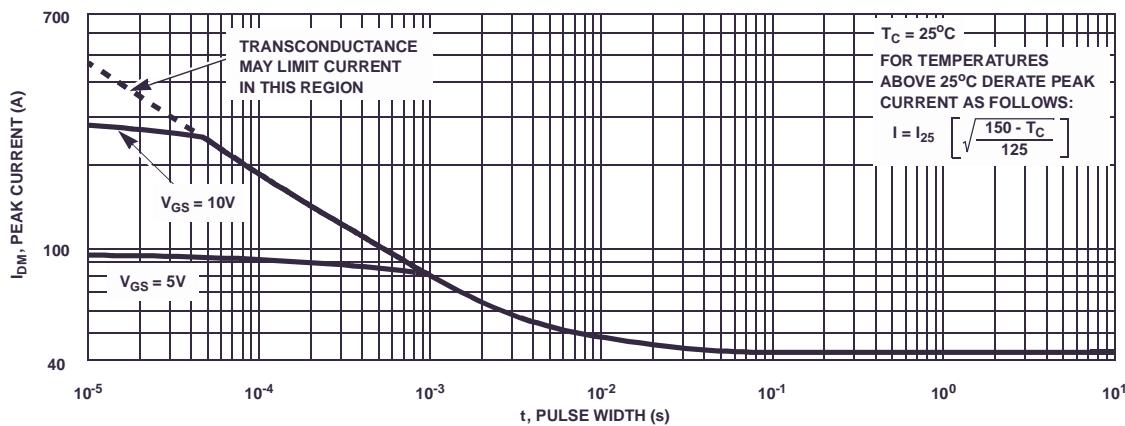


Figure 4. Peak Current Capability

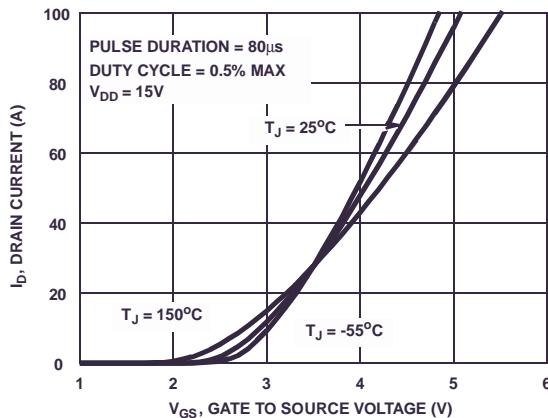
**Typical Characteristic**  $T_C = 25^\circ\text{C}$  unless otherwise noted (Continued)


Figure 5. Transfer Characteristics

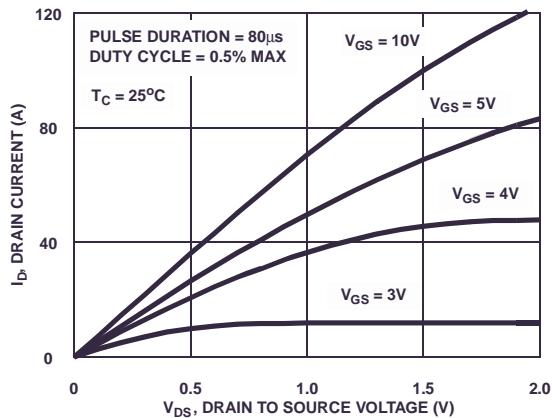


Figure 6. Saturation Characteristics

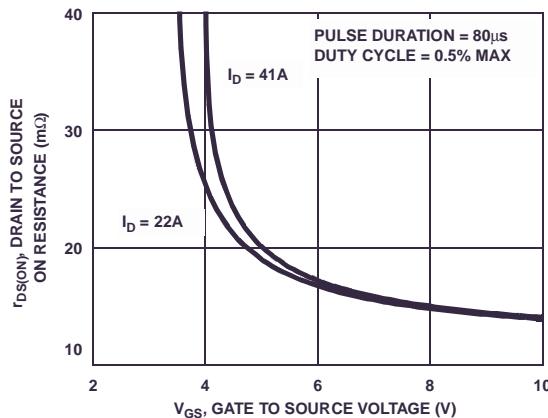


Figure 7. Drain to Source On Resistance vs Gate Voltage and Drain Current

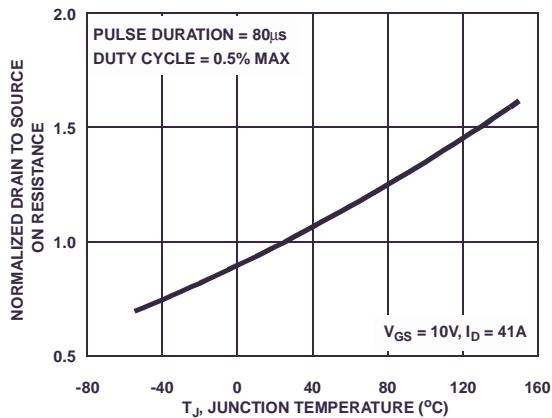


Figure 8. Normalized Drain to Source On Resistance vs Junction Temperature

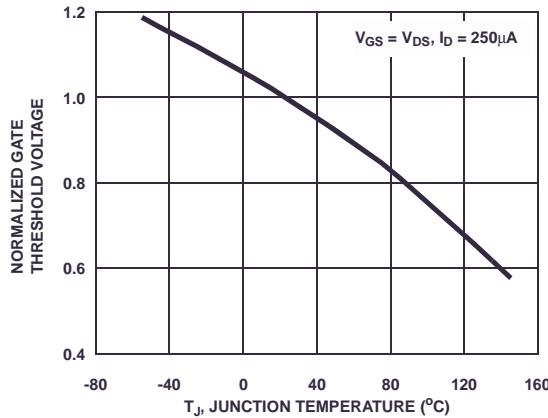


Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature

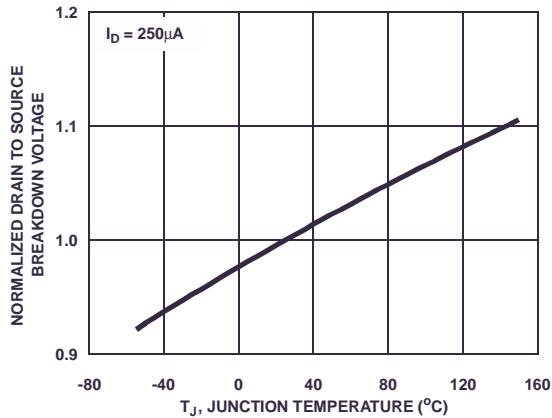


Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

### Typical Characteristic $T_C = 25^\circ\text{C}$ unless otherwise noted (Continued)

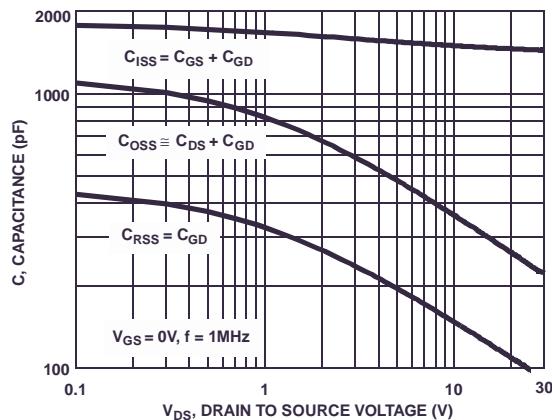


Figure 11. Capacitance vs Drain to Source Voltage

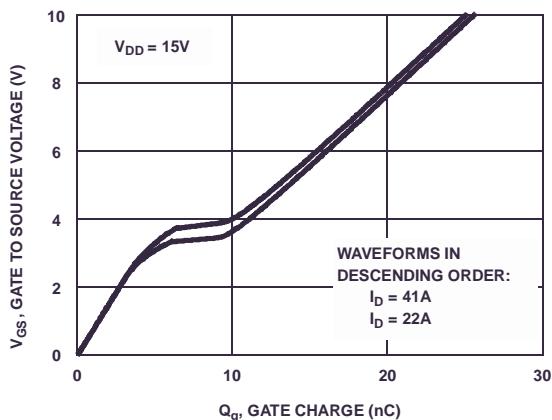


Figure 12. Gate Charge Waveforms for Constant Gate Currents

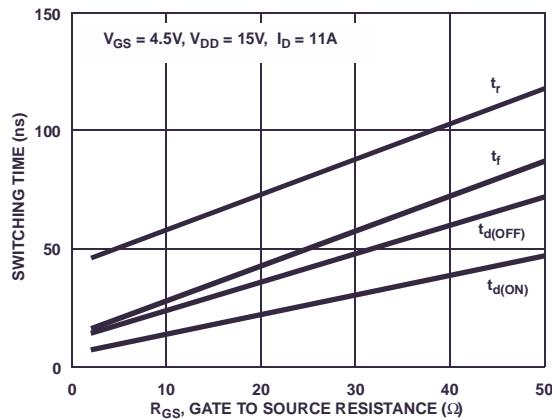


Figure 13. Switching Time vs Gate Resistance

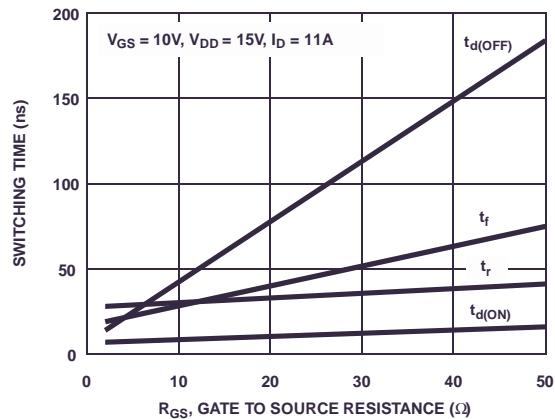


Figure 14. Switching Time vs Gate Resistance

### Test Circuits and Waveforms

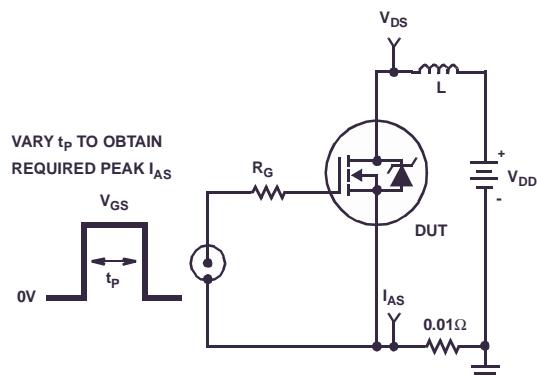


Figure 15. Unclamped Energy Test Circuit

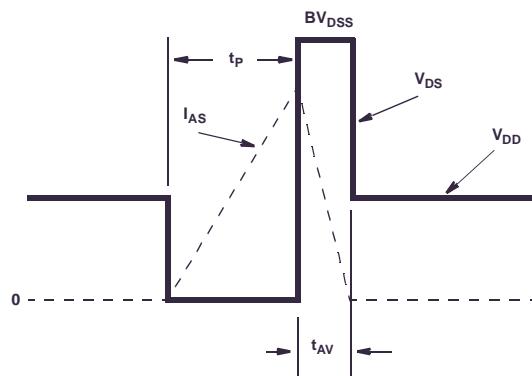


Figure 16. Unclamped Energy Waveforms

## Test Circuits and Waveforms (Continued)

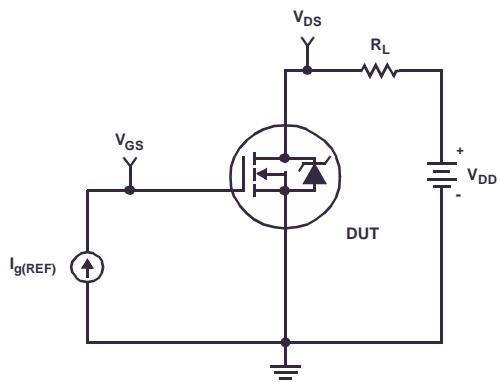


Figure 17. Gate Charge Test Circuit

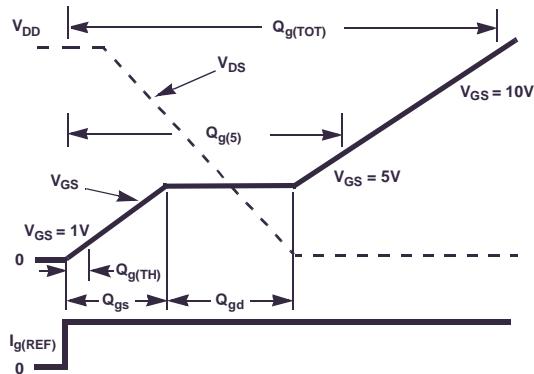


Figure 18. Gate Charge Waveforms

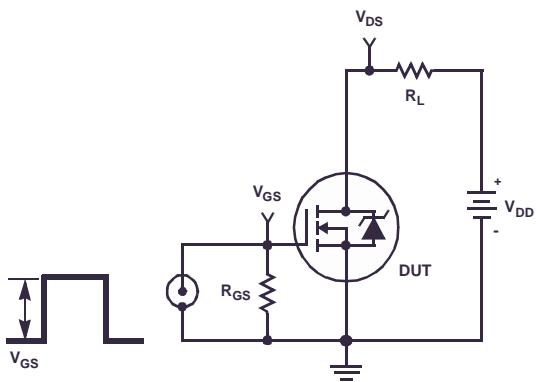


Figure 19. Switching Time Test Circuit

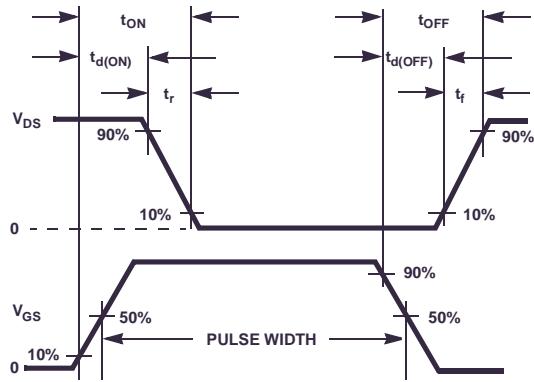


Figure 20. Switching Time Waveforms

**PSPICE Electrical Model**

.SUBCKT FQP45N03L 2 1 3 ; rev October 2002

CA 12 8 8e-10  
CB 15 14 1e-9  
CIN 6 8 1.35e-9

DBODY 7 5 DBODYMOD  
DBREAK 5 11 DBREAKMOD  
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 31.8  
EDS 14 8 5 8 1  
EGS 13 8 6 8 1  
ESG 6 10 6 8 1  
EVTHRES 6 21 19 8 1  
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
LGATE 1 9 6.24e-9  
LSOURCE 3 7 3.15e-9

MMED 16 6 8 8 MMEDMOD  
MSTRO 16 6 8 8 MSTROMOD  
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
RDRAIN 50 16 RDRAINMOD 2e-3  
RGATE 9 20 1.9  
RLDRAIN 2 5 10  
RLGATE 1 9 62.4  
RLSOURCE 3 7 31.5  
RSLC1 5 51 RSLCMOD 1e-6  
RSLC2 5 50 1e3  
RSOURCE 8 7 RSOURCEMOD 9.5e-3  
RVTHRES 22 8 RVTHRESMOD 1  
RVTEMP 18 19 RVTEMPPMOD 1

S1A 6 12 13 8 S1AMOD  
S1B 13 12 13 8 S1BMOD  
S2A 6 15 14 13 S2AMOD  
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*160),5))}

.MODEL DBODYMOD D (IS = 1.1e-11 N=1.075 RS = 8.9e-3 TRS1 = 9e-4 TRS2 = 1e-6 XTI=2.2 CJO = 7e-10 TT = 8e-11 M = 0.49)

.MODEL DBREAKMOD D (RS = 1.1 TRS1 = 1e-3 TRS2 = -8.9e-6)

.MODEL DPLCAPMOD D (CJO = 4.5e-10 IS = 1e-30 N = 10 M = 0.46)

.MODEL MMEDMOD NMOS (VTO = 1.9 KP = 6 IS=1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.9)

.MODEL MSTROMOD NMOS (VTO = 2.29 KP = 50 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)

.MODEL MWEAKMOD NMOS (VTO = 1.54 KP = 0.05 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 19 RS = 0.1)

.MODEL RBREAKMOD RES (TC1 = 1e-3 TC2 = -7e-7)

.MODEL RDRAINMOD RES (TC1 = 1.9e-2 TC2 = 3e-5)

.MODEL RSLCMOD RES (TC1 = 1e-3 TC2 = 1e-6)

.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)

.MODEL RVTHRESMOD RES (TC1 = -2.1e-3 TC2 = -1e-5)

.MODEL RVTEMPPMOD RES (TC1 = -1.8e-3 TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.0 VOFF= -0.8)

.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.8 VOFF= -4.0)

.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.3 VOFF= 0.2)

.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.2 VOFF= -0.3)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

## SABER Electrical Model

REV October 2002

```

template FQP45N03L n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl = 1.1e-11, rs = 8.9e-3, trs1 = 9e-4, trs2 = 1e-6, xti=2.2, cjo = 7e-10, tt = 8e-11, m = 0.49, n1=1.075)
dp..model dbreakmod = (rs = 1.1, trs1 = 1e-3, trs2 = -8.9e-6)
dp..model dplcapmod = (cjo = 4.5e-10, isl=10e-30, nl=10, m=0.46)
m..model mmmedmod = (type=_n, vto = 1.9, kp=6, is=1e-30, tox=1)
m..model mstrongmod = (type=_n, vto = 2.29, kp = 50, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.54, kp = 0.05, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -4.0, voff = -.8)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -.8, voff = -4.0)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -0.3, voff = 0.2)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.2, voff = -0.3) DPLCAP 5
c.ca n12 n8 = 8e-10
c.cb n15 n14 = 1e-9
c.cin n6 n8 = 1.35e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

I.ldrain n2 n5 = 1e-9
I.lgate n1 n9 = 6.24e-9
I.lsource n3 n7 = 3.15e-9

m.mmed n16 n6 n8 n8 = model=mmmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1 = 1e-3, tc2 = -7e-7
res.rdrain n50 n16 = 2e-3, tc1 = 1.9e-2, tc2 = 3e-5
res.rgate n9 n20 = 1.9
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 62.4
res.rsource n3 n7 = 31.5
res.rsrc1 n5 n51 = 1e-6, tc1 = 1e-3, tc2 = 1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 9.5e-3, tc1 = 1e-3, tc2 = 1e-6
res.rvtemp n18 n19 = 1, tc1 = -1.8e-3, tc2 = 1e-6
res.rvthres n22 n8 = 1, tc1 = -2.1e-3, tc2 = -1e-5

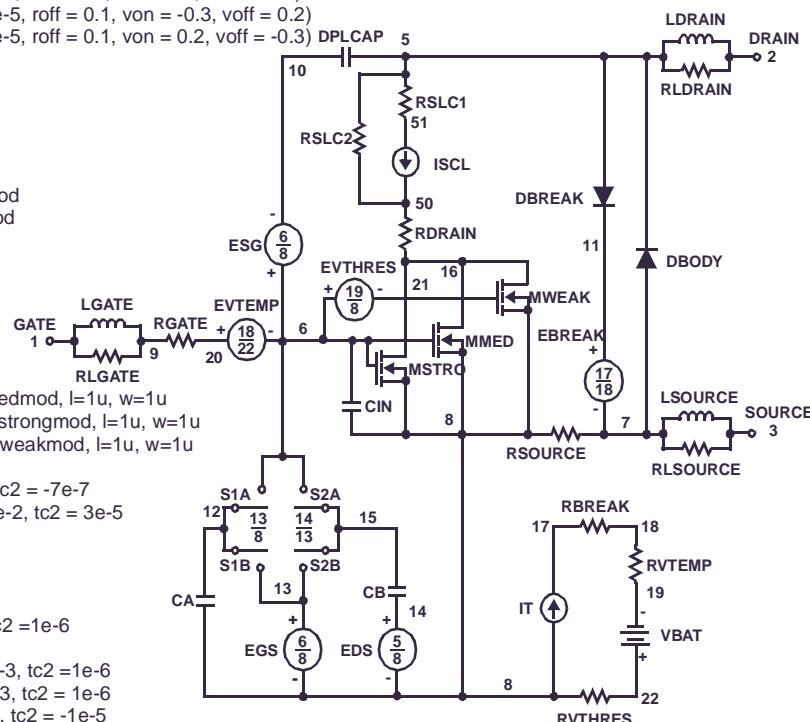
spe.ebreak n11 n7 n17 n18 = 31.8
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e-6/160))** 5))
}
}

```



**SPICE Thermal Model**

REV 23 October 2002

FQP45N03L\_THERMAL

```
CTHERM1 th 6 1.0e-3
CTHERM2 6 5 1.5e-3
CTHERM3 5 4 1.9e-3
CTHERM4 4 3 3e-3
CTHERM5 3 2 5e-3
CTHERM6 2 tl 2.5e-2
```

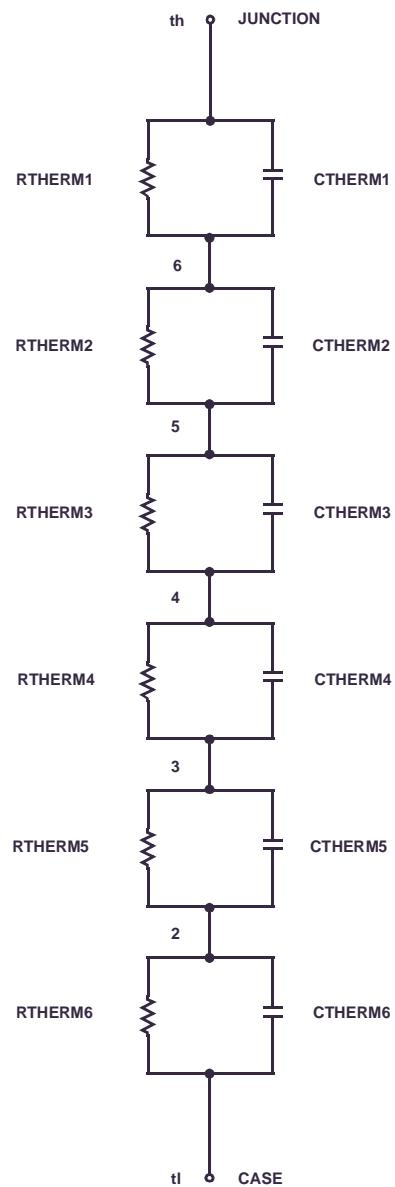
```
RTERM1 th 6 2.5e-3
RTERM2 6 5 3.5e-3
RTERM3 5 4 5.2e-2
RTERM4 4 3 5e-1
RTERM5 3 2 5.7e-1
RTERM6 2 tl 6.9e-1
```

**SABER Thermal Model**

SABER thermal model FQP45N03L\_THERMAL

```
template thermal_model th tl
thermal_c th, tl
{
  ctherm.ctherm1 th 6 = 1.0e-3
  ctherm.ctherm2 6 5 = 1.5e-3
  ctherm.ctherm3 5 4 = 1.9e-3
  ctherm.ctherm4 4 3 = 3e-3
  ctherm.ctherm5 3 2 = 5e-3
  ctherm.ctherm6 2 tl = 2.5e-2

  rtherm.rtherm1 th 6 = 2.5e-3
  rtherm.rtherm2 6 5 = 3.5e-3
  rtherm.rtherm3 5 4 = 5.2e-2
  rtherm.rtherm4 4 3 = 5e-1
  rtherm.rtherm5 3 2 = 5.7e-1
  rtherm.rtherm6 2 tl = 6.9e-1
}
```



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Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTR™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic™
E <sup>2</sup> CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I <sup>2</sup> C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCXTM
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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