N-Channel Enhancement Mode Power MOSFET

General Description

The YMP230N55 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

Features

- V_{DS}=55V；I_D=230A@ V_{GS}=10V；
  $R_{DS(ON)}$< 3 mΩ @ V_{GS} =10V
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

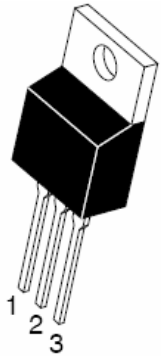
Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

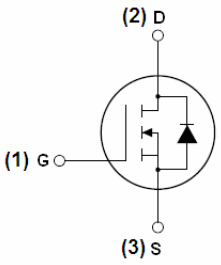
Product Summary

BV_{DSS}	typ.	55	V
$R_{DS(ON)}$	typ.	2	mΩ
	max.	3	mΩ
I_D		230	A

100% UIS TESTED!



TO-220-3L **top view**



Schematic diagram

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
YMP230N55	YMP230N55	TO-220-3L	-	-	-

Table 1. Absolute Maximum Ratings (TA=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V_{GS}=0V)	V_{DS}	55	V
Gate-Source Voltage (V_{DS}=0V)	V_{GS}	±25	V
Drain Current (DC) at Tc=25℃	$I_{D\ (DC)}$	230	A
Drain Current (DC) at Tc=100℃	$I_{D\ (DC)}$	170	A
Drain Current-Continuous@ Current-Pulsed (Note 1)	$I_{DM\ (pluse)}$	900	A
Maximum Power Dissipation(Tc=25℃)	P_D	300	W
Derating factor		1.33	W/℃
Single pulse avalanche energy (Note 2)	E_{AS}	2000	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition：Tj=25℃,V_{DD}=28V,VG=10V,L= 1mH ,R_g=25Ω;

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance，Junction-to-Case（Note2） ）	R_{thJC}	0.75	℃/W

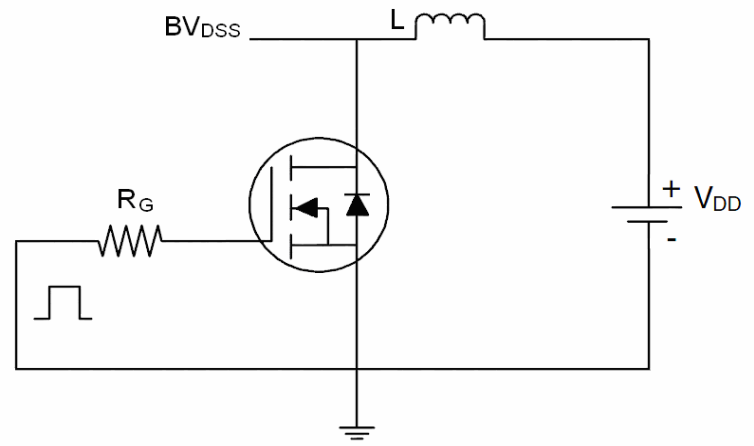
Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	55			V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{DSS}	V_{GS}=±25V,V_{DS}=0V			±100	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=10V,I_D=250μA	2	-	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=95A		2	3	mΩ
Dynamic Characteristics						
Forward Transconductance	g_{FS}	V_{DS}=25V,I_D=60A	106			S
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz		7360		PF
Output Capacitance	C_{oss}			1680		PF
Reverse Transfer Capacitance	C_{rss}			240		PF
Total Gate Charge	Q_g	V_{DS}=48V,I_D=95A, V_{GS}=10V		160		nC
Gate-Source Charge	Q_{gs}			35		nC
Gate-Drain Charge	Q_{gd}			42		nC
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=1A,R_L=30Ω		17	33	nS
Turn-on Rise Time	t_r			21	37	nS
Turn-Off Delay Time	$t_{d(off)}$	V_{GS}=10V,R_G= 3 Ω R_D=0.21Ω		72	148	nS
Turn-Off Fall Time	t_f			26	78	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}				95	A
Forward on voltage(Note 3)	V_{SD}	Tj=25℃,I_{SD}=20A,V_{GS}=0V		0.8	1.3	V
Reverse Recovery Time(Note 1)	t_{rr}	Tj=25℃,I_F=40A,di/dt=100A/μs		74		nS
Reverse Recovery Charge	Q_{rr}			140		nC
Forward Turn-on Time	t_{on}	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

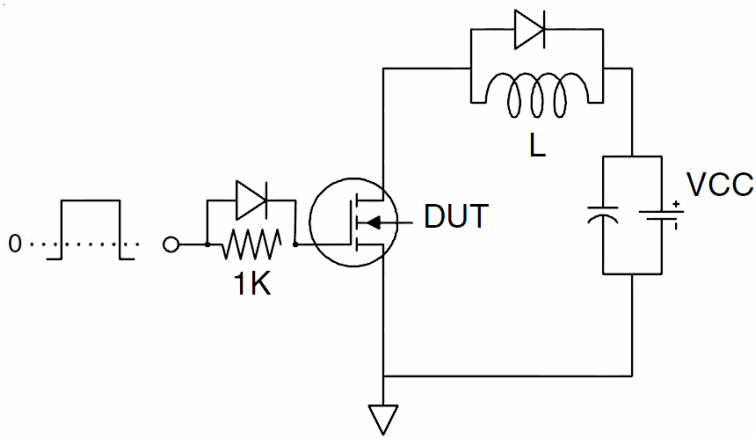
Notes 3.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%, R_G =25 Ω, Starting Tj=25℃

Test circuit

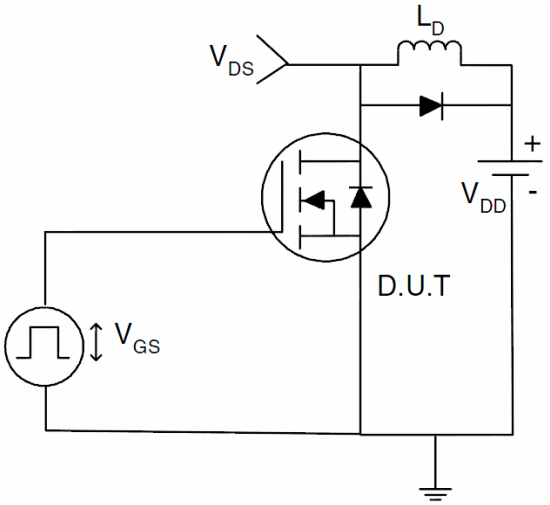
1）E_{AS} test Circuits



2）Gate charge test Circuit:

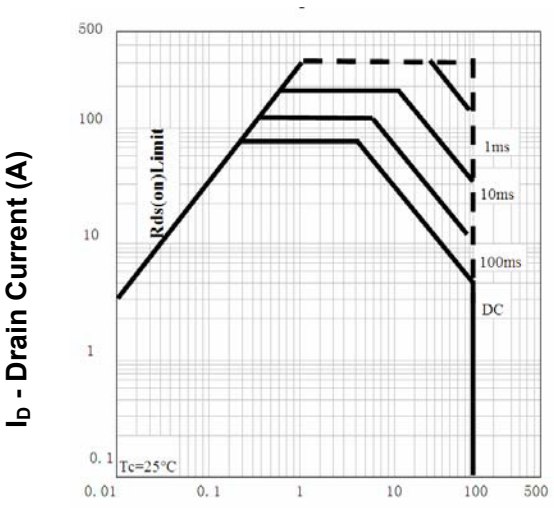


3）Switch Time Test Circuit：

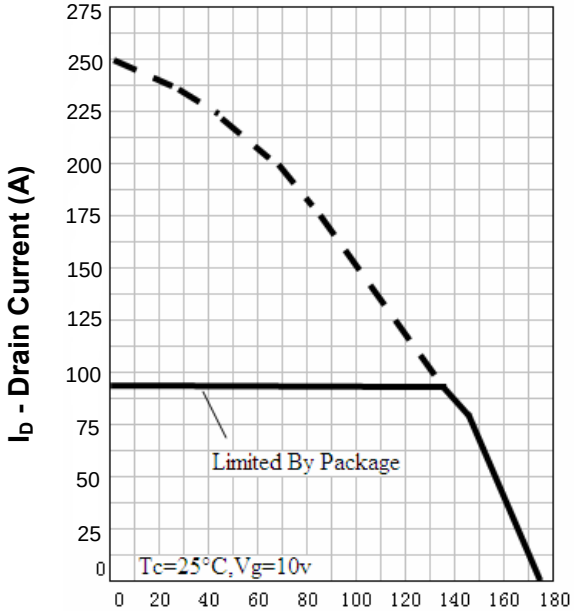


Typical Characteristics

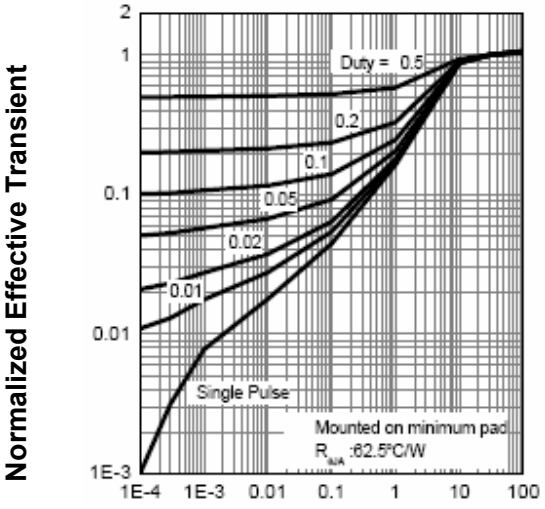
Safe Operation Area



Drain Current

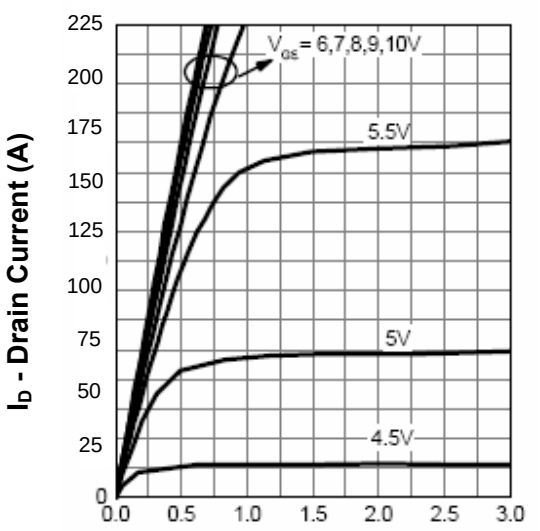


Thermal Transient Impedance

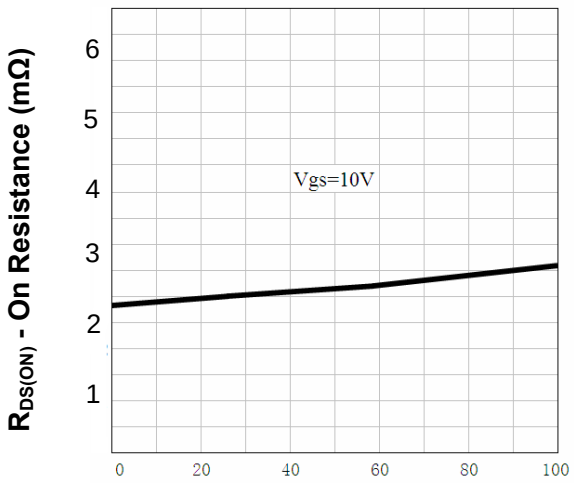


Typical Characteristics (Cont.)

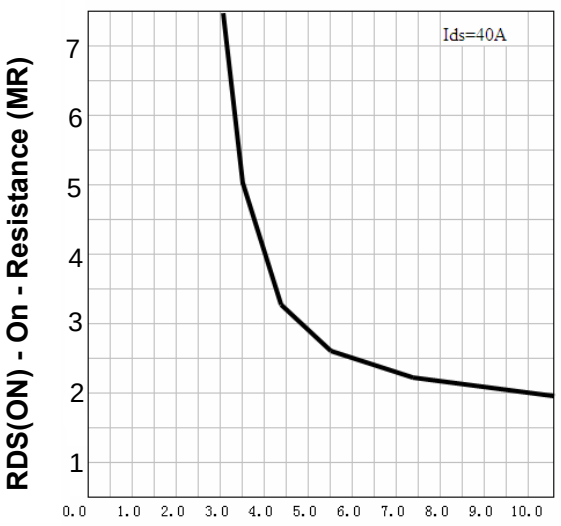
Output Characteristics



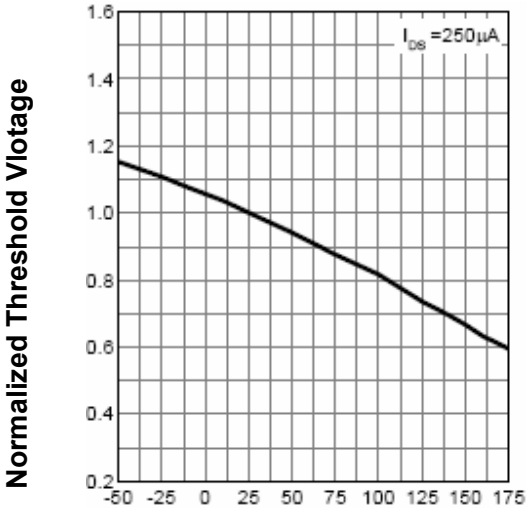
Drain-Source On Resistance



Drain-Source On Resistance

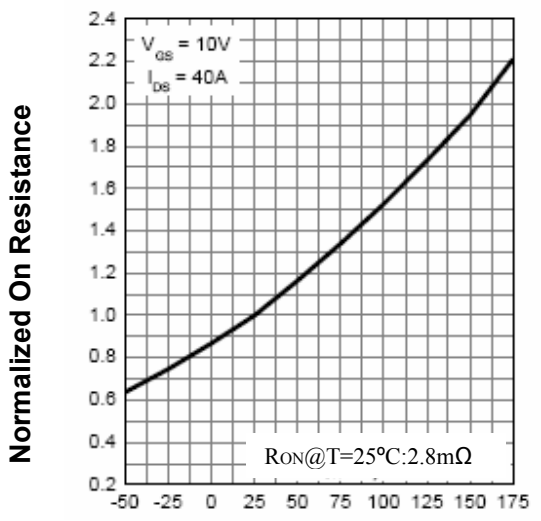


Gate Threshold Voltage

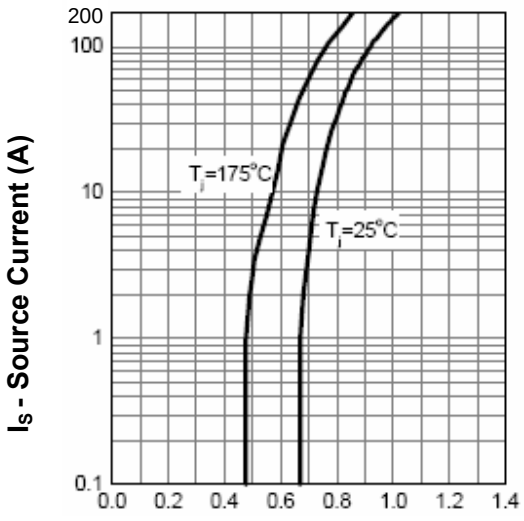


Typical Characteristics (Cont.)

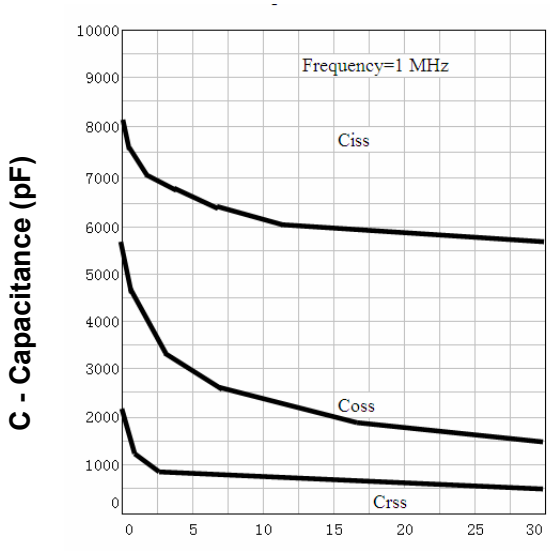
Drain-Source On Resistance



Source-Drain Diode Forward



Capacitance



Gate Charge