CLASS D AUDIO DRIVER

Features

- Hi-side and Lo-side independent floating PWM input
- Programmable bidirectional over-current detection with self-reset function
- Over current sensing output
- Shoot-through prevention logic
- High noise immunity
- ±100 V ratings deliver up to 500 W in output power
- 3.3 V / 5 V logic compatible input
- Operates up to 800 kHz

Product Summary

V_{OFFSET} (max)		± 100 V
Gate driver	Io+	2.0 A
	Io-	2.0 A
Propagation delay		120 ns
OC protection delay (max)		500 ns
Shutdown delay (max)		250 ns

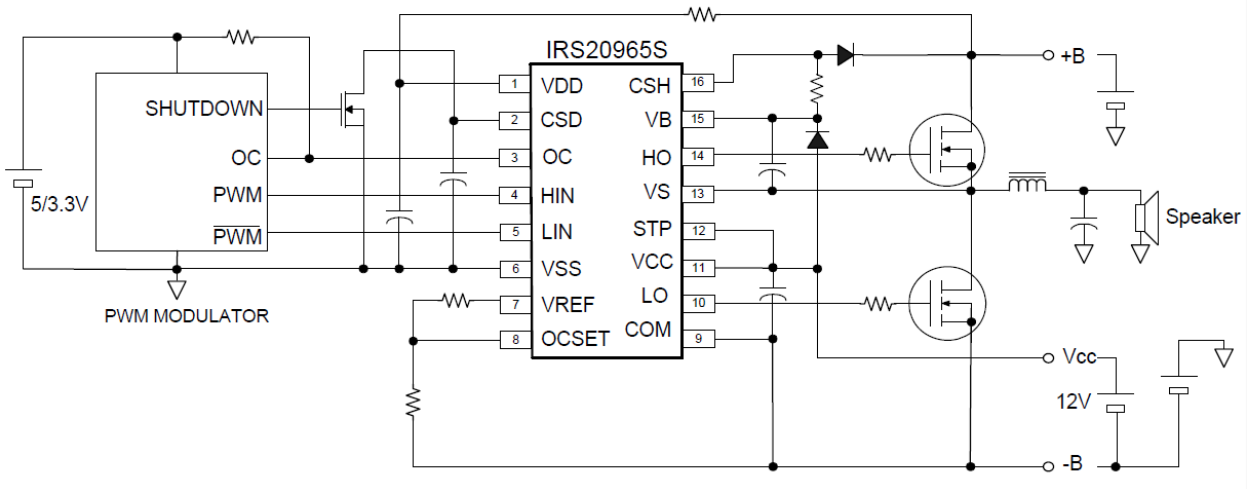
Typical Applications

- Class D audio amplifier
- Half bridge converter with digital controller

Package Options

16-Lead SOIC

Typical Connection Diagram



(Please refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only.)

Description

The IRS20965S is a high voltage, high speed MOSFET driver with floating PWM inputs designed for Class D audio amplifier applications.

Bi-directional current sensing using $R_{DS(ON)}$ of the MOSFETs detects over current conditions during positive and negative load currents without any external shunt resistors. An over current flag output provides over current status without shutting down, enabling full external control over OCP protection sequences.

Independent HIN and LIN inputs offers independent control on HO and LO. Internal shoot-thru prevention logic provides safe operation by eliminating simultaneous ON state in the output MOSFET.

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC16N	MSL2††† 260°C (per IPC/JEDEC J-STD-020)
ESD	**Machine Model**	Class B (per JEDEC standard EIA/JESD22-A115)	
	Human Body Model	Class 2 (per EIA/JEDEC standard JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78D)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS}; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	215	V
V_S	High side floating supply voltage †	V_B-20	V_B+0.3	
V_{HO}	High side floating output voltage	Vs-0.3	V_B+0.3	
V_{CSH}	CSH pin input voltage	Vs-0.3	V_B+0.3	
V_{CC}	Low side fixed supply voltage †	-0.3	20	
V_{LO}	Low side output voltage	-0.3	V_{CC} +0.3	
V_{DD}	Floating input supply voltage	-0.3	210	
V_{SS}	Floating input supply voltage †	(See I_{DDZ})	V_{DD}+0.3	
V_{HIN}	PWM input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{LIN}	PWM input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{CSD}	CSD pin input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{OC}	OC pin input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{OCSET}	OCSET pin input voltage	-0.3	V_{CC} +0.3	
V_{REF}	VREF pin voltage	-0.3	V_{CC} +0.3	
I_{DDZ}	Floating input supply zener clamp current †	-	10	mA
I_{CCZ}	Low side supply zener clamp current †	-	10	
I_{BSZ}	Floating supply zener clamp current †	-	10	
I_{OREF}	Reference output current	-	5	
dVs/dt	Allowable Vs voltage slew rate	-	50	V/ns
dVss/dt	Allowable Vss voltage slew rate ††	-	50	
dVss/dt	Allowable Vss voltage slew rate upon power-up †††	-	50	V/ms
Pd	Maximum power dissipation	-	1.0	W
Rth_{JA}	Thermal resistance, Junction to ambient	-	115	˚C/W
T_J	Junction Temperature	-	150	˚C
T_S	Storage Temperature	-55	150	
T_L	Lead temperature (Soldering, 10 seconds)	-	300	

† V_{DD} - V_{SS}, V_{CC} - COM, and V_B - V_S contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

†† For the rising and falling edges of step signal of 10V. V_{SS} = 15V to 200V.

††† V_{SS} ramps up from 0V to 200V.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at I_{DD} = 3mA, V_{CC} = 12V and V_B - V_S = 12V.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	Vs+10	Vs+14	V
V_S	High side floating supply offset voltage	†	200	
I_{DDZ}	Floating input supply zener clamp current	1	5	mA
V_{OC}	OC pin input voltage	V_{SS}	V_{DD}	V
V_{SS}	Floating input supply absolute voltage	0	100	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	15	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{HIN}	HIN PWM input voltage	V_{SS}	V_{DD}	
V_{LIN}	LIN PWM input voltage	V_{SS}	V_{DD}	
V_{CSD}	CSD pin input voltage	V_{SS}	V_{DD}	
I_{OREF}	Reference output current to COM ††	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
T_A	Ambient Temperature	-40	125	˚C

† Logic operational for Vs equal to -5V to +200V. Logic state held for Vs equal to -5V to $-V_{BS}$.

†† Nominal voltage for V_{REF} is 5V. I_{OREF} of 0.3 – 0.8 mA dictates total external resistor value on VREF to be 6.3k to 16.7kΩ.

Electrical Characteristics

V_{CC}, V_{BS}= 12 V, I_{DD}=3mA, V_{SS}=20V, C_L=1nF, STP=VCC and T_A=25˚C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Supply						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
I_{QCC}	Low side quiescent current	-	-	1	mA	V_{DT} =Vcc
V_{CLAMPL}	Low side zener diode clamp voltage	19.6	20.4	21.6	V	I_{CC}=5mA
High Side Floating Supply						
UV_{BS+}	High side well UVLO positive threshold	8.0	8.5	9.0	V	
UV_{BS-}	High side well UVLO negative threshold	7.8	8.3	8.8	V	
I_{QBS}	High side quiescent current	-	-	1	mA	
I_{LKH}	High to Low side leakage current	-	-	50	µA	V_B=V_S =200V
V_{CLAMPH}	High side zener diode clamp voltage	14.7	15.3	16.2	V	I_{BS}=5mA
Floating Input Supply						
UV_{DD+}	V_{DD}, V_{SS} floating supply UVLO positive threshold	8.2	8.7	9.2	V	V_{SS} =0V
UV_{DD-}	V_{DD}, V_{SS} floating supply UVLO negative threshold	7.7	8.2	8.7	V	V_{SS} =0V
I_{QDD}	Floating Input quiescent current	-	-	1	mA	V_{DD}=9.5V +Vss
V_{CLAMPM}	Floating Input zener diode clamp voltage	9.8	10.2	10.8	V	I_{DD}=5mA
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{DD}=V_{SS} =200V
Floating PWM Input						
V_{IH}	Logic “1” input threshold voltage	2.3	1.9	-	V	
V_{IL}	Logic “0” input threshold voltage	-	1.9	1.5	V	
I_{IN+}	Logic “1” input bias current	-	-	40	µA	V_{IN} =3.3V
I_{IN-}	Logic “0” input bias current	-	-	1	µA	V_{IN} = V_{SS}

Electrical Characteristics (cont'd)

V_{CC},V_{BS}= 12 V, I_{DD}=3mA, V_{SS}=20V, C_L=1nF, STP=VCC and T_A=25˚C unless otherwise specified.

Protection						
V_{REF}	Reference output voltage	4.8	5.1	5.4	V	I_{OREF} =0.5mA
Vth_{OCL}	Low side OC threshold in Vs	1.1	1.2	1.3	V	OCSET=1.2V
Vth_{OCH}	High side OC threshold in V_{CSH}	1.1+ Vs	1.2+ Vs	1.3+ Vs	V	
Vth1	CSD pin shutdown release threshold	0.62 x V_{DD}	0.70 x V_{DD}	0.78 x V_{DD}	V	V_{SS} =0V
Vth2	CSD pin self reset threshold	0.26 x V_{DD}	0.30 x V_{DD}	0.34 x V_{DD}	V	V_{SS} =0V
I_{CSD+}	CSD pin charge current	70	100	130	µA	V_{SD} = V_{SS} +5V
I_{CSD-}	CSD pin discharge current	70	100	130	µA	V_{SD} = V_{SS} +5V
I_{OCC}	OC output sink current	10	-	-	mA	Voc=1V
		1	-	-	mA	Voc=0.1V
t_{OCL}	Propagation delay time from Vs> Vth_{OCL} to Shutdown	-	-	500	ns	
t_{OCH}	Propagation delay time from V_{CSH} > Vth_{OCH} to Shutdown	-	-	500	ns	
PW_{OC}	OC output minimum pulse width	1	-	-	µs	
Gate Driver						
Io+	Output high short circuit current (Source)		2.0	-	A	Vo=0V, PW≤10µS
Io-	Output low short circuit current (Sink)		2.0	-	A	Vo=12V, PW≤10µS
V_{OL}	Low level output voltage LO – COM, HO - VS	-	-	0.1	V	
V_{OH}	High level output voltage VCC – LO, VB - HO	-	-	1.4	V	Io=0A
tr	Turn-on rise time	-	15	-	ns	
tf	Turn-off fall time	-	15	-	ns	
ton_1	High and low side turn-on propagation delay, floating inputs	-	120	-	ns	V_S = 100V, V_{SS} = 100V
toff_1	High and low side turn-off propagation delay, floating inputs	-	120	-	ns	
ton_2	High and low side turn-on propagation delay, non-floating inputs	-	130	-	ns	
toff_2	High and low side turn-off propagation delay, non-floating inputs	-	130	-	ns	
DT	Intrinsic dead-time: LO turn-off to HO turn-on ($DT_{LO-HO)}$ & HO turn-off to LO turn-on (DT_{HO-LO})	0	10	20	ns	
PWmin	Minimum pulse width for outputs to respond. Positive or Negative.	-	25	-	ns	V_S = COM V_{SS} = COM
OWmin	Allowable LO/HO over wrap	10	-	-	ns	

Waveform Definitions

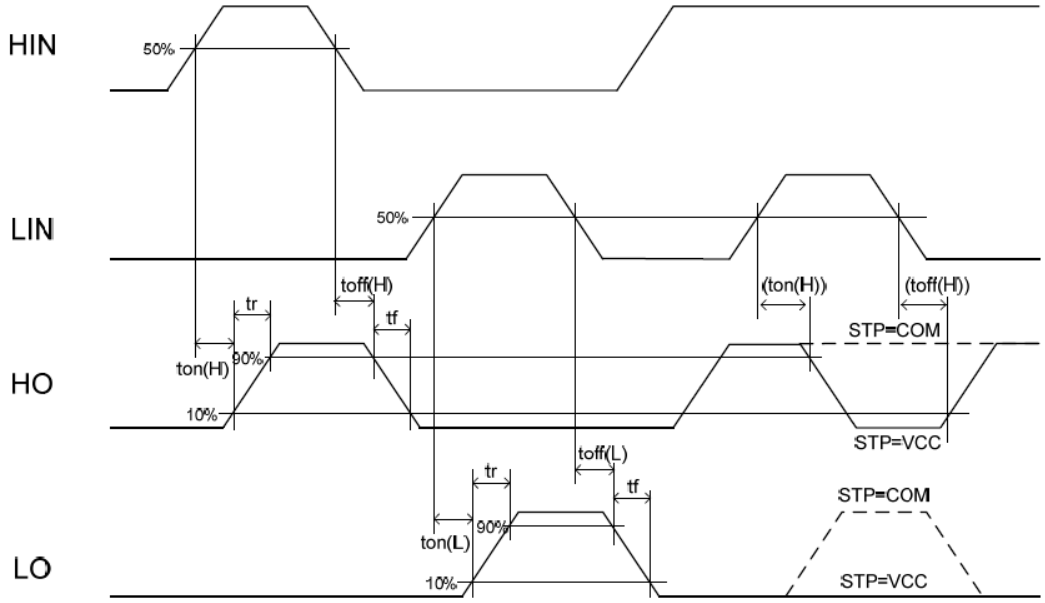


Figure 1: Timing Diagram

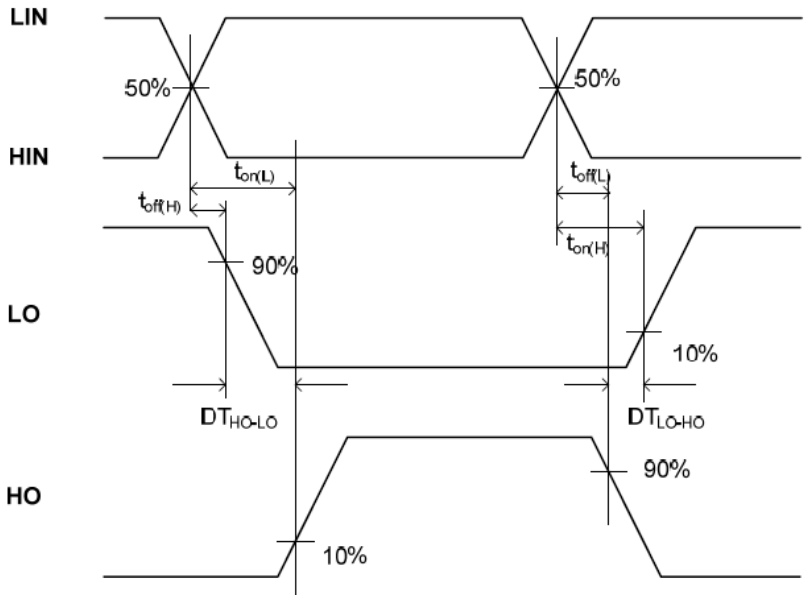


Figure 2: Deadtime Waveform Definitions

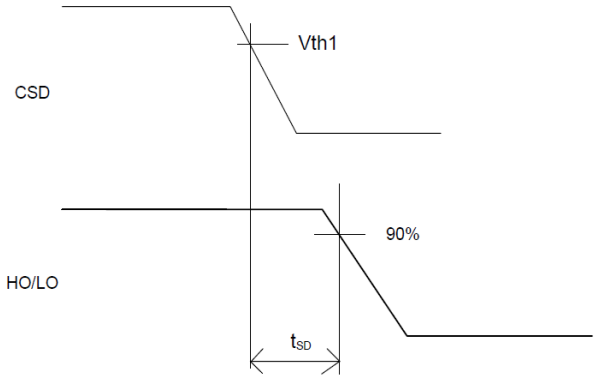


Figure 3: CSD to Shutdown Waveform Definitions

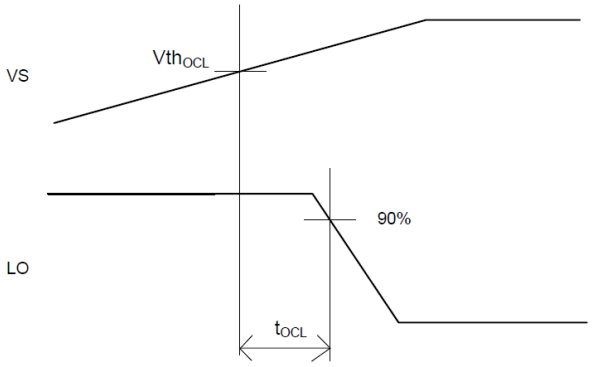


Figure 4: V_S > Vth_{OCL} to Shutdown Waveform

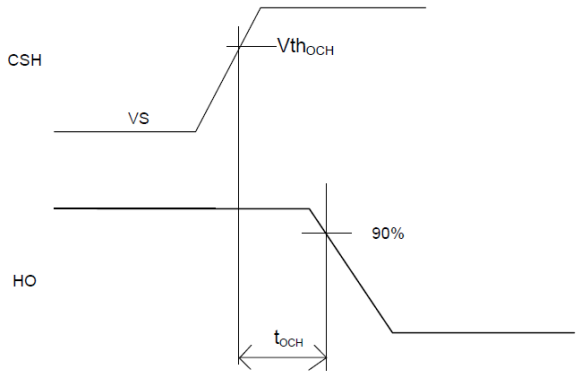
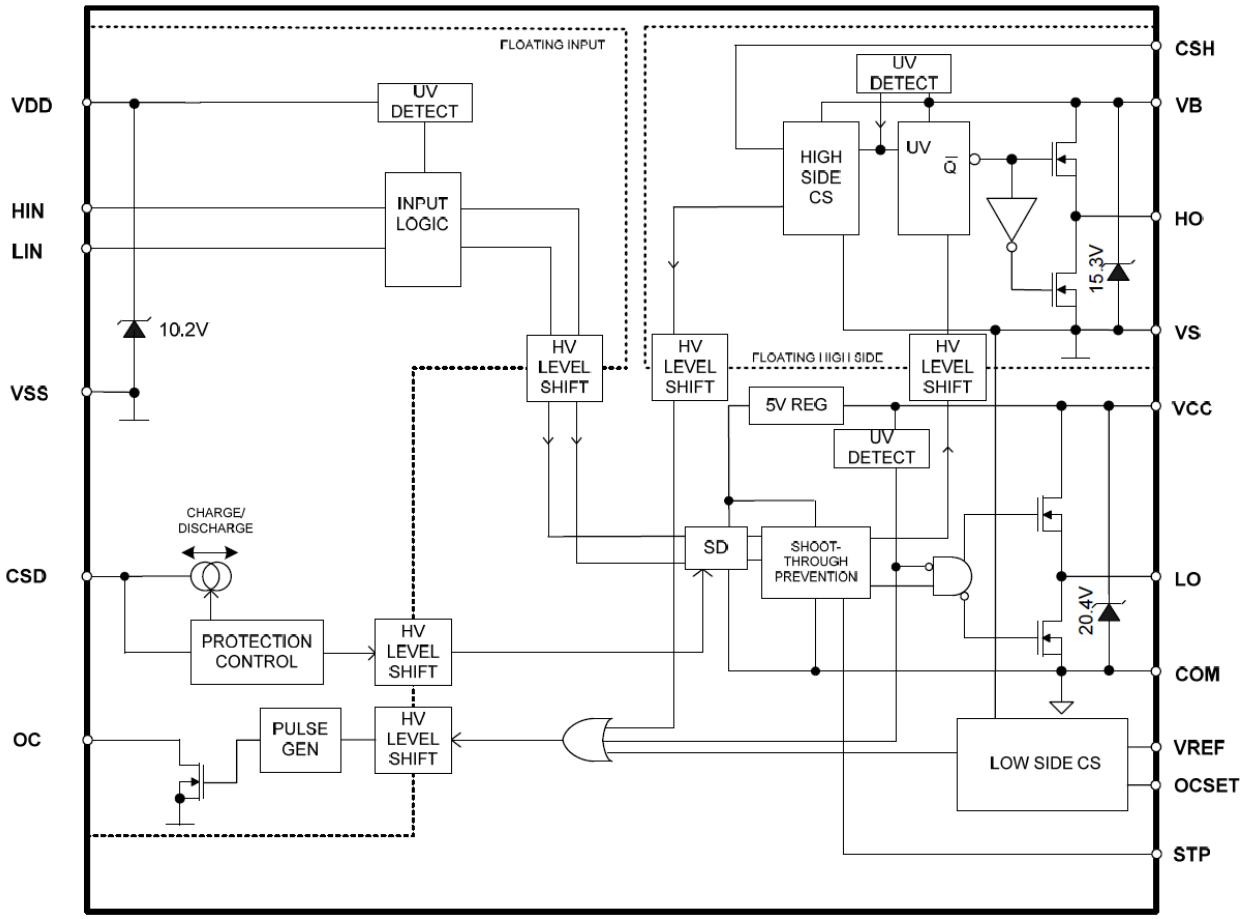
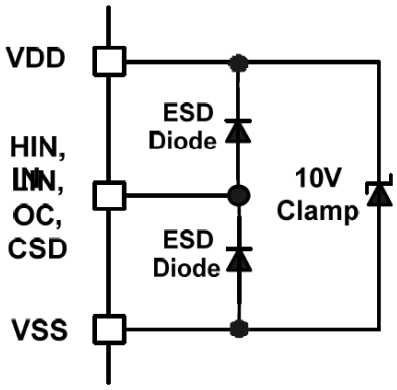


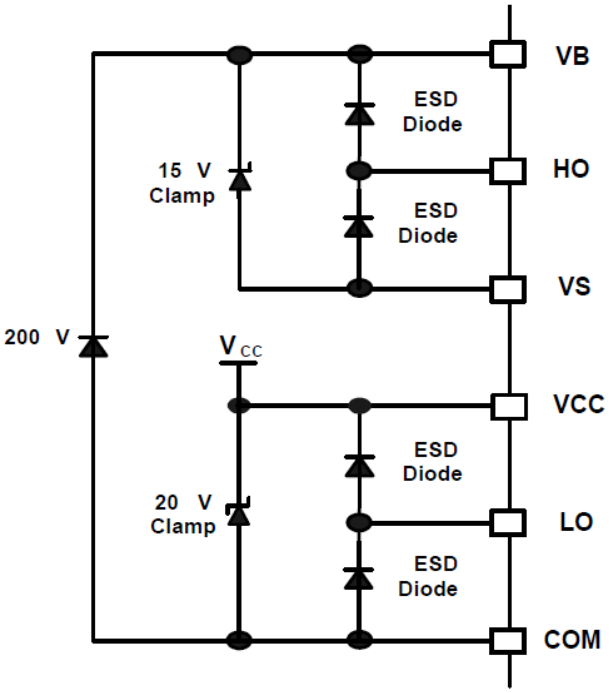
Figure 5: V_{CSH} > Vth_{OCH} to Shutdown Waveform

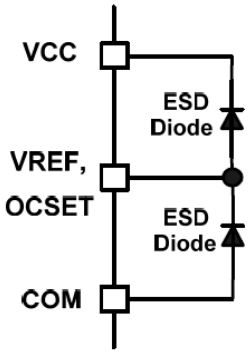
Functional Block Diagram

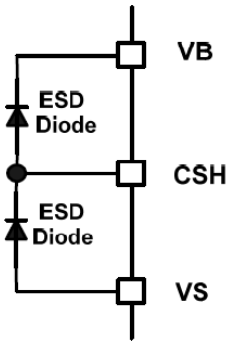


Input/Output Pin Equivalent Circuit Diagrams:





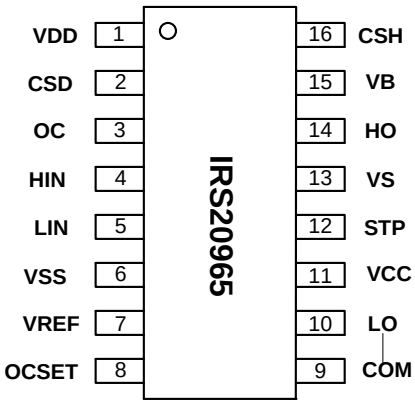




Lead Definitions

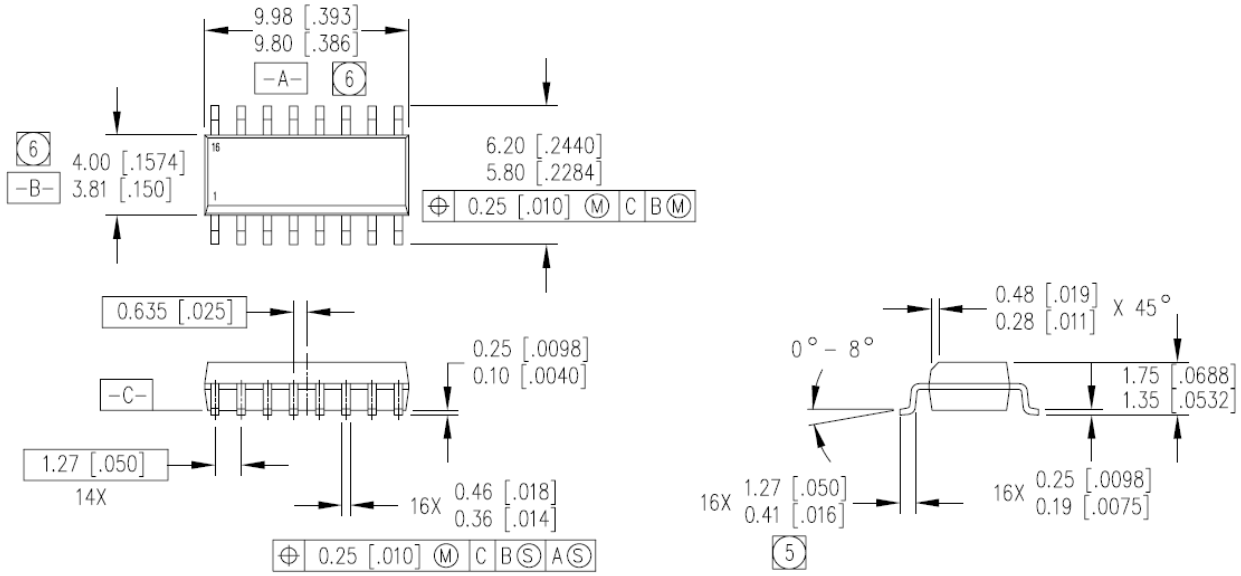
Pin #	Symbol	Description
1	VDD	Floating input positive supply
2	CSD	Shutdown timing capacitor, referenced to VSS
3	OC	Over current warning output, open drain referenced to VSS
4	HIN	PWM input, in phase with HO, referenced to VSS
5	LIN	PWM input, in phase with LO, referenced to VSS
6	VSS	Floating input supply return
7	VREF	5V reference output for setting OCSET, reference to COM
8	OCSET	Low side over current threshold setting, referenced to COM
9	COM	Low side supply return
10	LO	Low side output
11	VCC	Low side logic supply
12	STP	Shoot-thru prevention logic override (VCC: enabled, COM: disabled)
13	VS	High side floating supply return
14	HO	High side output
15	VB	High side floating supply
16	CSH	High side over current sensing input, referenced to VS

Lead Assignments



SOIC16N

Package Details: SOIC16N



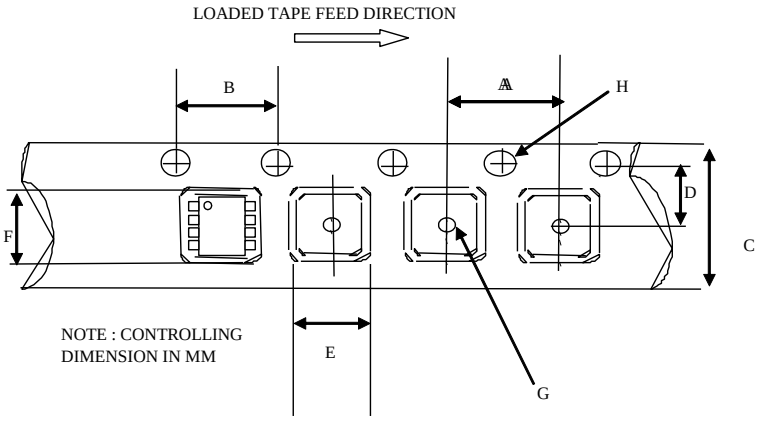
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC.

5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

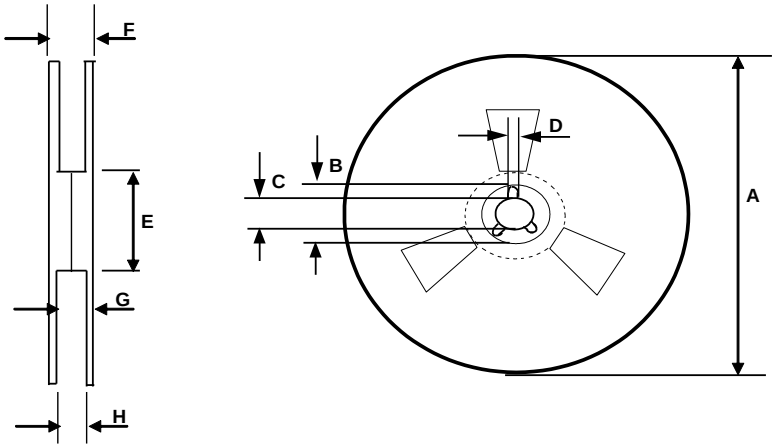
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

Tape and Reel Details: SOIC16N



CARRIER TAPE DIMENSION FOR 16SOICN

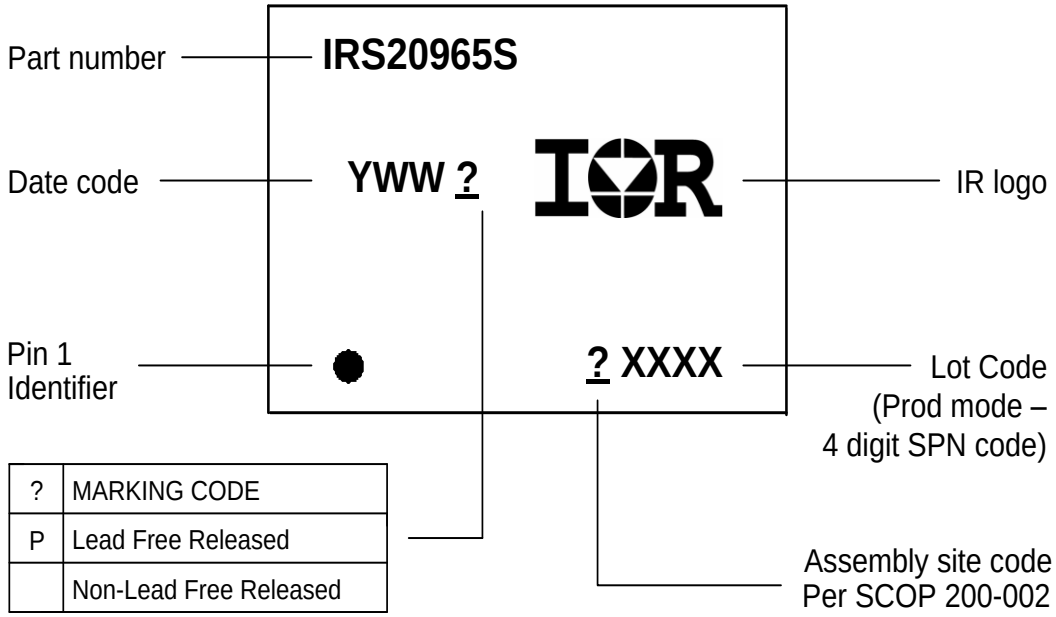
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS20965SPBF	SO16N	Tube/Bulk	45	IRS20965SPBF
		Tape and Reel	2500	IRS20965STRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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