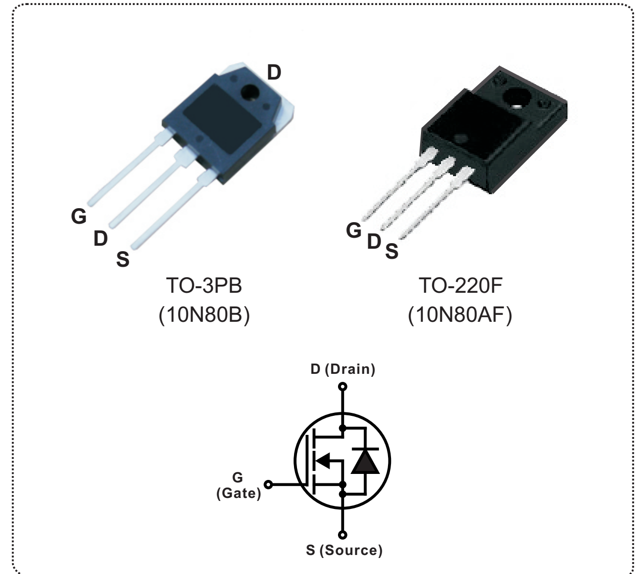
N-Channel Power MOSFET
10A, 800Volts

DESCRIPTION

The Nell **10N80** is a three-terminal silicon device with current conduction capability of 10A, fast switching speed, low on-state resistance, breakdown voltage rating of 800V, and max. threshold voltage of 5 volts.

They are designed for use in applications such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits and general purpose switching applications.



FEATURES

- $R_{DS(ON)}$ = 1.1Ω @ V_{GS} = 10V
- Ultra low gate charge(58nC max.)
- Low reverse transfer capacitance (C_{RSS} = 15pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature

PRODUCT SUMMARY	
I_D (A)	10
V_{DSS} (V)	800
$R_{DS(ON)}$ (Ω)	1.1 @ V_{GS} = 10V
Q_G(nC) max.	58

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		VALUE	UNIT
V_{DSS}	Drain to Source voltage	T_J=25°C to 150°C		800	V
V_{DGR}	Drain to Gate voltage	R_{GS}=20KΩ		800	
V_{GS}	Gate to Source voltage			±30	
I_D	Continuous Drain Current	T_C=25°C		10	A
		T_C=100°C		6.2	
I_{DM}	Pulsed Drain current(Note 1)			40	
I_{AR}	Avalanche current(Note 1)			10	
E_{AR}	Repetitive avalanche energy(Note 1)	I_{AR}=10A, R_{GS}=50Ω, V_{GS}=10V		24	mJ
E_{AS}	Single pulse avalanche energy(Note 2)	I_{AS}=10A, L=17.3mH		920	
dv/dt	Peak diode recovery dv/dt(Note 3)			4	V /ns
P_D	Total power dissipation	T_C=25°C	TO-3PB	240	W
			TO-220F	37	
	Linear derating factor above T_C=25°C	T_C=25°C	TO-3PB	1.92	°C/W
			TO-220F	0.296	
T_J	Operation junction temperature			-55 to 150	°C
T_{STG}	Storage temperature			-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case		300	
	Mounting torque, #6-32 or M3 screw			10 (1.1)	lbf·in (N·m)

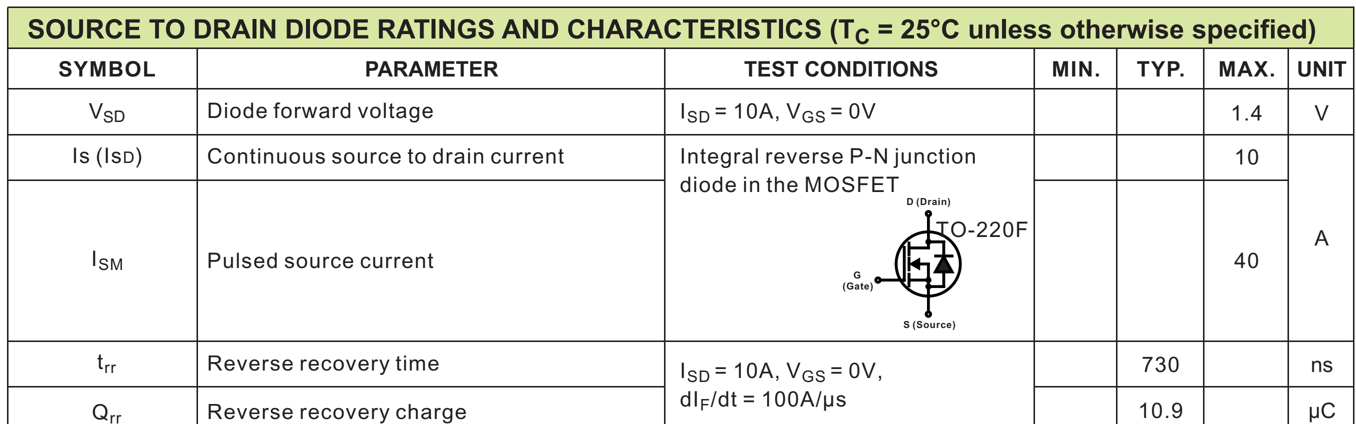
Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.I_{AS}=10A, L=17.3mH, V_{DD}=50V, R_{GS}=25Ω, starting T_J =25°C.
3.I_{SD} ≤ 10A, di/dt ≤ 200A/μs, V_{DD} ≤ $V_{(BR)DSS}$, starting T_J = 25°C.

THERMAL RESISTANCE

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-3PB			0.52	°C/W
		TO-220F			3.4	
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-3PB			40	
		TO-220F			62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
◎ OFF CHARACTERISTICS						
$V_{(BR)DSS}$	Drain to source breakdown voltage	I_D = 250μA, V_{GS} = 0V	800			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	I_D = 250μA, V_{DS} = V_{GS}		0.98		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=800V, V_{GS}=0V, T_C=25°C			10	μA
		V_{DS}=640V, V_{GS}=0V, T_C=125°C			100	
I_{GSS}	Gate to source forward leakage current	V_{GS} = 30V, V_{DS} = 0V			100	nA
	Gate to source reverse leakage current	V_{GS} = -30V, V_{DS} = 0V			-100	
◎ ON CHARACTERISTICS						
$R_{DS(ON)}$	Static drain to source on-state resistance	V_{GS}=10V, I_D=5A		0.9	1.1	Ω
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS}, I_D=250μA	3		5	V
◎ DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		2150	2800	pF
C_{OSS}	Output capacitance			180	230	
C_{RSS}	Reverse transfer capacitance			15	20	
◎ SWITCHING CHARACTERISTICS						
$t_{d(ON)}$	Turn-on delay time	V_{DD}=400V, V_{GS}=10V I_D=10A, R_{GS}=25Ω (Note1,2)		50	110	ns
t_r	Rise time			130	270	
$t_{d(OFF)}$	Turn-off delay time			90	190	
t_f	Fall time			80	170	
Q_G	Total gate charge	V_{DD}= 640V, V_{GS}=10V I_D=10A, (Note1,2)		45	58	nC
Q_{GS}	Gate to source charge			13.5		
Q_{GD}	Gate to drain charge (Miller charge)			17		



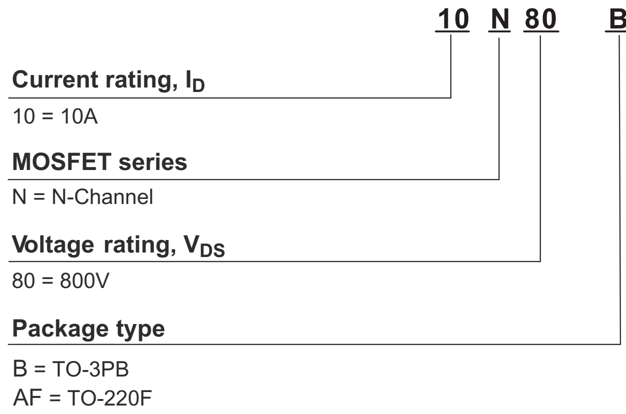
SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 10A, V_{GS} = 0V			1.4	V
Is (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET TO-220F D (Drain) G (Gate) S (Source)			10	A
I_{SM}	Pulsed source current				40	
t_{rr}	Reverse recovery time	I_{SD} = 10A, V_{GS} = 0V, dI_F/dt = 100A/μs		730		ns
Q_{rr}	Reverse recovery charge			10.9		μC

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME



■ TEST CIRCUITS

Fig.1A Peak diode recovery dv/dt test circuit

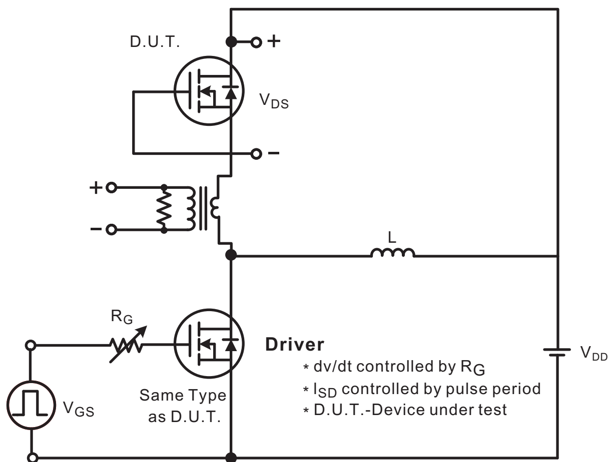
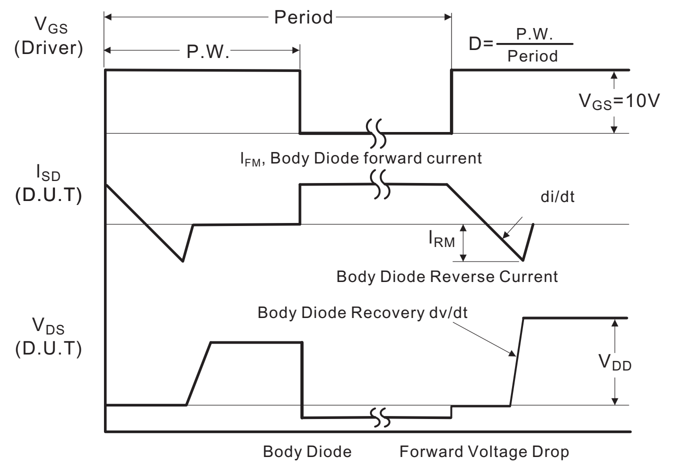


Fig.1B Peak diode recovery dv/dt waveforms



■ TEST CIRCUIT(Cont.)

Fig.2A Switching test circuit

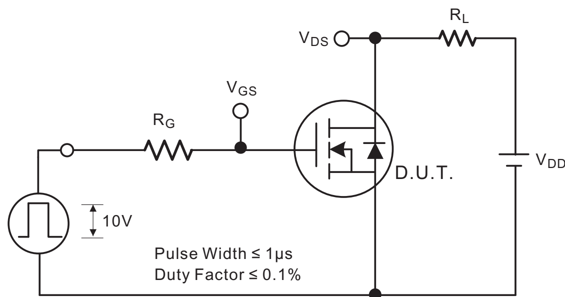


Fig.2B Switching Waveforms

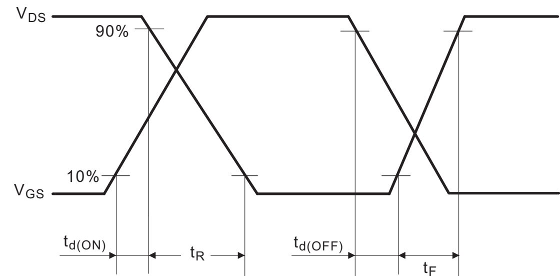


Fig.3A Gate charge test circuit

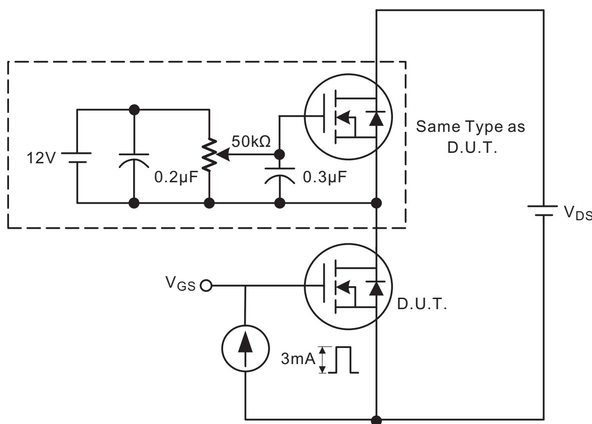


Fig.3B Gate charge waveform

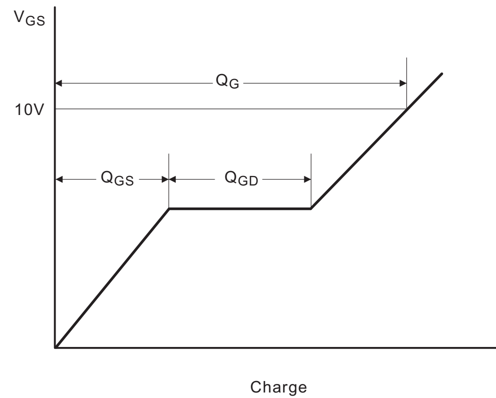


Fig.4A Unclamped Inductive switching test circuit

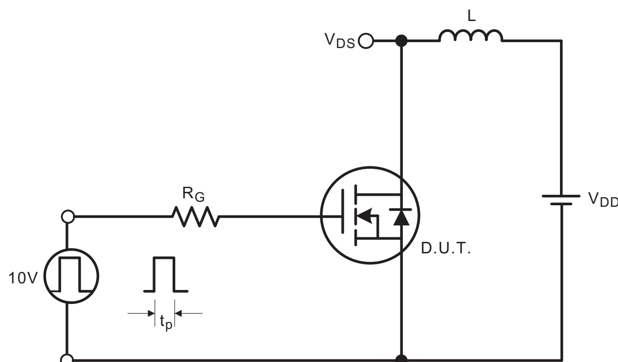
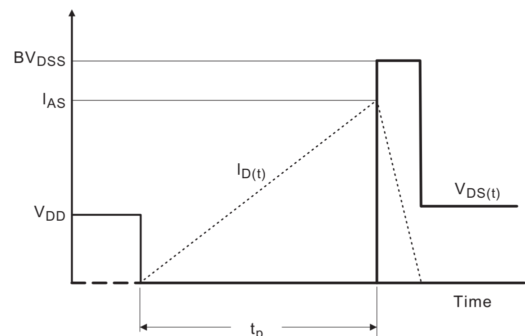


Fig.4B Unclamped Inductive switching waveforms



■ TYPICAL CHARACTERISTICS

Fig.1 Drain current vs. Source to drain voltage

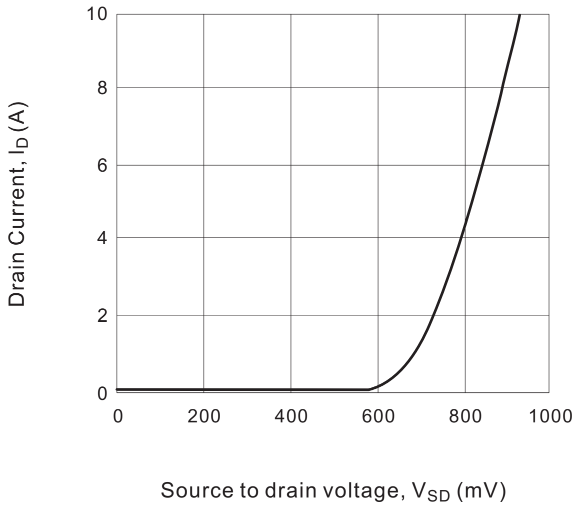


Fig.2 Drain-source on-state resistance characteristics

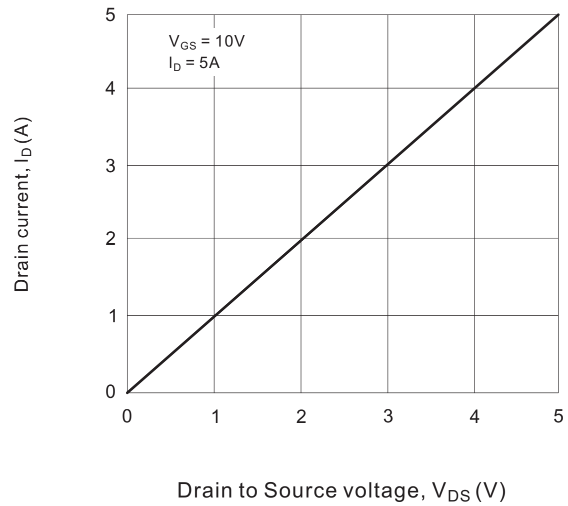


Fig.3 Drain current vs. Gate threshold voltage

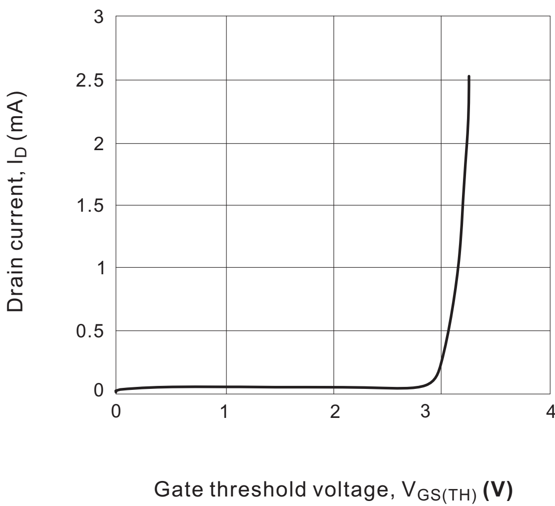
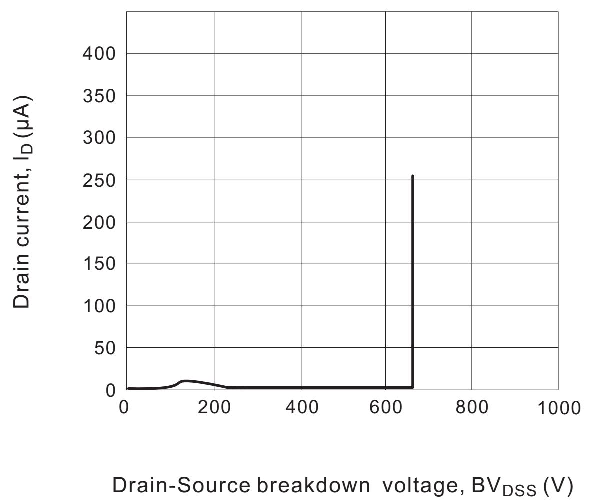
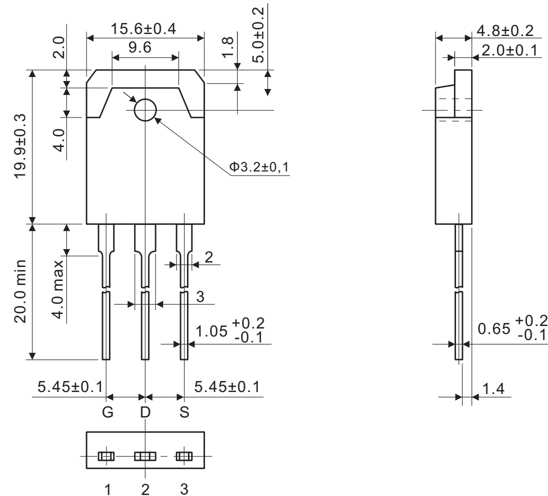
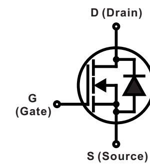


Fig.4 Drain current vs. Drain-Source breakdown voltage



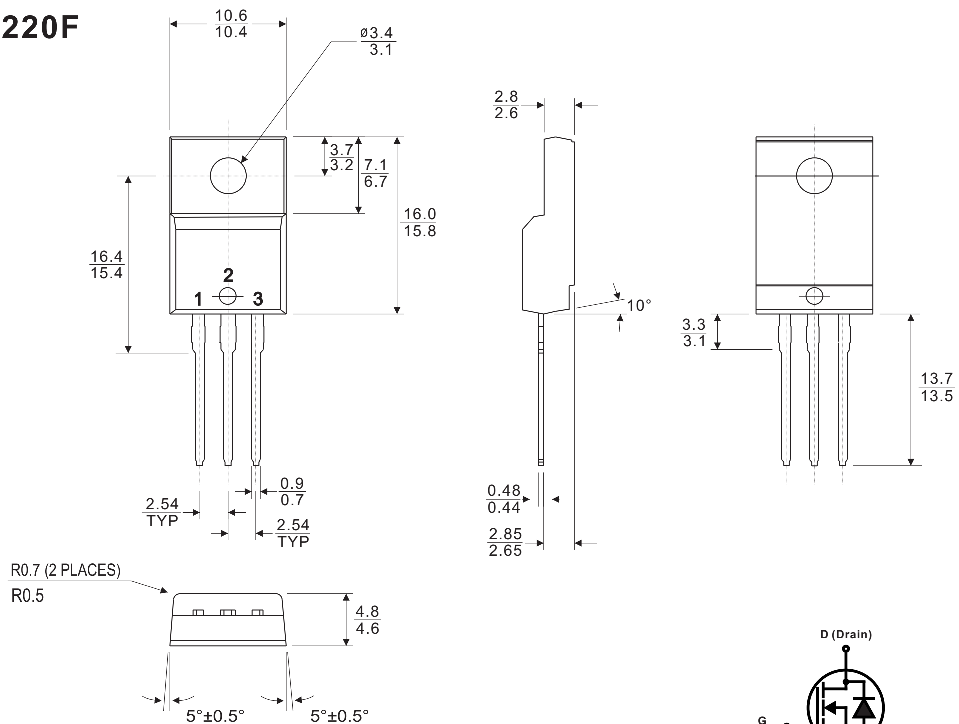
TO-3PB

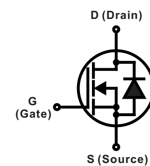




All dimensions in millimeters

TO-220F





All dimensions in millimeters