



Z86C95

CMOS Z8® DIGITAL SIGNAL PROCESSOR (DSP)

GENERAL DESCRIPTION

The Z86C95 MCU (Microcontroller Unit) introduces a new level of sophistication to Superintegration™ ICs. The Z86C95 is a member of the Z8® single-chip microcontroller family incorporating a CMOS ROMless Z8 microcontroller with an embedded DSP processor for digital servo control. The DSP slave processor can perform 16-bit x 16-bit multiplies and accumulates in one clock cycle. Additionally, the Z86C95 is further enhanced with a hardwired 16-bitx16-bit multiplier and a 32-bit/16-bit divider, three 16-bit counter timers with capture and compare registers, a half flash 8-channel 8-bit A/D converter with a 2 μsec conversion time, an 8-bit DAC with 1/4 programmable gain stage, UART, serial peripheral interface, and a PWM output channel (Functional Block Diagram). It is fabricated using CMOS technology and offered in an 80-pin QFP, 84-pin PLCC, or 100-pin VQFP package.

The Z86C95 provides up to 16 output address lines thus permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits are provided via output address bits A15-A8.

There are 256 registers located on chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into sixteen groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. Also, the Z86C95 contains 512 bytes of DSP Program RAM and 128 words of DSP data RAM.

Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	V _{CC} GND	V _{DD} V _{SS}

OPERATING ERRATA

This notice only applies to devices top marked "Z86C9524 ASC/FSC/VSC" with a date code of 9237 or later.

1. A DSP load to the DAC Register fails below approximately V_{CC} = 4.7V.
2. Clipping occurs in the linearity of the DAC with a 100K load at about 3.3V output (VDHI = 3.5V).
3. I_{CC1} at HALT Mode will show a current of 17-18 mA, then will jump to 40-70 mA, and will settle between 17-24 mA. Settling time is about 10-15 seconds.
4. I_{CC2} at STOP Mode and DSP Pause will show a current of 1-2 mA, then will jump to 5-7 mA, and will settle at 3-4 mA. Settling time is about 10-15 seconds.

The following operating errata only applies to devices topmarked with "Z86C95 ASC/FSC/VSC."

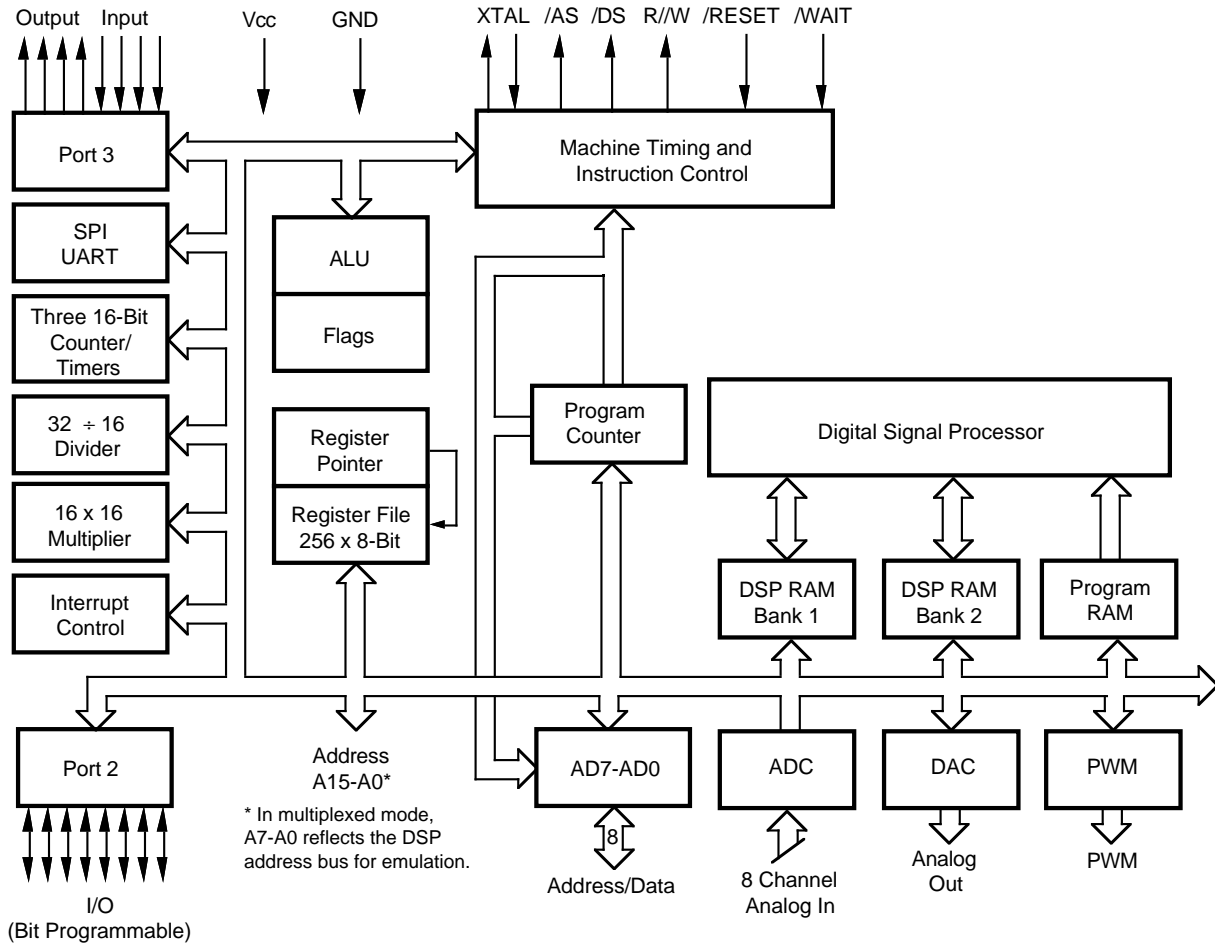
1. ICC1 at HALT Mode will show a current of 17-18 mA, then will jump to 40-70 mA, and will settle between 17-24 mA. Settling time is about 10-15 seconds.
2. ICC2 at STOP Mode and DSP Pause will show a current of 1-2 mA, then will jump to 5-7 mA, and will settle at 3-4 mA. Settling time is about 10-15 seconds.

The following operating errata only applies to devices topmarked with "Z86C9540 ASC/FSC/VSC or SL 1636."

1. ICC1 at HALT Mode will show a current of 17-18 mA, then will jump to 40-70 mA, and will settle between 17-24 mA. Settling time is about 10-15 seconds.

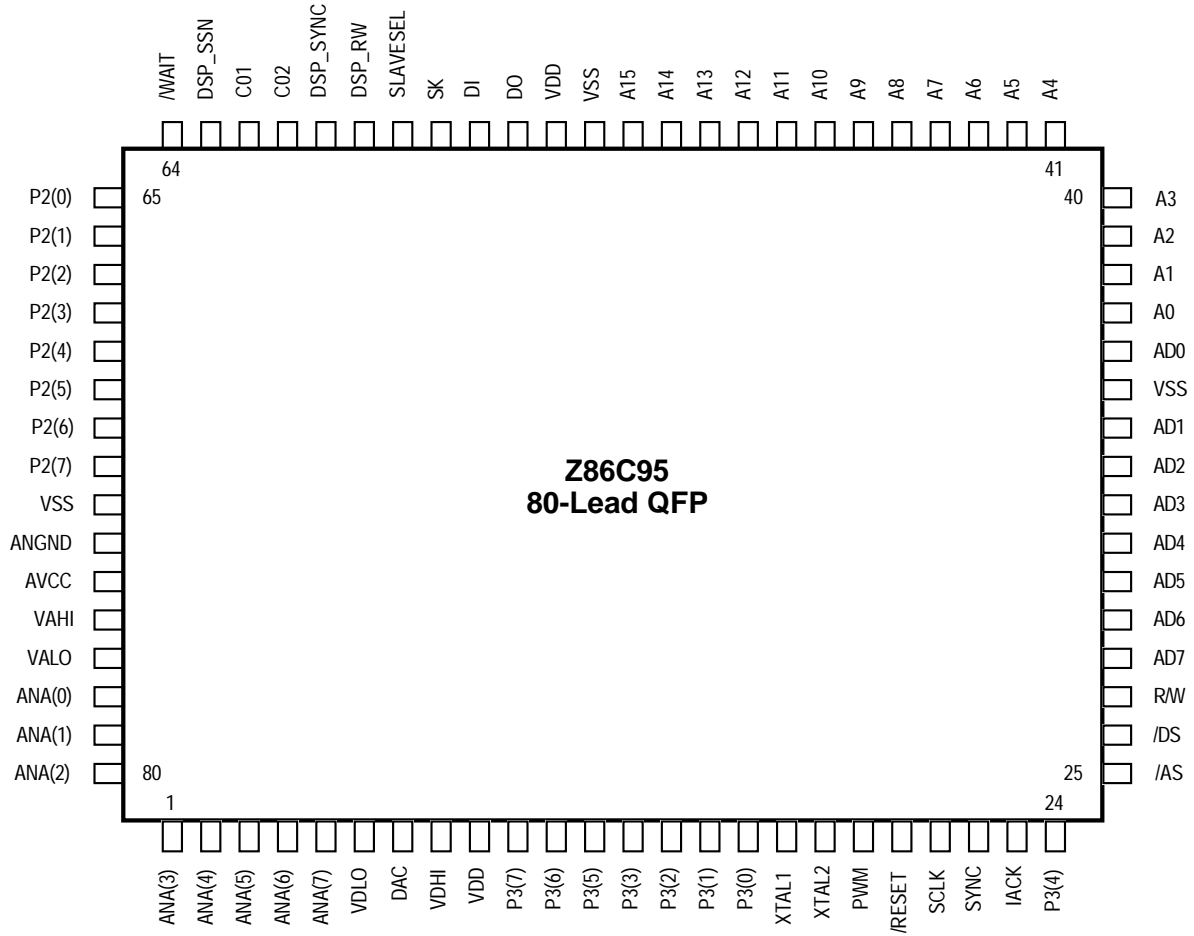
GENERAL DESCRIPTION (Continued)

- 2. ICC2 at STOP Mode and DSP Pause will show a current of 1-2 mA, then will jump to 5-7 mA, and will settle at 3-4 mA. Settling time is about 10-15 seconds.
- 3. The zero error for the ADC at 25°C is about 180 mV.



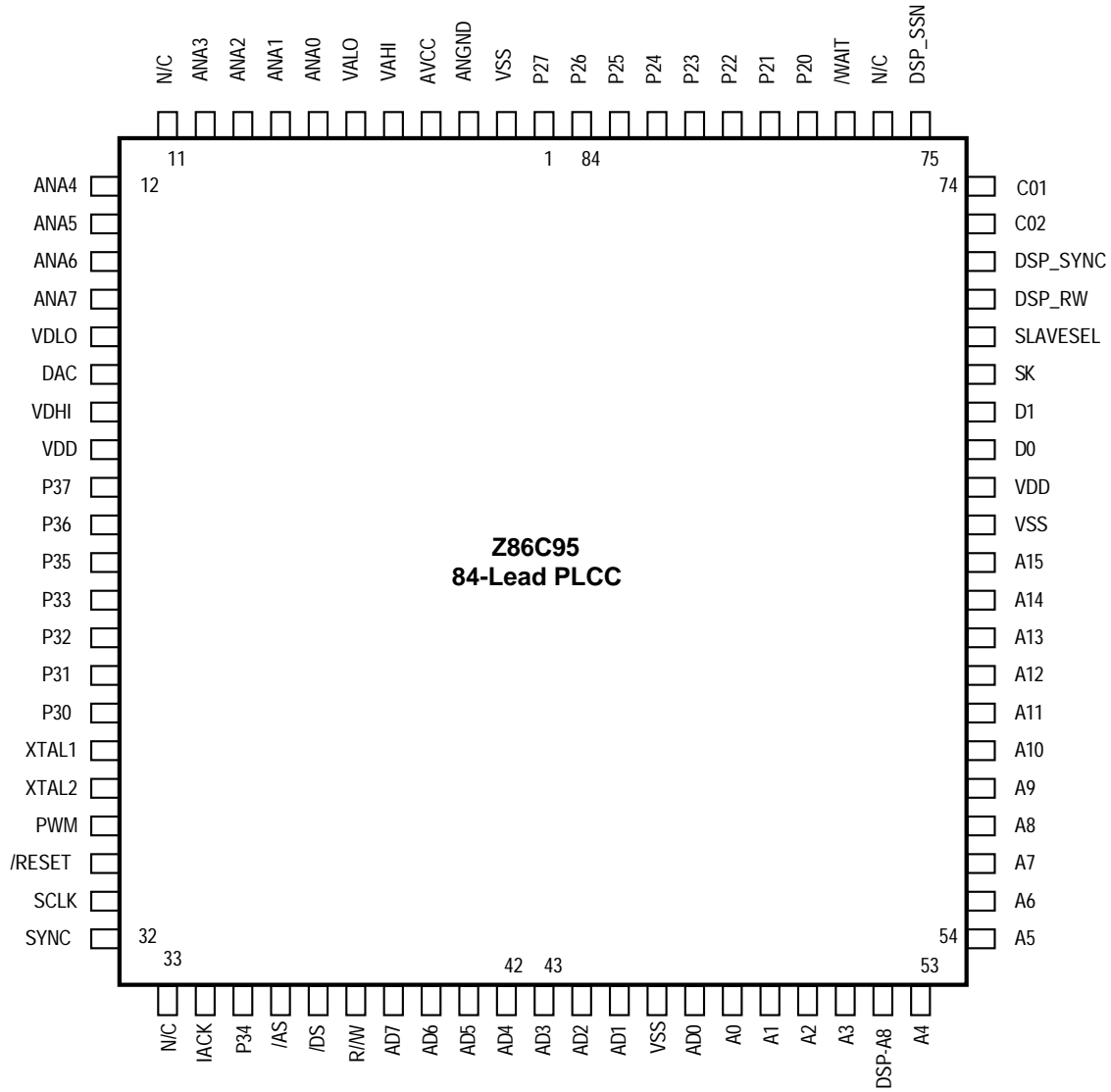
Functional Block Diagram

PIN DESCRIPTION



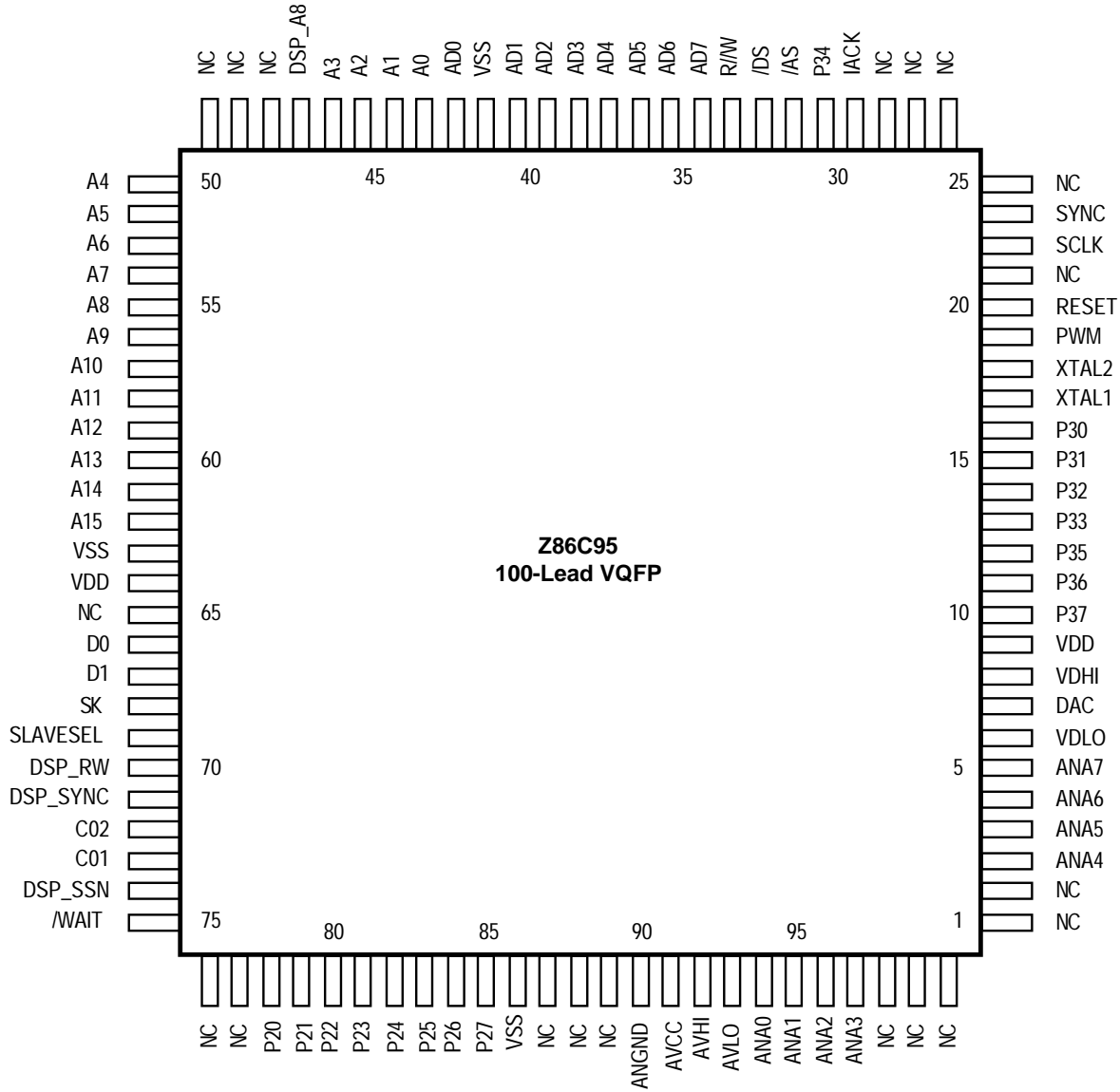
80-Lead QFP Pin Assignments

PIN DESCRIPTION (Continued)



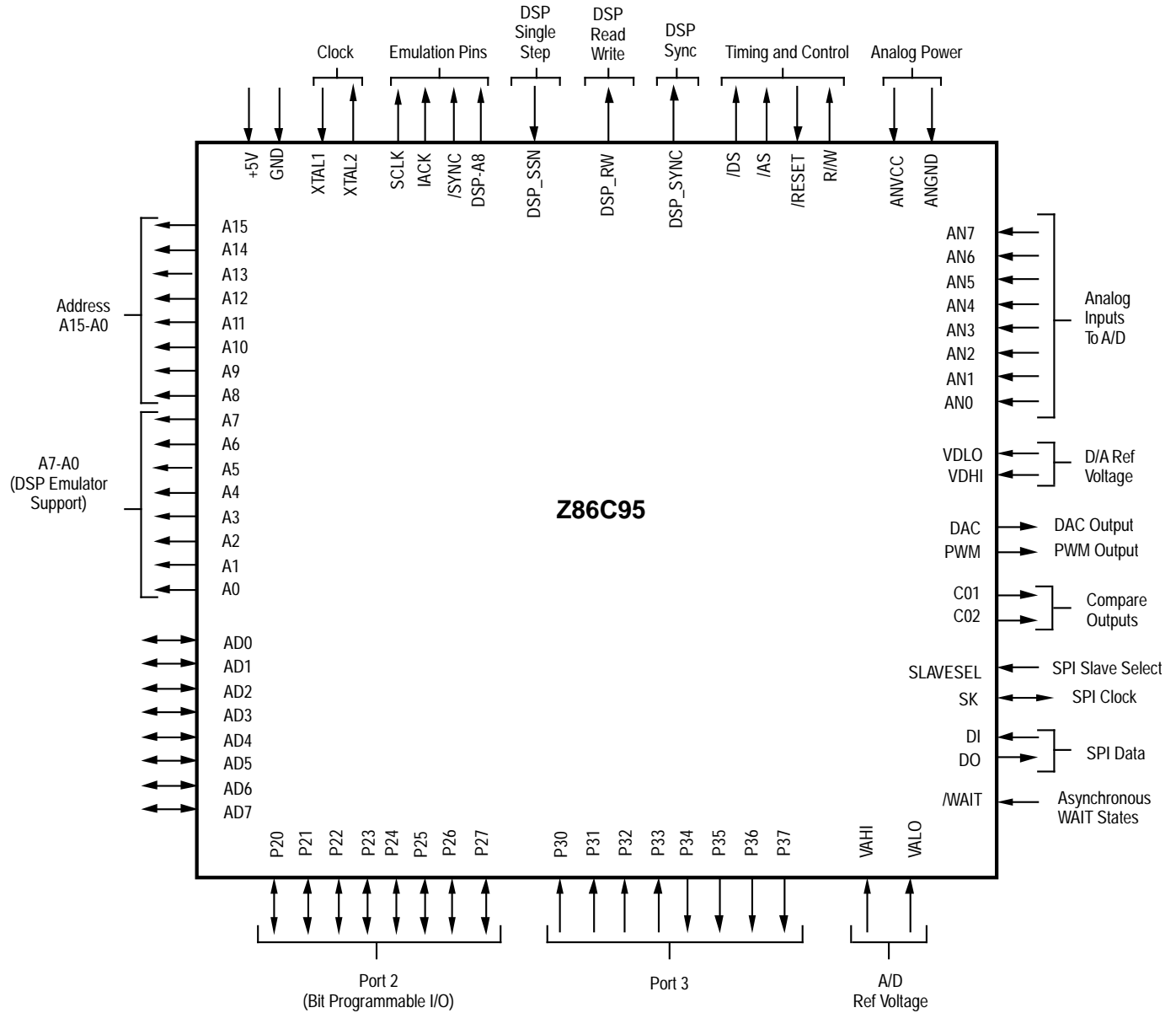
84-Lead PLCC Pin Assignments

PIN DESCRIPTION (Continued)



100-Pin VQFP Pin Assignments

PIN FUNCTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Unit
V_{DD}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp	†	†	C

Notes:

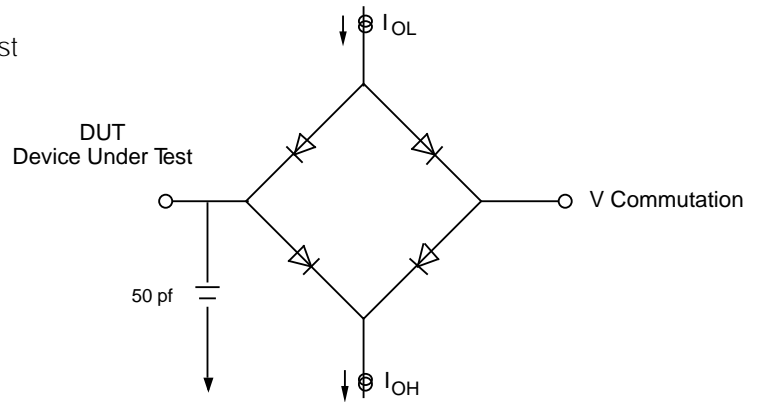
* Voltages on all pins with respect to GND.

† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted (Test Load Diagram).



Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

$$V_{CC} = 3.3V \pm 10\%$$

Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Typical at 25°C	Units	Conditions
		Min	Max			
	Max Input Voltage		7		V	$I_{IN} = 250 \mu\text{A}$
V_{CH}	Clock Input High Voltage	$0.8 V_{CC}$	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	$0.1xV_{CC}$		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	$0.6xV_{CC}$	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	$0.2xV_{CC}$		V	
V_{OH}	Output High Voltage	2.0			V	$I_{OH} = -1.0 \text{ mA}$
V_{OH}	Output High Voltage	$V_{CC} - 100 \text{ mV}$			V	$I_{OH} = -100 \mu\text{A}$
V_{OL}	Output Low Voltage		0.4		V	$I_{OL} = +1.0 \text{ mA}$
V_{RH}	Reset Input High Voltage	$0.8xV_{CC}$	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	$0.2xV_{CC}$		V	
I_{IL}	Input Leakage	-2	2		μA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		μA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-180		μA	$V_{RL} = 0V$
I_{CC}	Supply Current		50	40	mA	@ 24 MHz [1]
I_{CC1}	HALT		15	10	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 24 MHz [1]
I_{CC2}	STOP and Pause Mode		20	6	μA	STOP Mode $V_{IN} = 0V$, V_{CC} [1]
I_{ALL}	Auto Latch Low Current	-10	10	5	μA	

Note:

[1] All inputs driven to 0V, V_{CC} and outputs floating.

DC ELECTRICAL CHARACTERISTICS

$$V_{CC} = 5.0V \pm 10\%$$

Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Typical at 25°C	Units	Conditions
		Min	Max			
	Max Input Voltage		7		V	$I_{IN} = 250 \mu\text{A}$
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -2.0 \text{ mA}$
V_{OH}	Output High Voltage	$V_{CC} - 100\text{mV}$			V	$I_{OH} = -100 \mu\text{A}$
V_{OL}	Output Low Voltage		0.4		V	$I_{OH} = +2.0 \text{ mA}$
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	0.8		V	
I_{IL}	Input Leakage	-2	2		μA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		μA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-180		μA	$V_{RL} = 0V$
I_{CC}	Supply Current		82	50	mA	@ 24 MHz [1]
			120	70	mA	@ 33 MHz [1]
			150	85	mA	@ 40 MHz [1], [2]
I_{CC1}	HALT		20	13	mA	HALT Mode $V_{IN}=0V$, V_{CC} @ 24 MHz [1]
			30	20	mA	HALT Mode $V_{IN}=0V$, V_{CC} @ 33 MHz [1]
			45	30	mA	HALT Mode $V_{IN}=0V$, V_{CC} @ 40 MHz [1], [2]
I_{CC2}	STOP and Pause Mode		20	6	μA	STOP Mode $V_{IN}=0V$, V_{CC} [1]
I_{ALL}	Auto Latch Low Current	-20	20	5	μA	

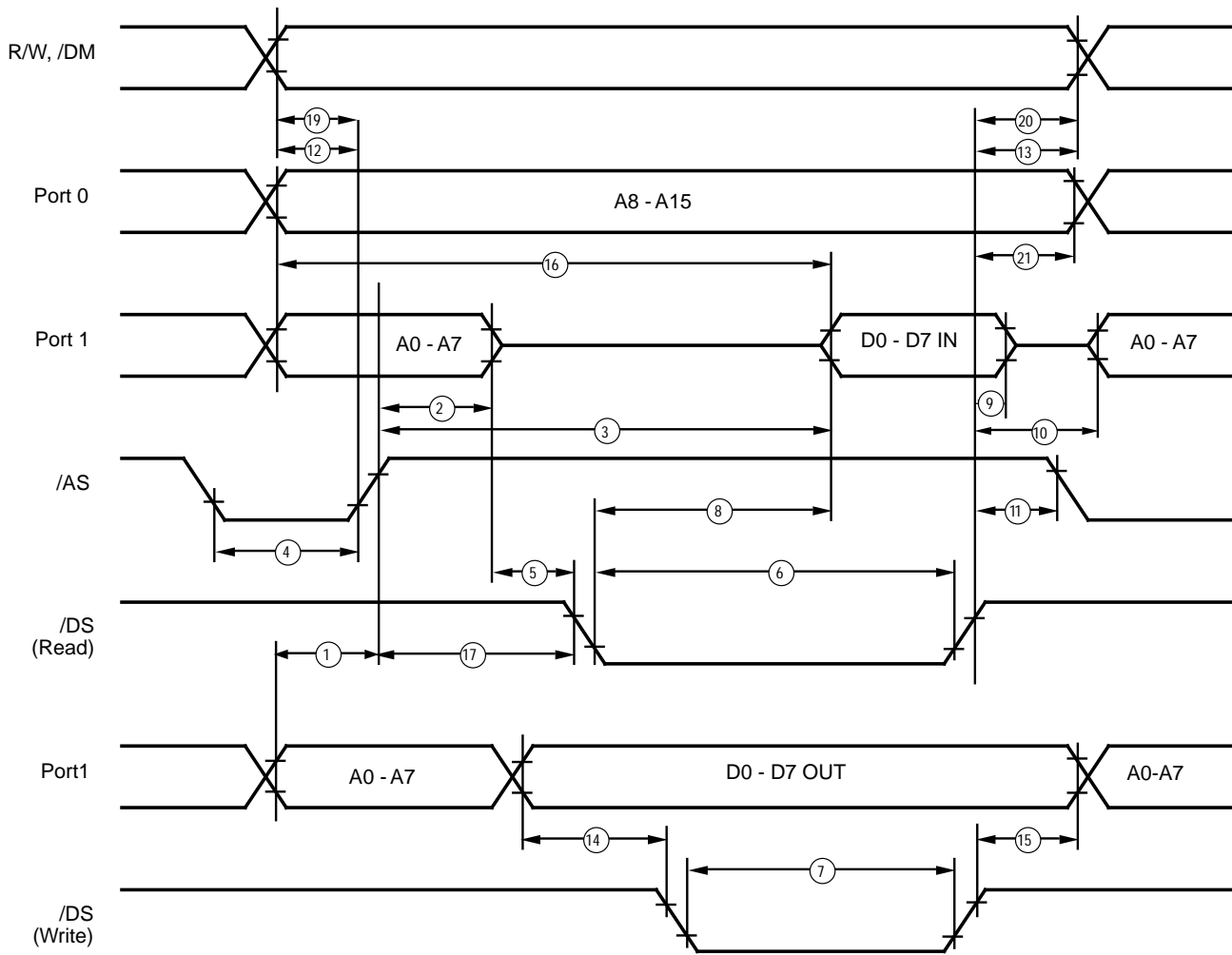
Note:

[1] All inputs driven to 0V, V_{CC} and outputs floating.

[2] Preliminary values, to be characterized.

AC CHARACTERISTICS

External I/O or Memory Read/Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

No	Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$						Units
			40 MHz**		33 MHz		24 MHz		
			Min	Max	Min	Max	Min	Max	
1	TdA(AS)	Address Valid To /AS Rise Delay	8		15		22		ns
2	TdAS(A)	/AS Rise To Address Hold Time	15		20		25		ns
3	TdAS(DI)	/AS Rise Data In Req'd Valid Delay		75		96		130	ns
4	TwAS	/AS Low Width	10		15		28		ns
5	TdAZ(DSR)	Address Float To /DS Fall (Read)	0		0		0		ns
6	TwDSR	/DS (Read) Low Width	60		65		100		ns
7	TwDSW	/DS (Write) Low Width	35		40		65		ns
8	TdDSR(DI)	/DS Fall (Read) To Data Req'd Valid Delay		40		45		80	ns
9	ThDSR(DI)	/DS Rise (Read) to Data In Hold Time	0		0		0		ns
10	TdDS(A)	/DS Rise To Address Active Delay	20		25		40		ns
11	TdDS(AS)	/DS Rise To /AS Delay	16		16		30		ns
12	TdR/W(AS)	R/W To Valid /AS Rise Delay	10		12		26		ns
13	TdDS(R/W)	/DS Rise To R/W Not Valid Delay	12		12		30		ns
14	TdDO(DSW)	Data Out To /DS Fall (Write) Delay	12		12		34		ns
15	ThDSW(DO)	/DS Rise (Write) To Data Out Hold Time	12		12		34		ns
16	TdA(DI)	Address Valid To Data Req'd Valid Delay		90		115		160	ns
17	TdAS(DSR)	/AS Rise To /DS Fall (Read) Delay	20		20		40		ns
19	TdDM(AS)	/DM Valid To /AS Rise Delay	10		10		22		ns
20	TdDS(DM)	/DS Rise To /DM Valid Delay	15		15		35		ns
21	ThDS(A)	/DS Rise To Address Valid Hold Time	15		15		30		ns
22	TdXT(SCR)	XTAL Falling to SCLK Rising		30		35		40	ns
23	TdXT(SCF)	XTAL Falling to SCLK Falling		30		35		40	ns
24	TdXT(DSRF)	XTAL Falling to /DS Read Falling		40		45		50	ns
25	TdXT(DSRR)	XTAL Falling to /DS Read Rising		30		35		45	ns
26	TdXT(DSWF)	XTAL Falling to /DS Write Falling		40		45		50	ns
27	TdXT(DSWF)	XTAL Falling to /DS Write Rising		30		35		45	ns
28	TsW(XT)	Wait Set-up Time	5		5		5		ns
29	ThW(XT)	Wait Hold Time	15		15		15		ns
30	TwW	Wait Width (One Wait Time)	20		20		25		ns

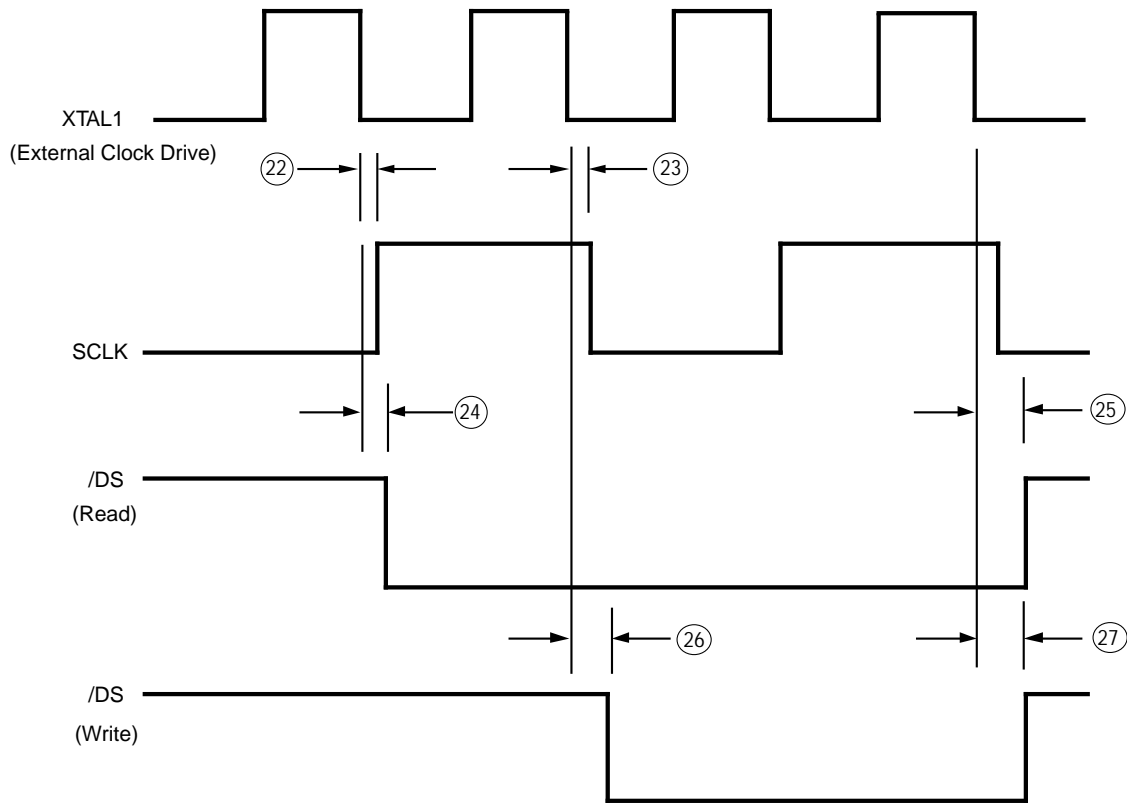
Notes:

When using extended memory timing add 2 TpC.

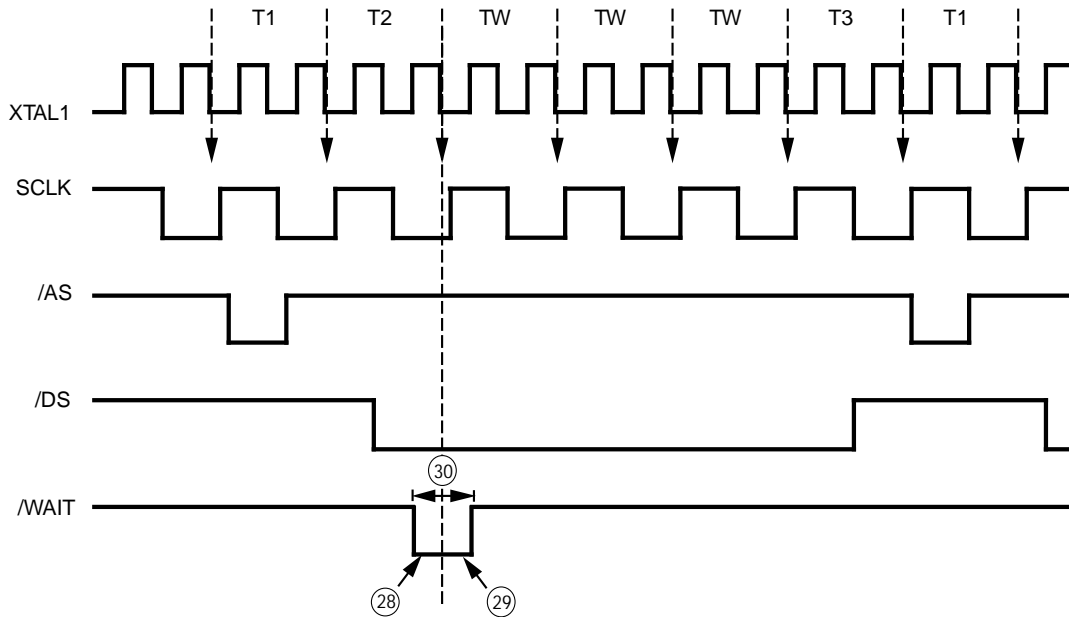
Timing numbers given are for minimum TpC.

** Preliminary values, to be characterized.

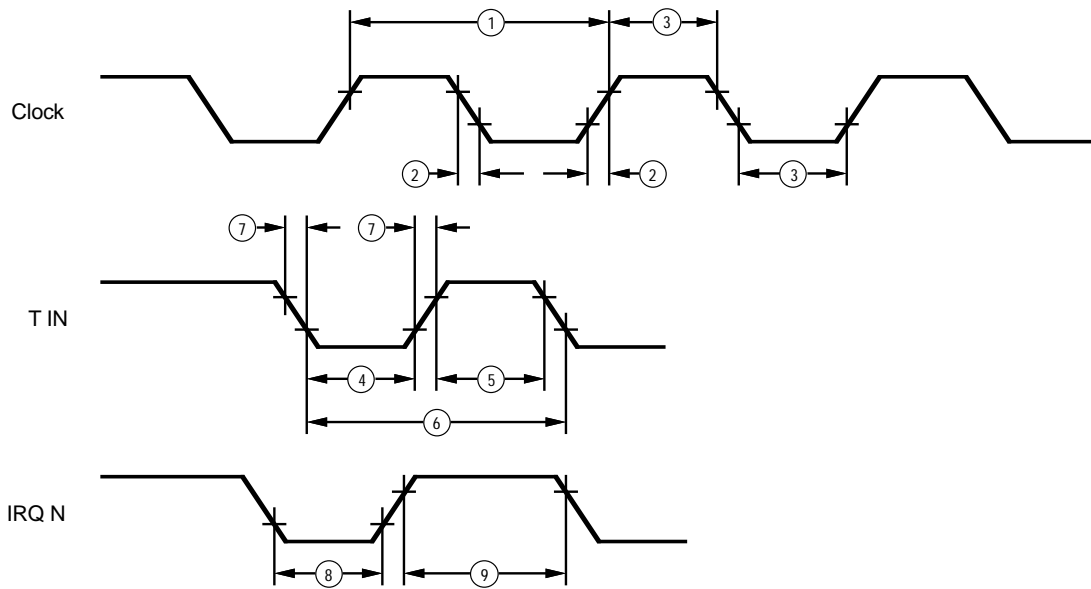
AC CHARACTERISTICS (Continued)
Timing Diagrams



XTAL/SCLK To DSR and DSW Timing



XTAL/SCLK To WAIT Timing



Additional Timing

AC CHARACTERISTICS

Additional Timing Table

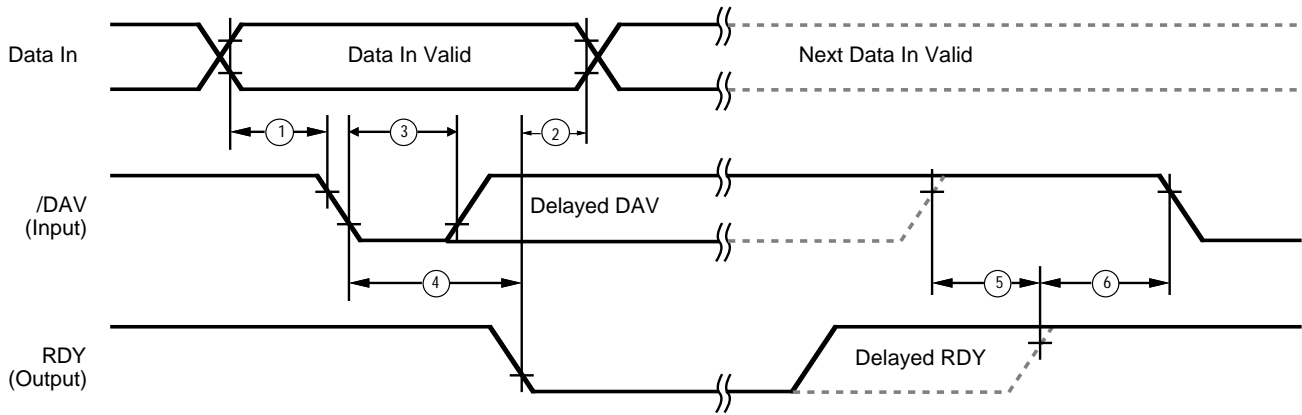
No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$						Units	Notes
			40 MHz		24 MHz		33 MHz			
			Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	25	1000	42	1000	30	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		5		10		5	ns	[1]
3	TwC	Input Clock Width	8		11		10		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3 TpC		3 TpC		3 TpC			[2]
6	TpTin	Timer Input Period	8 TpC		8 TpC		8 TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times		100		100		100	ns	[2]
8a	TwIL	Interrupt Request Input Low Times	70		70		70		ns	[2,4]
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		5 TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3 TpC		3 TpC		3 TpC			[2,3]

Notes:

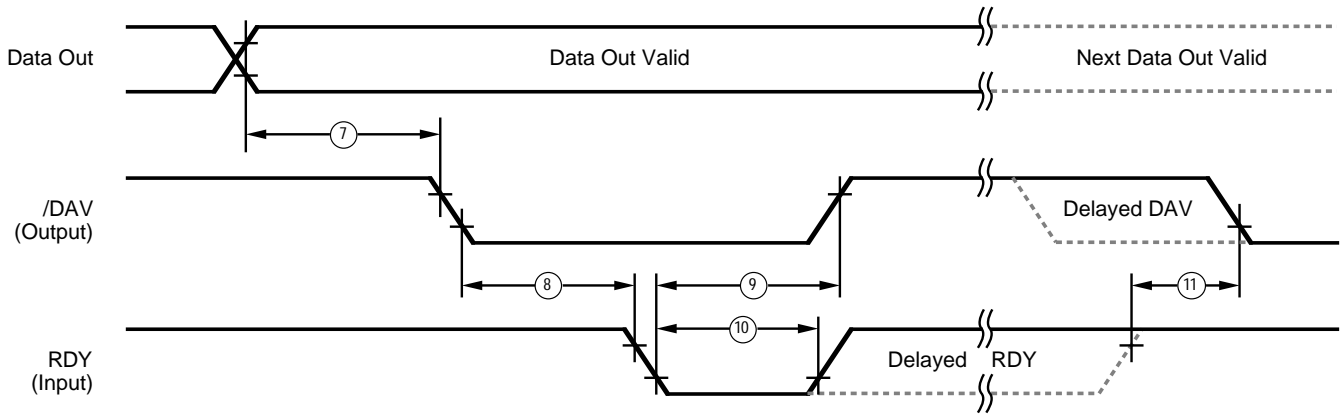
- [1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request via Port 3.
- [4] Interrupt request via Port 3 (P33-P31).
- [5] Interrupt request via Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Units	Data Direction
			Min	Max		
1	TsDI(DAV)	Data In Setup Time to /DAV	0		ns	In
2	ThDI(DAV)	RDY to Data In Hold Time	0		ns	In
3	TwDAV	/DAV Width	40		ns	In
4	TdDAVIf(RDYf)	/DAV to RDY Delay		70	ns	In
5	TdDAVr(RDYr)	DAV Rise to RDY Wait Time		40	ns	In
6	TdRDYOr(DAVIf)	RDY Rise to DAV Delay	0		ns	In
7	TdDO(DAV)	Data Out to DAV Delay	TpC		ns	Out
8	TdDAVOf(RDYIf)	/DAV to RDY Delay	0		ns	Out
9	TdRDYIf(DAVOr)	RDY to /DAV Rise Delay		70	ns	Out
10	TwRDY	RDY Width	40		ns	Out
11	TdRDYIr(DAVOf)	RDY Rise to DAV Wait Time		40	ns	Out

AC CHARACTERISTICS (Continued)
A/D Converter Electrical Characteristics

$$V_{CC} = 3.3V \pm 10\%$$

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	2.7	3.0	3.3	Volts
Power dissipation, no load		20	40	mW
Clock frequency			24	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			2	μ sec
Input capacitance on ANA	25		40	pF
VA_{HI} range	$VA_{LO} + 2.5$		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		$AV_{CC} - 2.5$	Volts
$VA_{HI} - VA_{LO}$	2.5		AV_{CC}	Volts

Notes:

Voltage 2.7V – 3.3V

Temp 0-70°C

D/A Converter Electrical Characteristics

$$V_{CC} = 3.3V \pm 10\%$$

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0	μ sec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		0.25	0.5	LSB
Supply Range	2.7	3.0	3.3	Volts
Power dissipation, no load		10		mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		μ Vp-p
VD_{HI} range at 3 volts	1.5	1.8	2.1	Volts
VD_{LO} range at 3 volts	0.2	0.5	0.8	Volts
$VD_{HI} - VD_{LO}$, at 3 volts	1.3	1.6	1.9	Volts
Capacitive output load, CL			20	pF
Resistive output load, RL	50K			Ohms
Output slew rate	1.0	3.0		V/ μ sec

Notes:

Voltage 2.7V – 3.3V

Temp 0-70°C

A/D Converter Electrical Characteristics

$V_{CC} = 5.0V \pm 10\%$

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			33	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			2	μ sec
Input capacitance on ANA	25		40	pF
VA_{HI} range	$VA_{LO} + 2.5$		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		$AV_{CC} - 2.5$	Volts
$VA_{HI} - VA_{LO}$	2.5		AV_{CC}	Volts

Notes:

Voltage 4.5V -5.5V

Temp 0-70°C

D/A Converter Electrical Characteristics

$V_{CC} = 5.0V \pm 10\%$

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0	μ sec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		1	2	% FSR
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		μ Vp-p
VD_{HI} range at 3 volts	2.6		3.5	Volts
VD_{LO} range at 5V volts	0.8		1.7	Volts
$VD_{HI} - VD_{LO}$, at 5V volts	0.9		2.7	Volts
Capacitive output load, CL			30	pF
Resistive output load, RL	20K*			Ohms
Output slew rate	1.0	3.0		V/ μ sec

Notes:

Voltage 4.5V - 5.5V

Temp 0-70°C

* 100K for 24 MHz device.

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