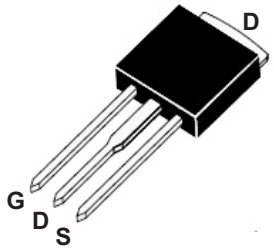
N-Channel Power MOSFET
(50A, 60Volts)

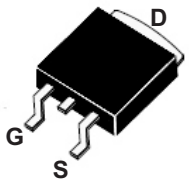
DESCRIPTION

The Nell **50N06** is a three-terminal silicon device with current conduction capability of 50A, fast switching speed, low on-state resistance, breakdown voltage rating of 60V, and max. threshold voltage of 4 volts.

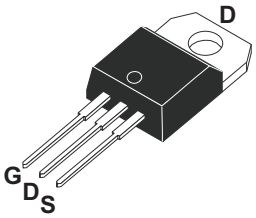
They are designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.



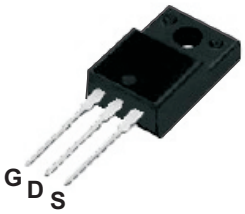
TO-251
(50N06F)



TO-252
(50N06G)



TO-220AB
(50N06A)

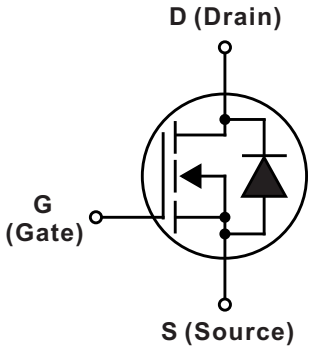


ITO-220AB (TO-220F)
(50N06AF)

FEATURES

- $R_{DS(ON)}$ = 22mΩ@V_{GS} = 10V
- Ultra low gate charge(40nC max.)
- Low reverse transfer capacitance (C_{RSS} = 80pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 175°C operation temperature

PRODUCT SUMMARY	
I_D (A)	50
V_{DSS} (V)	60
$R_{DS(ON)}$ (Ω)	0.022 @ V_{GS} = 10V
Q_G(nC) max.	40

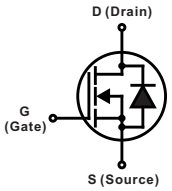


ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)					
SYMBOL	PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltag		T_J=25°C to 150°C	60	V
V_{DGR}	Drain to Gate voltage		R_{GS}=20KΩ	60	
V_{GS}	Gate to Source voltage			±20	
I_D	Continous Drain Current		T_C=25°C	50	A
			T_C=100°C	35	
I_{DM}	Pulsed Drain current(Note 1)			200	
E_{AS}	Single pulses avalanche energy(Note 2)			480	mJ
E_{AR}	Repetitive avalanche energy(Note 1)			13	
dv/dt	Peak diode recovery dv/dt(Note 3)			7	V /ns
P_D	Total power dissipation, T_C=25°C	TO-251		130	W
		TO-252		130	
		TO-220		120	
		TO-220F		70	
T_J	Operation junction temperature			-55 to 175	°C
T_{STG}	Storage temperature			-55 to 175	
T_L	Maximum soldering temperature, for 10 seconds		1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw			10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.L = 5.6mH, I_{AS} = 50A, V_{DD} = 25V, R_G = 0Ω, starting T_J=25°C.
3.I_{SD} ≤ 50A, di/dt ≤ 300A/us, V_{DD} ≤ $V_{(BR)DSS}$, starting T_J=25°C.

THERMAL RESISTANCE						
SYMBOL	PARAMETER		Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-251/TO-252			1.15	°C/W
		TO-220			1.24	
		TO-220F			1.78	
$R_{th(c-s)}$	Thermal resistance, case to heatsink			0.5		
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-251/TO-252			100	
		TO-220/TO-220F			62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{(BR)DSS}$	Drain to source breakdown voltage	I_D = 250μA, V_{GS} = 0V	60			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	I_D = 250μA, referenced to 25°C		0.07		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=60V, V_{GS}=0V, T_C = 25°C			1.0	μA
		V_{DS}=60V, V_{GS}=0V, T_C=150°C			50	
I_{GSS}	Gate to source forward leakage current	V_{GS} = 20V, V_{DS} = 0V			100	nA
	Gate to source reverse leakage current	V_{GS} = -20V, V_{DS} = 0V			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	I_D = 50A, V_{GS} = 10V		18	22	mΩ
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS}, I_D=250μA	2.0		4.0	V
C_{ISS}	Input capacitance	V_{DS} = 25V, V_{GS} = 0V, f =1MHz		900	1220	pF
C_{OSS}	Output capacitance			430	550	
C_{RSS}	Reverse transfer capacitance			80	100	
$t_{d(ON)}$	Turn-on delay time	V_{DD} = 30V, I_D = 25A, R_G=50Ω (Note 1, 2)		40	60	ns
t_r	Rise time			100	200	
$t_{d(OFF)}$	Turn-off delay time			90	180	
t_f	Fall time			80	160	
Q_G	Total gate charge	V_{DS} = 48V, V_{GS} = 10V, I_D = 50A (Note 1, 2)		30	40	nC
Q_{GS}	Gate to source charge			9.6		
Q_{GD}	Gate to drain charge (Miller charge)			10		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 50A, V_{GS} = 0V			1.5	V
I_S	Continous source current	Integral reverse P-N junction diode in the MOSFET			50	A
I_{SM}	Pulsed source current				200	
t_{rr}	Reverse recovery time	I_S = 50A, V_{GS} = 0V, dI_F/dt = 100A/μs		55		ns
Q_{rr}	Reverse recovery charge			80		nC

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

50 N 06 A

Current rating, I_D
50 = 50A

MOSFET series
N = N-Channel

Voltage rating, V_{DS}
06 = 60V

Package type
A = TO-220AB
AF = TO-220F
F = TO-251 (I-PAK)
G = TO-252(D-PAK)

■ TEST CIRCUITS AND WAVEFORMS

Fig.1A Peak diode recovery dv/dt test circuit

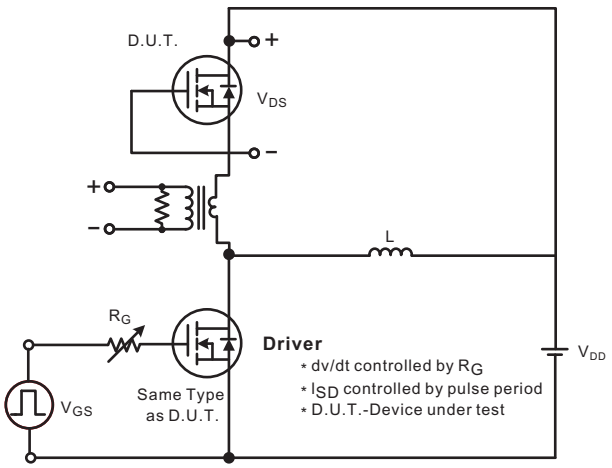
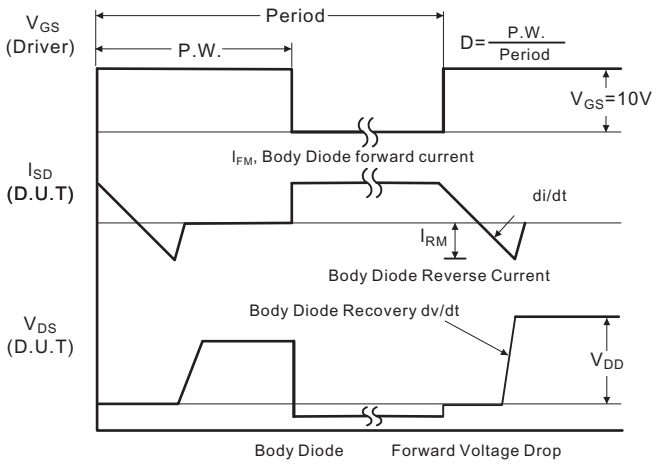


Fig.1B Peak diode recovery dv/dt waveforms



■ TEST CIRCUITS AND WAVEFORMS (Cont.)

Fig.2A Switching test circuit

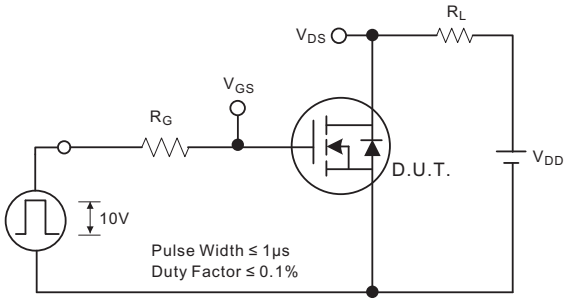


Fig.2B Switching Waveforms

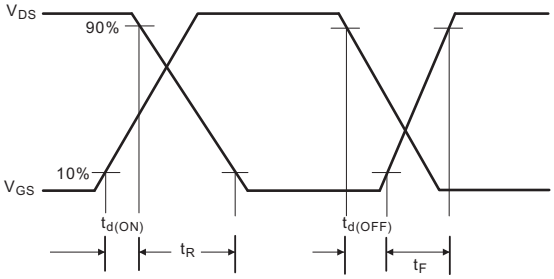


Fig.3A Gate charge test circuit

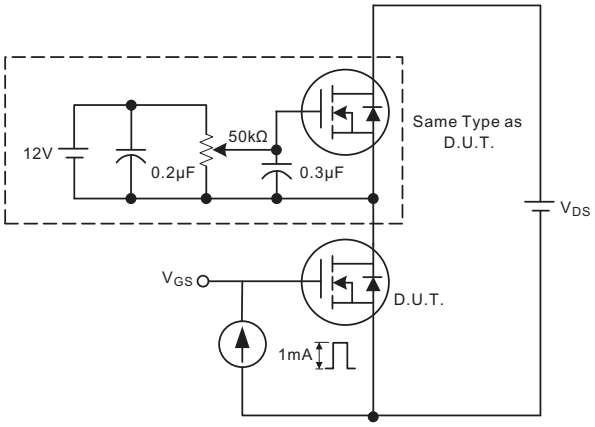


Fig.3B Gate charge waveform

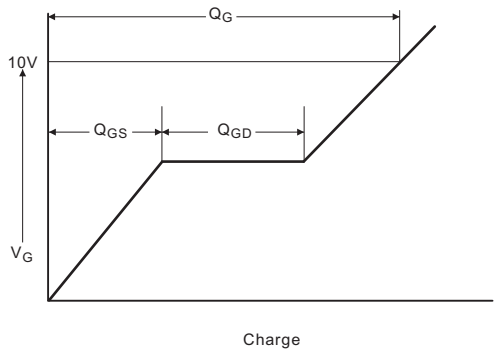


Fig.4A Unclamped Inductive switching test circuit

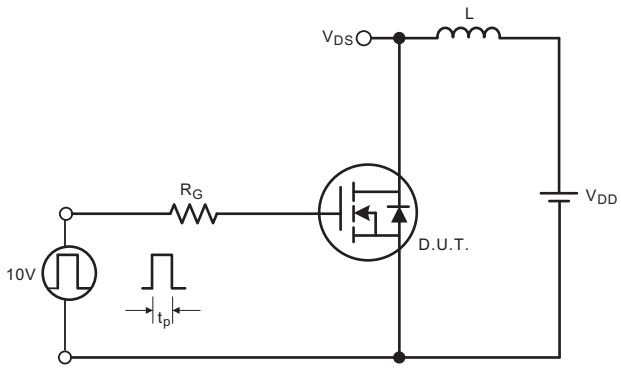
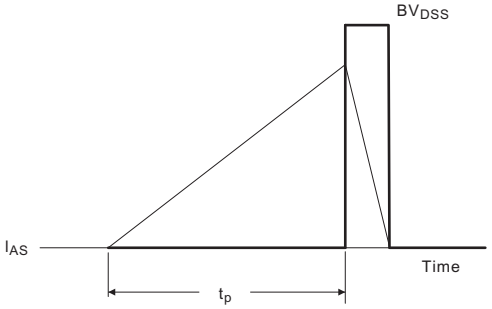


Fig.4B Unclamped Inductive switching waveforms



■ TYPICAL CHARACTERISTICS

Fig.1 On-State characteristics

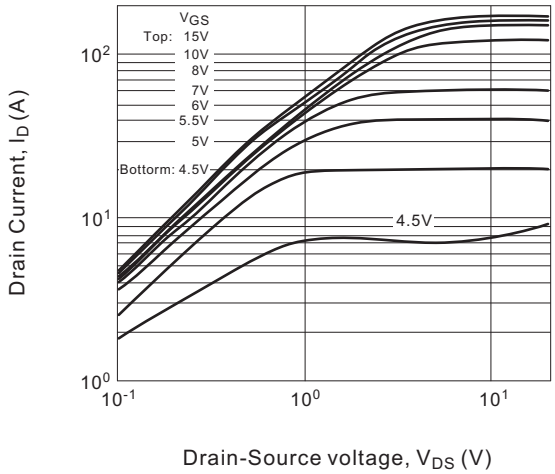


Fig.2 Transfer characteristics

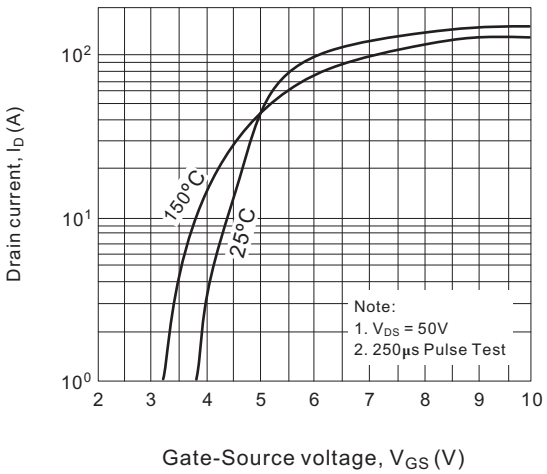


Fig.3 On-Resistance variation vs drain current and gate voltage

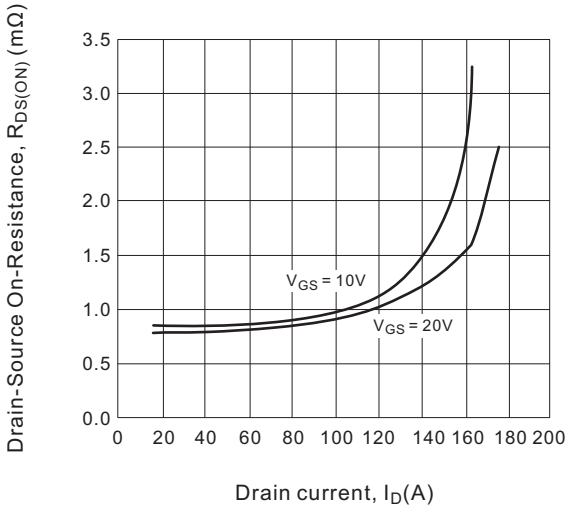


Fig.4 On state current vs. allowable case temperature

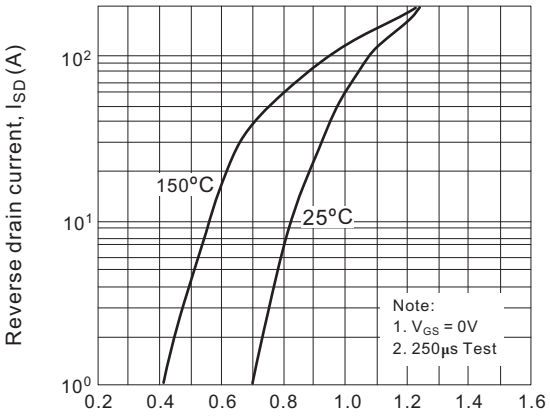


Fig.5 Capacitance characteristics (Non-Repetitive)

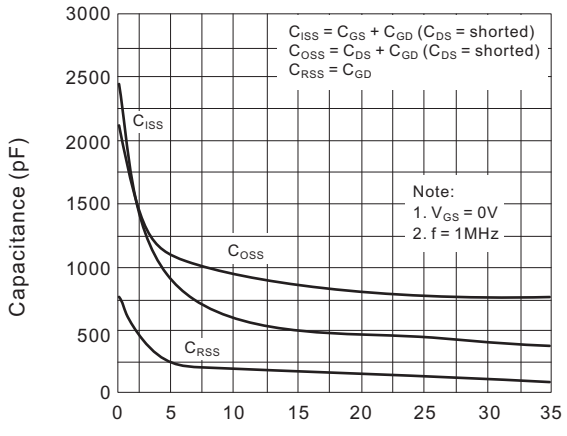


Fig.6 Gate charge characteristics

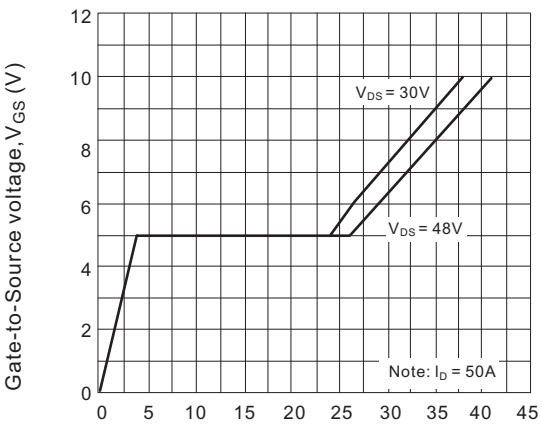


Fig.7 Breakdown voltage variation vs junction temperature

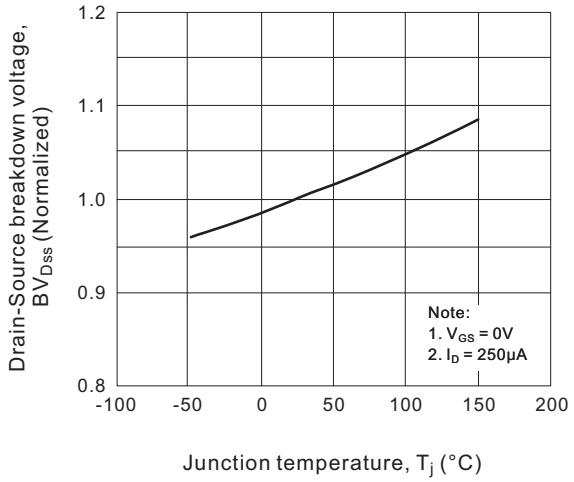


Fig.8 On-Resistance variation vs junction temperature

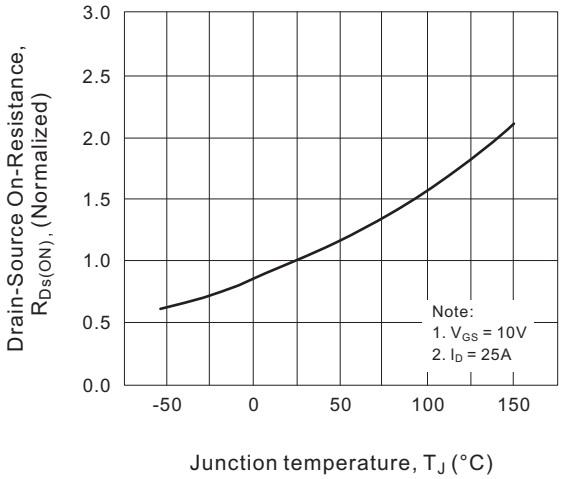


Fig.9 Maximum safe operating

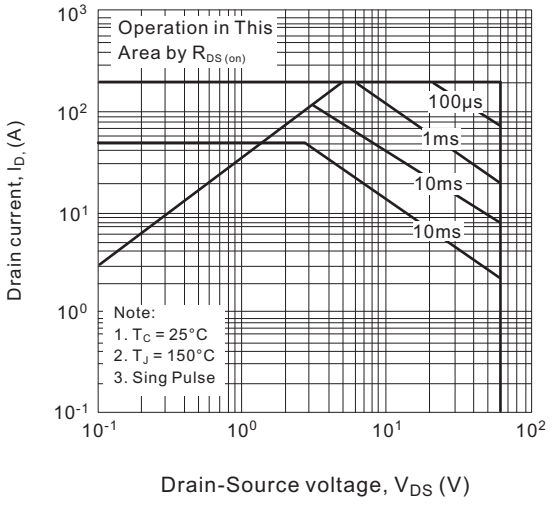


Fig.10 Maximum drain current vs. case temperature

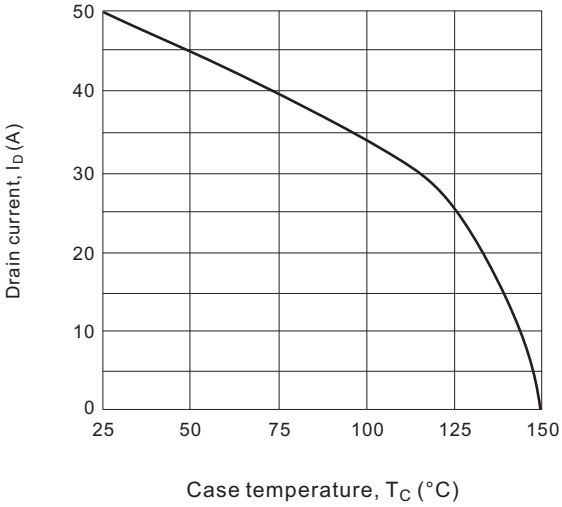
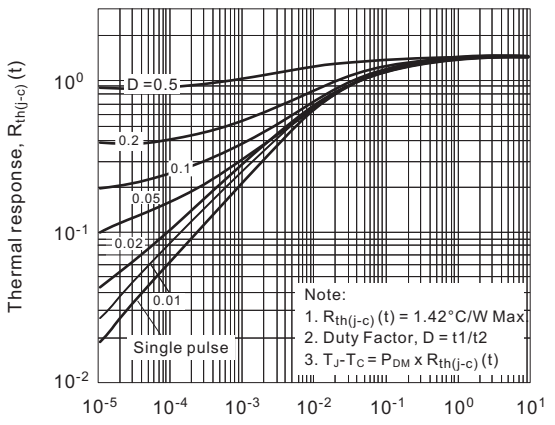
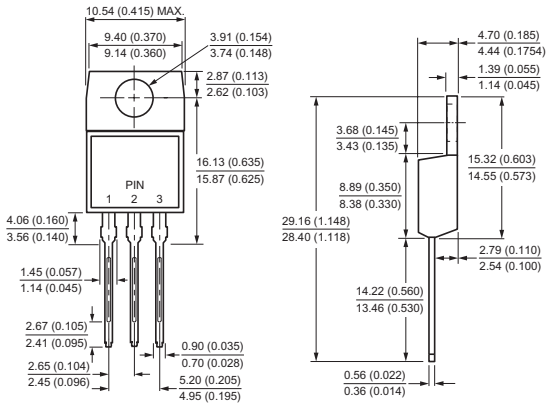


Fig.11 Transient thermal response curve

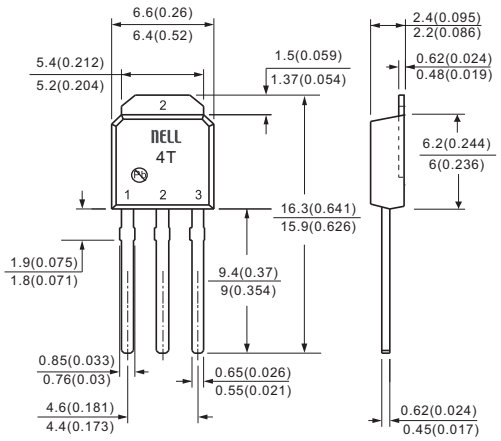


Case Style

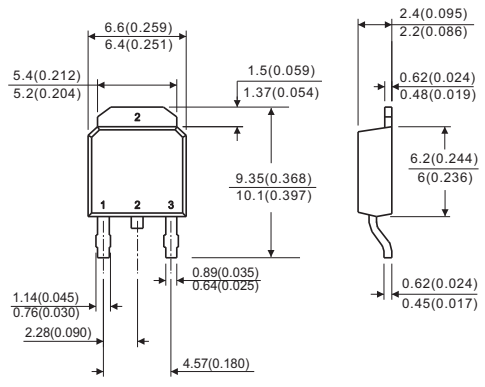
TO-220AB

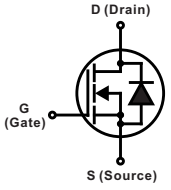


TO-251 (I-PAK)



TO-252 (D-PAK)

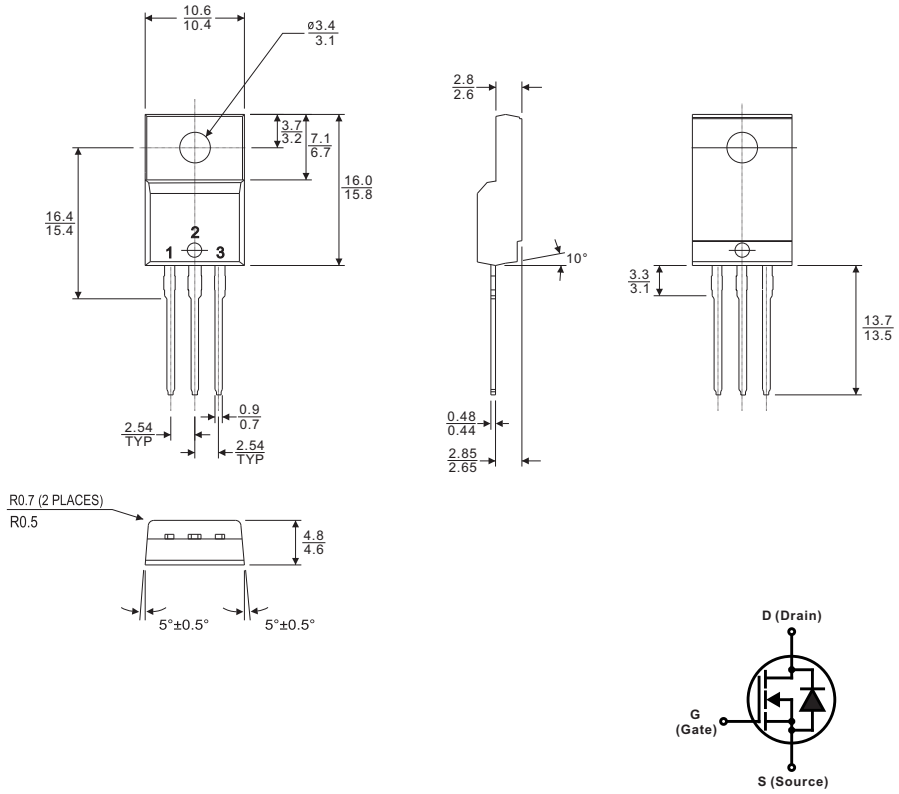




All dimensions in millimeters(inches)

Case Style

ITO-220AB



All dimensions in millimeters