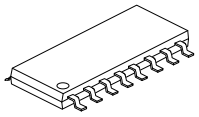
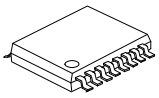
UCD4050B

Preliminary ***CMOS IC***

CMOS HEX BUFFER/CONVERTERS



SOP-16



TSSOP-16

■ DESCRIPTION

The **UCD4050B** devices are non-inverting hex buffers, and feature logic-level conversion using only one supply voltage(V_{CC}).The input-signal high level(V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads.

■ FEATURES

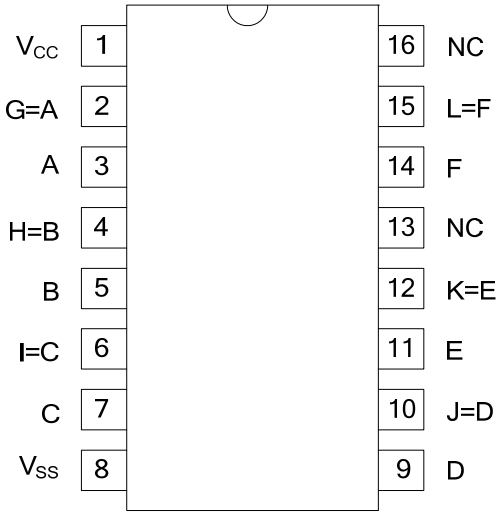
* **UCD4050B** non inverling
* High Sink Current for Driving 2 TTL Loads
* High-To-Low Level Logic Conversion
* Maximum Input Current of 1uA at 18V Over Full Package Temperature Range
* 5V, 10V and 15V Parametric Ratings

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4050BL-S16-R	UCD4050BG-S16-R	SOP-16	Tape Reel
UCD4050BL-S16-T	UCD4050BG-S16-T	SOP-16	Tube
UCD4050BL-P16-R	UCD4050BG-P16-R	TSSOP-16	Tape Reel
UCD4050BL-P16-T	UCD4050BG-P16-T	TSSOP-16	Tube

UCD4050BL-S16-R (1)Packing Type (2)Package Type (3)Lead Free	(1) T: Tube, R: Tape Reel (2) S16: SOP-16, TSSOP-16 (3) L: Lead Free, G: Halogen Free

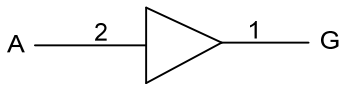
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(G)
H	H
L	L

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING(T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 20	V
Input Voltage	V_{IN}	-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	-0.5~V_{DD}+0.5	V
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		5		15	V
Operating Temprature	T_{OPR}		-40		125	°C

■ ELECTRICAL CHARACTERISTICS(T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=5V, V_{OUT}=4.5V	3.5			V
		V_{CC}=10V, V_{OUT}=9.0V	7.0			
		V_{CC}=15V, V_{OUT}=13.5V	11.0			
Low-Level Input Voltage	V_{IL}	V_{CC}=5V, V_{OUT}=0.5V			1.5	V
		V_{CC}=10V, V_{OUT}=1.0V			3.0	
		V_{CC}=15V, V_{OUT}=1.5V			4.0	
High-Level Output Voltage	V_{OH}	V_{CC}=5V, No Load	4.95	5		V
		V_{CC}=10V, No Load	9.95	10		
		V_{CC}=15V, No Load	14.95	15		
Low-Level Output Voltage	V_{OL}	V_{CC}=5V, No Load		0	0.05	V
		V_{CC}=10V, No Load		0	0.05	
		V_{CC}=15V, No Load		0	0.05	
High-Level Output Current (Note)	I_{OH}	V_{CC}=5V, V_{OUT}=4.6V	-0.65	-1.2		mA
		V_{CC}=5V, V_{OUT}=2.5V	-2.1	-3.9		
		V_{CC}=10V, V_{OUT}=9.5V	-1.65	-3.0		
		V_{CC}=15V, V_{OUT}=13.5V	-4.3	-8.0		
Low-Level Output Current (Note)	I_{OL}	V_{CC}=5V, V_{OUT}=0.4V	3.2	6.4		
		V_{CC}=10V, V_{OUT}=0.5V	8.0	16.0		
		V_{CC}=15V, V_{OUT}=1.5V	24.0	48.0		
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=15V ,V_{IN}=V_{CC}or GND			±0.1	μA
Quiescent Supply Current	I_Q	V_{CC}=5V, V_{IN}=V_{CC}orV_{SS}, I_{OUT}=0		0.02	1	μA
		V_{CC}=10V, V_{IN}=V_{CC}orV_{SS}, I_{OUT}=0		0.02	2	
		V_{CC}=15V, V_{IN}=V_{CC}orV_{SS}, I_{OUT}=0		0.02	4	
		V_{CC}=20V, V_{IN}=V_{CC}orV_{SS}, I_{OUT}=0		0.02	20	

Note: I_{OL} and I_{OH} are tested one output at a time

■ SWITCHING CHARACTERISTICS(T_A=25°C, Input: t_R=t_F=20ns, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	t_{PLH}	VDD=5V, C_L=50pF, R_L=200kΩ		70	140	ns
		VDD=10V, C_L=50pF, R_L=200kΩ		40	80	
		VDD=15V, C_L=50pF, R_L=200kΩ		30	60	
	t_{PHL}	VDD=5V, C_L=50pF, R_L=200kΩ		55	110	
		VDD=10V, C_L=50pF, R_L=200kΩ		22	55	
		VDD=15V, C_L=50pF, R_L=200kΩ		15	30	
Transition Time	t_{TLH}	VDD=5V, C_L=50pF, R_L=200kΩ		80	160	ns
		VDD=10V, C_L=50pF, R_L=200kΩ		40	80	
		VDD=15V, C_L=50pF, R_L=200kΩ		30	60	
	t_{THL}	VDD=5V, C_L=50pF, R_L=200kΩ		30	60	
		VDD=10V, C_L=50pF, R_L=200kΩ		20	40	
		VDD=15V, C_L=50pF, R_L=200kΩ		15	30	

■ OPERATING CHARACTERISTICS(T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		5	7.5	pF

■ TEST CIRCUIT AND WAVEFORMS

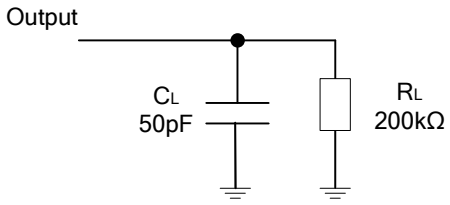


Fig 1. Definitions for test circuit

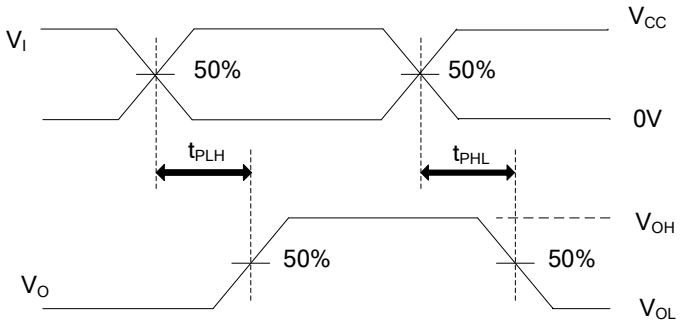


Fig 2. Propagation Delay Times

Note: C_L includes probe and jig capacitance.