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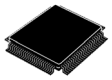
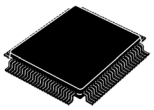
MPC560xS

MPC560xS Microcontroller Data Sheet



LQFP 144
20 x 20 x 1.4 mm



LQFP 176
24 x 24 x 1.4 mm

- High performance 64 MHz e200z0h CPU
  - 32-bit Power Architecture™ book E CPU
  - Up to 60 DMIPs operation
  - Variable length encoding (VLE)
- Memory available
  - Up to 1 MB on-chip Flash, with ECC
  - Up to 48 KB on-chip RAM with ECC
  - 160 KB on-chip graphic RAM
  - External flash extension via Quad-SPI
  - 12-entry memory protection unit
- Dashboard peripheral set
  - 6 stepper motor drivers with stall detection and zero positioning
  - 4 × 40 or 6 × 38 LCD display driver
  - Sound control
  - Real-time clock
- TFT display control unit
  - 4 × plane and cursor graphic controller
  - Display capable of driving up to WVGA
  - 24-bit RGB
  - Parallel Data Interface
- Interrupts and DMA
  - Up to 128 selectable interrupts
  - 16 priority levels
  - Non-maskable interrupt (NMI)
  - Up to 32 external interrupts with 18 wakeup lines
  - 16-channel eDMA controller
- Up to 133 GPIOs in LQFP176
- Timer units
  - 4-channel 32-bit periodic interrupt timers
  - 4-channel 32-bit system timer module
  - System watchdog timer
- Timed I/O
  - 8-channel 16-bit counter IC/OC
  - 16-channel 16-bit counter IC/OC/PWM
  - Communications interface
  - 2 FlexCAN interfaces (2.0B active)
  - Up to 3 LINFlex/UART channels
  - Up to 3 DSPI channels, with one Quad-SPI
  - Up to 4 I^2C interfaces
- 16/23-channel, 10-bit ADC converter
- On-chip CAN/UART bootstrap loader
- Clock generation
  - 4–16 MHz fast external crystal oscillator
  - 32 kHz slow external crystal oscillator
  - 16 MHz fast internal RC oscillator
  - 128 kHz slow internal RC oscillator for low power modes
  - Up to 2 software-controlled internal FMPLL modulated or not
- Exhaustive debugging capability
  - Nexus L1 on all devices
  - Nexus L2+ on LBGA208 package
  - Nexus L2+ on LQFP176 package as alternate function
- Voltage supply
  - Single 5 V or 3.3 V supply for I/Os and ADC
  - On-chip voltage regulator with external ballast transistor
- Operating temperature range –40 to 105 °C

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Preliminary—Subject to Change Without Notice

Table of Contents

1 Overview

The MPC560xS family of devices is designed to enable the development of automotive instrument cluster applications by providing a single-chip solution capable of hosting real-time applications and driving a TFT display directly using an on-chip color TFT display controller.

MPC560xS devices incorporate a cost-efficient host processor core compliant with the Power Architecture™ embedded category. The processor is 100% user-mode compatible with the original PowerPC user instruction set architecture (UISA) and capitalizes on the available development infrastructure of current Power Architecture devices with full support from available software drivers, operating systems and configuration code to assist with users' implementations.

Offering high performance processing at speeds up to 64 MHz, the MPC560xS family is optimized for low power consumption and supports a range of on-chip SRAM and internal flash memories. The 1 MB flash version (MPC5606S) features 160 KB of on-chip graphics SRAM.

Refer to Table 1 for specific memory and feature sets of the product family members.

This document describes the features of the MPC560xS family of microcontrollers and highlights important electrical and physical characteristics of the devices. For functional characteristics, refer to the MPC560xS *Microcontroller Reference Manual.*

The following sections provide high-level descriptions of the features found on the MPC560xS.

1.1 Device Comparison

Table 1. MPC560xS family

Feature	MPC5602S	MPC5604S	MPC5606S
CPU	e200z0h		
Execution Speed	Static - 64 MHz		
Flash (ECC)	256 KB	512 KB	1 MB
EEPROM Emulation Block (ECC)	4 × 16 KB		
RAM (ECC)	24 KB	48 KB	48 KB
Graphics RAM	No	No	160 KB
MPU	12 entry		
eDMA	16 channels		
Display Control Unit	No	No	Yes
Parallel Data Interface	No	No	Yes
Stepper Motor Controller	6 motors		
Stepper Motor Stall Detect	Yes		
Sound Generation	Yes		
LCD Segment Driver	64 × 6	64 × 6	40 × 4, 38 × 6[1]
32 kHz Slow External Crystal Oscillator	Yes		
Real-Time Counter and Autonomous Periodic Interrupt	Yes	Yes	Yes

Table 1. MPC560xS family (continued)

Feature	MPC5602S	MPC5604S	MPC5606S
Periodic Interrupt Timer	4 ch, 32-bit		
System Watchdog Timer	Yes		
System Timer Module	4 ch, 32-bit		
Timed I/O[2]	8 ch, 16-bit IC/OC		
	16 ch, 16-bit OPWM/IC/OC[3]		
ADC[4]	16 channels, 10-bit		
CAN (64 Mailboxes)	1 × FlexCAN	2 × FlexCAN	2 × FlexCAN
CAN Sampler	Yes		
SCI	2 × LINFlex		
SPI	2 × DSPI	2 × DSPI	3[5] × DSPI
QuadSPI Serial Flash Interface	No	No	Yes
I^2C	2	2	4
GPIO	105	105	105 (144-pin package) 133 (176-pin package)
Debug	Nexus 1	Nexus 1	Nexus 2+[6]
Package	144 LQFP	144 LQFP	144 LQFP[7] 176 LQFP208 MAPBGA[8]

1 Configuration is software-programmable

2 IC-Input Capture, OC-Output Compare, OPWM-Output Pulse Width Modulation

3 This functionality is split over two eMIOS blocks.

4 Support for external multiplexer enabling up to 23 channels

5 QuadSPI serial Flash controller can be optionally used as a third DSPI

6 Nexus2+ available on 176 LQFP as alternate pin function and on 208 MAPBGA

7 Not all features are available simultaneously in 144 LQFP package option

8 The 208-pin package is not a production package; it is available in limited quantities for tool development only.

1.2 MPC560xS Features

- Single issue, 32-bit Power Architecture Book E compliant CPU core complex (e200z0h)
  - Compatible with classic PowerPC instruction set
  - Includes variable length encoding (VLE) instruction set for smaller code size footprint; with the encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction over conventional Book E compliant code
- On-chip ECC flash memory with flash controller
  - Up to 1 MB primary flash—two 512 KB modules with prefetch buffer and 128-bit data access port
  - 64 KB data flash—separate 4×16 KB flash block for EEPROM Emulation with prefetch buffer and 128-bit data access port
- Up to 48 KB on-chip ECC SRAM with SRAM controller
- Up to 160 KB on-chip non-ECC graphics SRAM with SRAM controller
- Memory protection unit (MPU) with up to 12 region descriptors and 32-byte region granularity to provide basic memory access permission
- Interrupt controller (INTC) with up to 127 peripheral interrupt sources and eight software interrupts
- Two frequency-modulated phase-locked loops (FMPLLs)
  - Primary FMPLL provides a 64 MHz system clock
  - Auxiliary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation
- Crossbar switch architecture enables concurrent access of peripherals, flash memory or RAM from multiple bus masters (AMBA 2.0 v6 AHB)
- 16-channel enhanced direct memory access controller (eDMA) with multiple transfer request sources using a DMA channel multiplexer
- Boot assist module (BAM) supports internal flash programming via a serial link (FlexCAN or LINFlex)
- Display control unit to drive TFT LCD displays. It includes processing of up to four planes that can be blended together and offers a direct unbuffered hardware bit-blitter of up to 16 software-configurable dynamic layers in order to drastically minimize graphic memory requirements and provide fast animations. Programmable display resolutions are available up to WVGA.
- Parallel Data Interface for digital video input
- LCD segment driver module with two software programmable configurations:
  - Up to 40 front plane drivers and 4 backplane drivers
  - Up to 38 frontplane drivers and 6 backplane drivers
- Stepper Motor Controller module with high-current drivers for up to six instrument cluster gauges driven in full dual H-Bridge configuration including full diagnostics for short circuit detection
- Stepper motor return-to-zero and stall detection module
- Sound generation and playback utilizing PWM channels and eDMA; supports monotonic and polyphonic sound
- 24 eMIOS channels providing up to 16 PWM and 24 input capture / output compare channels
- 10-bit analog-to-digital converter (ADC)
  - Maximum conversion time of 1 µs
  - Up to 16 internal channels, expandable to 23 via external multiplexing
- Up to 2 DSPI (Deserial Serial Peripheral Interface) modules for full-duplex, synchronous, communications with external devices (extendable to include up to 8 multiplexed external channels)
- QuadSPI serial flash memory controller supporting single, dual and quad modes of operation to interface to external serial flash memory. QuadSPI can be configured to function as another DSPI module (MPC5606S only).

- Two Local Interconnect Network Flexible (LINFlex) controller modules capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support. Compliant with LIN protocol rev 2.1
- Two full CAN 2.0B controllers with 64 configurable buffers each; bit rate programmable up to 1 Mbit/s
- Up to four Inter-integrated circuit (I^2C) internal bus controllers with master/slave bus interface
- Up to 133 configurable general purpose pins supporting input and output operations
- Real Time Counter (RTC) with multiple clock sources:
  - 128 kHz slow internal RC oscillator or 16 MHz fast internal RC oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
  - 32 kHz slow external crystal oscillator, supporting wakeup with 1 s resolution and maximum timeout of one hour
  - 4–16 MHz fast external crystal oscillator
- System timers:
  - 4-channel 32-bit System Timer Module (STM)—included in processor platform
  - 4-channel 32-bit Periodic Interrupt Timer (PIT) module
  - Software Watchdog Timer (SWT)
- System Integration Unit (SIU) module to manage resets, external interrupts, GPIO and pad control
- System Status and Configuration Module (SSCM) to provide information for identification of the device, last boot mode, or debug status and provides an entry point for the censorship password mechanism
- Clock Generation Module (MC_CGM) to generate system clock sources and provide a unified register interface, enabling access to all clock sources
- Clock Monitor Unit (CMU) to monitor the integrity of the main crystal oscillator and the PLL and act as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- Mode Entry Module (MC_ME) to control the device power mode, i.e., RUN, HALT, STOP, or STANDBY, control mode transition sequences, and manage the power control, voltage regulator, clock generation and clock management modules
- Reset Generation Module (MC_RGM) to manage reset assertion and release to the device at initial power-up
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board boundary-scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating the 3.3 or 5 V supply voltage down to 1.2 V for core logic (requires external ballast transistor)
- The MPC560xS microcontrollers are offered in the following packages:[1]
  - 144 LQFP, 0.5 mm pitch, 20 mm × 20 mm outline
  - 176 LQFP, 0.5 mm pitch, 24 mm × 24 mm outline
  - 208 MAPBGA, 1.0 mm pitch, 17 mm × 17 mm outline (not a production package; available in limited quantities for tool development only)

1. See the device comparison table or orderable parts summary for package offerings for each device in the family.

1.3 MPC560xS Series Blocks

1.3.1 Block Diagram

Figure 1 shows a top-level block diagram of the MPC560xS series.

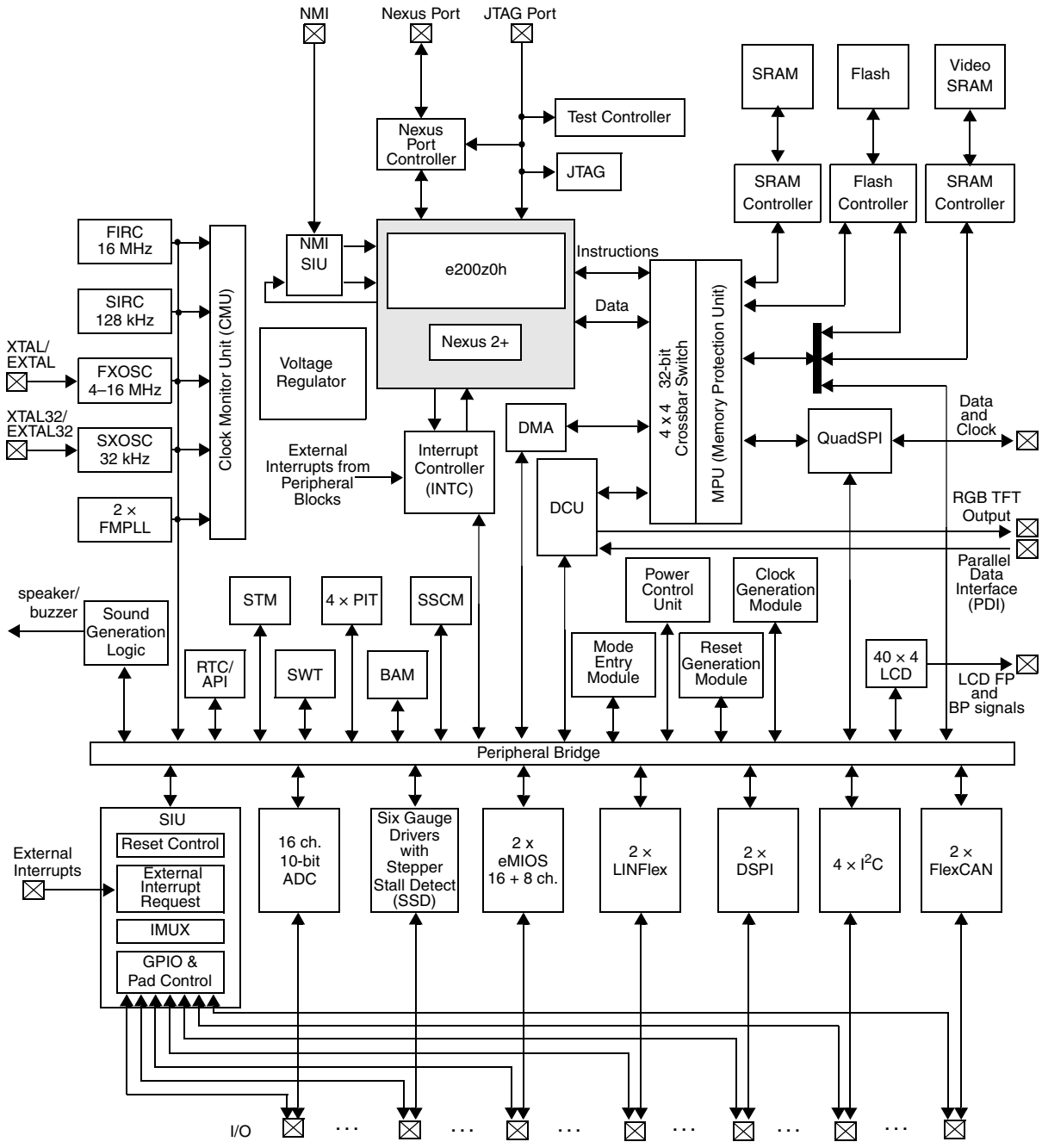


Figure 1. MPC560xS Series Block Diagram

1.3.2 Block Summary

Table 2 summarizes the functions of all blocks present in the MPC560xS series microcontrollers. Please note that the presence and number of blocks varies by device and package.

Table 2. MPC560xS Series Block Summary

Block	Function
16-channel 2nd-generation Direct Memory Access (eDMA)	Second-generation platform module capable of performing complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
AHB crossbar switch "lite" (XBAR-Lite)	Internal busmaster
Analog-to-digital converter (ADC)	16-channel, 10-bit analog to digital converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Display control unit (DCU)	Generates all signals required to drive a TFT LCD display, allowing blending of data of up to 16 layers; can also display external digital video/graphics in the background plane
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
QuadSPI (QSPI)	Provides a synchronous serial bus for communication with external serial flash memory and is optionally configurable as a third DSPI module
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Two FMPLLs generate high-speed system clocks and support programmable frequency modulation
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LCD driver module	Provides 40 × 4 (frontplane drivers × backplane drivers) or 6 × 38 driver configuration for driving LCD segments
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device

Table 2. MPC560xS Series Block Summary (continued)

Block	Function
Error Correction Status Module (ECSM)	Provides miscellaneous control functions including program-visible information about the platform configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and generic access error information for the processor core
Mode entry module (MEM)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Nexus development interface (NDI) level	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
Reset generation module (RGM)	Centralizes reset sources and manages the device reset sequence of the device
Real time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
Sound generation logic (SGL)	Provides monotonic and polyphonic sound generation capability
Stepper motor controller (SMC)	A PWM motor controller suitable for driving instruments in a cluster configuration or any other loads requiring a PWM signal
Stepper stall detect (SDD)	The SSD module connects to one stepper (SM) motor with 2 coils and is used to monitor the movement of the SM to detect that the attached gauge pointer has reached the stall position of the scale
System integration unit (SIU)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status configuration module (SSCM)	Provides system configuration and status data, e.g., memory size and status, device mode and security status, DMA status, etc., device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer (STM)	Provides a set of output compare events to support AutoSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Test control unit (TCU)	An extension of the JTAG controller module, the TCU provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode

2 Pinout and Signal Descriptions

2.1 144 LQFP Package Pinout

Figure 2 shows the pinout for the 144-pin LQFP package.

WARNING

Any pins labeled “NC” must not be connected to any external circuit.

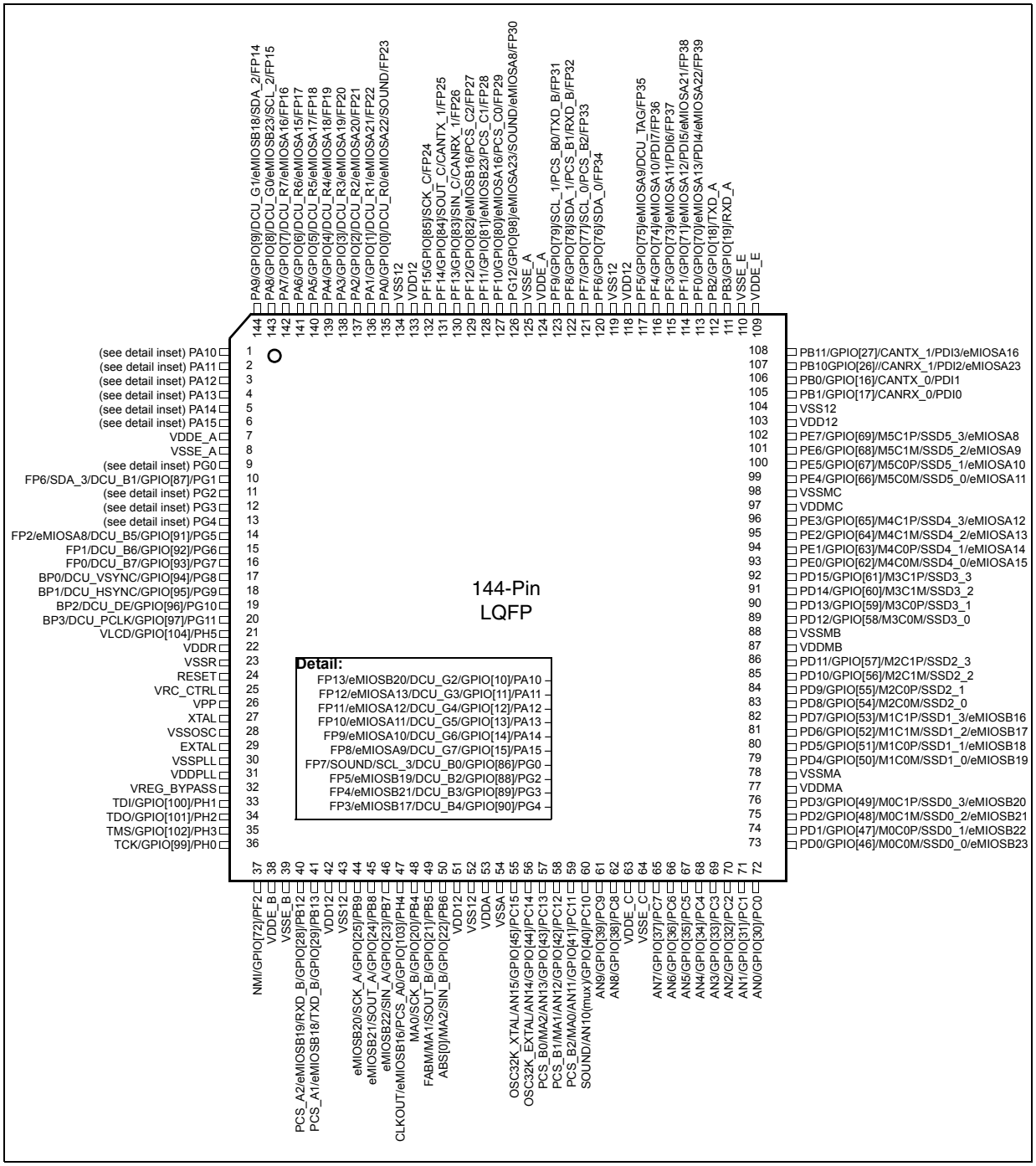


Figure 2. 144-pin LQFP Pinout

2.2 176 LQFP Package Pinout

Figure 3 shows the pinout for the 176-pin LQFP package.

WARNING

Any pins labeled “NC” must not be connected to any external circuit.

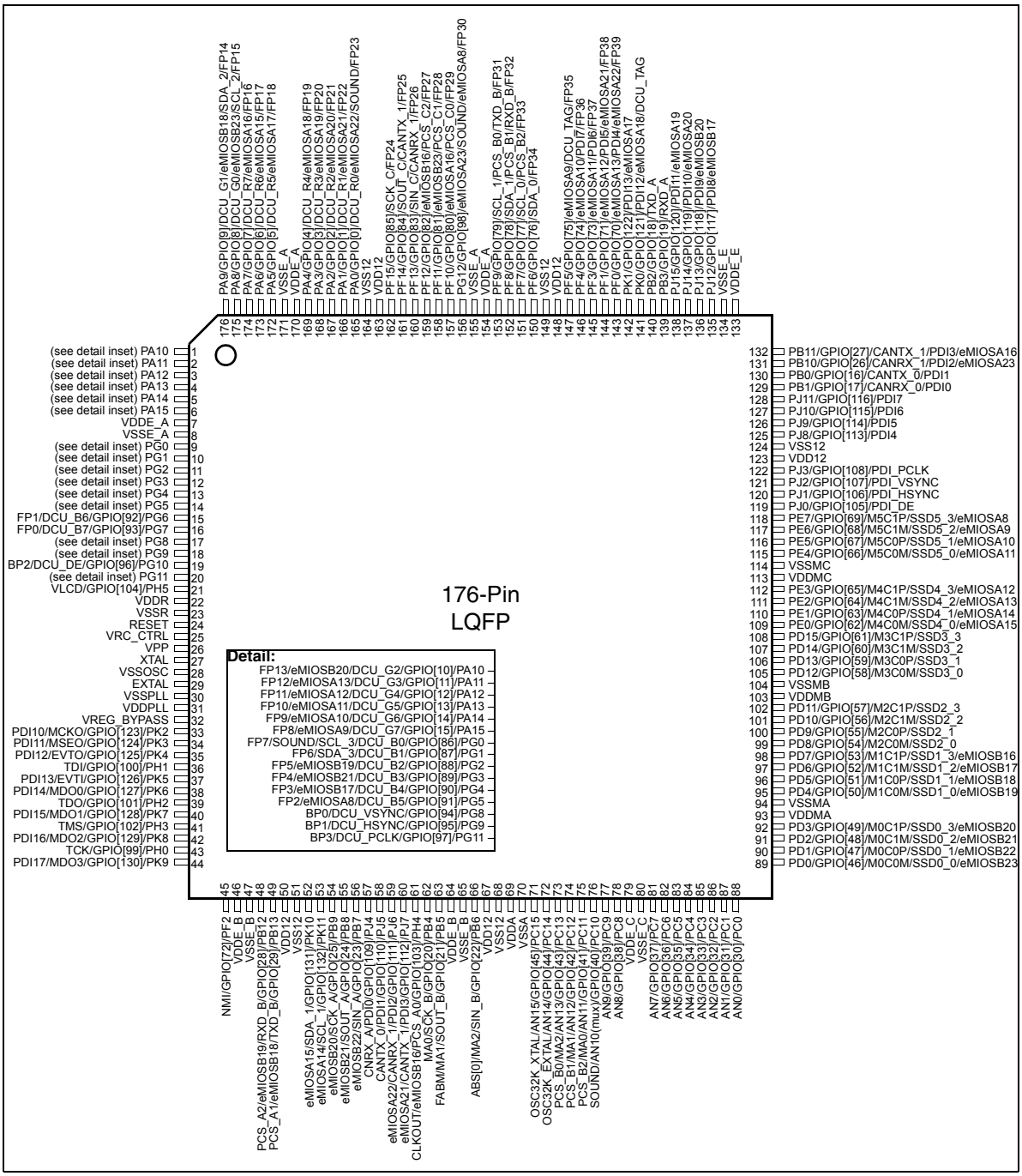


Figure 3. 176-pin LQFP Pinout

2.3 208 MAPBGA Package Ballmap

WARNING

Any pins labeled “NC” must not be connected to any external circuit.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	PA0	PJ0	PJ1	PJ3	PJ5	PJ7	PJ14	PF0	PF5	PK9	PK5	NC	NC	PF10	PF11	PF12
B	PA1	VDDE_A	PJ2	PJ4	PJ6	PJ8	PJ15	PF1	PF6	NC	PK6	PK2	NC	NC	VDDE_E	PF13
C	PA2	PA3	VDDE_A	PJ9	PJ10	PJ12	PK0	PF3	PF7	NC	PK7	PK3	NC	VDDE_E	NC	PF14
D	PA4	PA5	PG0	VDD12	PJ11	PJ13	PK1	PF4	VDD12	PG12	PK8	PK4	VDD12	NC	NC	PF15
E	PA6	PA7	PG1	PG2									NC	NC	NC	NC
F	PA8	PA9	PG3	PG4									NC	NC	NC	NC
G	PA10	PA11	PG5	PG6			VSS	VSS	VSS	VSS			NC	PE7	PE1	NC
H	PA12	PA13	PA15	PG7			VSS	VSS	VSS	VSS			PE5	PE6	VDDMC	VSSMC
J	RESET	PA14	PG8	PG10			VSS	VSS	VSS	VSS			PE4	PE2	PE0	PD8
K	EXTAL	VDDE_A	PG9	PG11			VSS	VSS	VSS	VSS			PE3	PD13	PD9	PD7
L	VSSPLL	VDDPLL	NMI/PF2	MDO3									PD15	PD12	VDDMB	VSSMB
M	XTAL	VPP	PH3	VREG BYPASS									PD14	PD11	PD5	PD6
N	VDDR	VLCD	PH2	VDD12	PK11	PK10	PB8	PB5	PC13	PC9	PC6	PB11	VDDMA	PD10	PD4	PD3
P	VRC_CTRL	PH1	VDDE_B	MDO2	MDO1	PB13	PB7	PB4	PC12	PC8	PC5	PC3	PB10	NC	PD2	PD1
R	PH0	VDDE_B	EVTO	PF9	PH4	PB12	PB6	PC15	PC11	PC7	PC4	PC2	PB3	PB2	VDDE_B	PD0
T	MCKO	MSEO	EVTI	PF8	MDO0	PB9	VDDE_C	PC14	PC10	VSSA	VDDA	PC1	PC0	PB1	PB0	VSSMA

Figure 4. 208-pin MAPBGA Pinout

2.4 Signal Description

The following sections provide signal descriptions and related information about the functionality and configuration.

2.4.1 Pad Configuration during Reset Phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are floating with the following exceptions:

- $\overline{\text{RESET}}$ pad is driven low. This is released only after PHASE2 reset completion.
- Main oscillator pads (EXTAL, XTAL) are tristate.
- Pull-up:
  - EVTI (208 MAPBGA package only)
  - PB[5] (FAB)—Without external strong pull-down the device starts fetching from flash.
  - PH[0] TCK
  - PH[1] TDI
  - PH[3] TMS

2.4.2 Voltage Supply Pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

Please note that there is a preferred power-up sequence for devices in the MPC560xS family. That sequence is described in the following paragraphs.

Broadly, the supply voltages can be grouped as follows:

- VREG HV supply (V_{DDR})
- Generic IO supply or noise free supply
  - V_{DDA}
  - V_{DDE_A}
  - V_{DDE_B}
  - V_{DDE_C}
  - V_{DDE_E}
  - V_{DDMA}
  - V_{DDMB}
  - V_{DDMC}
  - V_{DDPLL}
- LV supply (V_{DD12})

The preferred order of ramp up is as follows:

1. Generic IO supply or noise free supply
2. VREG HV supply (V_{DDR} - Should be the last HV supply to ramp up. It is also OK if all HV supplies including V_{DDR} ramp up together)
3. LV supply

The reason for following this sequence is to ensure that when VREG releases its LVDs, the I/O and other HV segments are powered properly. This is important because the MPC560xS does not monitor LVDs on I/O HV supplies.

Table 3. Voltage Supply Pin Descriptions

Supply pin	Function	Pin number		
		144 LQFP	176 LQFP	208 MAPBGA
V_{DD12}[1]	1.2 V core supply (1.08 V–1.32 V)	42, 51, 103, 118, 133	50, 67, 123, 148, 163	D4, D9, D13, N4
V_{SS12}	Low voltage ground for core domain	43, 52, 104, 119, 134	51, 68, 124, 149, 164	—
V_{SS}	Low voltage ground	—	—	G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10
V_{DDA}	3.3 V/5 V reference voltage and analog supply for A/D converter	53	69	T11
V_{SSA}	Reference ground and analog ground for A/D converter	54	70	T10
V_{DDR}	Voltage regulator VREG supply	22	22	N1
V_{SSR}	Voltage regulator ground	23	23	—
V_{DDE_A}	3.3 V/5 V I/O supply. This supply is shared with internal flash and 16 MHz fast internal RC oscillator.	7, 124	7, 154, 170	B2, C3, K2
V_{SSE_A}	3.3 V/5 V I/O supply ground	8, 125	8, 155, 171	—
V_{DDE_B}	3.3 V/5 V I/O supply. 4–16 MHz fast external crystal oscillator shares this supply.	38	46, 64	P3, R2, R15
V_{SSE_B}	3.3 V/5 V I/O supply ground	39	47, 65	—
V_{DDE_C}	3.3 V/5 V I/O supply. 32 kHz slow external crystal oscillator shares this supply with ADC.	63	79	T7
V_{SSE_C}	3.3 V/5 V I/O supply ground	64	80	—
V_{DDE_E}	3.3 V/5 V I/O supply	109	133	B15, C14
V_{SSE_E}	3.3 V/5 V I/O supply ground	110	134	—
V_{DDMA}[2]	Stepper motor 5 V pad supply. SSD shares this supply.	77	93	N13
V_{SSMA}	Stepper motor ground	78	94	T16
V_{DDMB}[2]	Stepper motor 5 V pad supply. SSD shares this supply.	87	103	L15
V_{SSMB}	Stepper motor ground	88	104	L16
V_{DDMC}[2]	Stepper motor 5 V pad supply. SSD shares this supply.	97	113	H15
V_{SSMC}	Stepper motor ground	98	114	H16
V_{DDPLL}	1.2 V PLL supply	31	31	L2

Table 3. Voltage Supply Pin Descriptions (continued)

Supply pin	Function	Pin number		
		144 LQFP	176 LQFP	208 MAPBGA
V_{SSPLL}	PLL ground	30	30	L1
V_{SSOSC}	Oscillator ground	28	28	—
V_{LCD}[3]	LCD supply option	21	21	N2
V_{PP}[4]	9 V–12 V flash test analog write signal	26	26	M2

1 Decoupling capacitors must be connected between these pins and the nearest V_{SS12} pin.
2 All stepper motor supplies need to be at same level (3.3 V or 5 V).
3 Refer to LCD segment of Reference manual for usage of VLCD as supply/reference voltage source.
4 This signal needs to be connected to ground during normal operation.

2.4.3 Pad Types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[1]
M = Medium[1,2]
F = Fast[1,2]
J = Fast/Medium/Slow Input/Output pads with analog feature
SMD = Stepper motor driver Input/Output pads
X = Oscillator

2.4.4 System Pins

The system pins are listed in Table 4.

1. Refer to Section 3.9, “I/O Pad Electrical Characteristics, for details
2. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (refer to PCR.SRC in the device reference manual, Pad Configuration Registers (PCR0–PCR120)).

Table 4. System Pin Descriptions

System pin	Function	I/O direction	Pad type	RESET configuration	Pin number		
					144 LQFP	176 LQFP	208 MAPBGA
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter	I/O	M	Input, weak pull-up	24	24	J1
EXTAL	Analog output of the oscillator amplifier circuit. Input for the clock generator in bypass mode.	O	X	—	29	29	K1
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	X	—	27	27	M1
VRC_CTRL	Voltage Regulator external NPN Ballast base control pin	O	—	—	25	25	P1
VREG_BYPASS[1]	Pin used during device test.	I	—	—	32	32	M4

[1] This pin should be tied to ground in normal use.

2.4.5 Nexus Pins

Table 5. Nexus Pins

System pin	Function	Pin number		
		144 LQFP	176 LQFP	208 MAPBGA
$\overline{\text{EVTI}}$	Nexus Event In	—	37	T3
$\overline{\text{EVTO}}$	Nexus Event Out	—	35	R3
MCKO	Nexus Message Clock Out	—	33	T1
MDO[0]	Nexus Message Data Out	—	38	T5
MDO[1]	Nexus Message Data Out	—	40	P5
MDO[2]	Nexus Message Data Out	—	42	P4
MDO[3]	Nexus Message Data Out	—	44	L4
$\overline{\text{MSE0}}$	Nexus Message Start/End Out	—	34	T2

2.4.6 Functional Ports A, B, C, D, E, F, G, H, I, J, K

The functional port pins are listed in Table 6.

Table 6. Port pin summary

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PA[0]	PCR[0]	Option 0 Option 1 Option 2 Option 3	GPIO[0] DCU_R0 eMIOSA[22] SOUND	FP23	SIU DCU PWM/Timer Sound	I/O	M	None, None	135	165	A1
PA[1]	PCR[1]	Option 0 Option 1 Option 2 Option 3	GPIO[1] DCU_R1 eMIOSA[21] —	FP22	SIU DCU PWM/Timer —	I/O	M	None, None	136	166	B1
PA[2]	PCR[2]	Option 0 Option 1 Option 2 Option 3	GPIO[2] DCU_R2 eMIOSA[20] —	FP21	SIU DCU PWM/Timer —	I/O	M	None, None	137	167	C1
PA[3]	PCR[3]	Option 0 Option 1 Option 2 Option 3	GPIO[3] DCU_R3 eMIOSA[19] —	FP20	SIU DCU PWM/Timer —	I/O	M	None, None	138	168	C2
PA[4]	PCR[4]	Option 0 Option 1 Option 2 Option 3	GPIO[4] DCU_R4 eMIOSA[18] —	FP19	SIU DCU PWM/Timer —	I/O	M	None, None	139	169	D1
PA[5]	PCR[5]	Option 0 Option 1 Option 2 Option 3	GPIO[5] DCU_R5 eMIOSA[17] —	FP18	SIU DCU PWM/Timer —	I/O	M	None, None	140	172	D2
PA[6]	PCR[6]	Option 0 Option 1 Option 2 Option 3	GPIO[6] DCU_R6 eMIOSA[15] —	FP17	SIU DCU PWM/Timer —	I/O	M	None, None	141	173	E1
PA[7]	PCR[7]	Option 0 Option 1 Option 2 Option 3	GPIO[7] DCU_R7 eMIOSA[16] —	FP16	SIU DCU PWM/Timer —	I/O	M	None, None	142	174	E2

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PA[8]	PCR[8]	Option 0 Option 1 Option 2 Option 3	GPIO[8] DCU_G0 eMIOSB[23] SCL_2	FP15	SIU DCU PWM/Timer I^2C_2	I/O	M	None, None	143	175	F1
PA[9]	PCR[9]	Option 0 Option 1 Option 2 Option 3	GPIO[9] DCU_G1 eMIOSB[18] SDA_2	FP14	SIU DCU PWM/Timer I^2C_2	I/O	M	None, None	144	176	F2
PA[10]	PCR[10]	Option 0 Option 1 Option 2 Option 3	GPIO[10] DCU_G2 eMIOSB[20] —	FP13	SIU DCU PWM/Timer —	I/O	M	None, None	1	1	G1
PA[11]	PCR[11]	Option 0 Option 1 Option 2 Option 3	GPIO[11] DCU_G3 eMIOSA[13] —	FP12	SIU DCU PWM/Timer —	I/O	M	None, None	2	2	G2
PA[12]	PCR[12]	Option 0 Option 1 Option 2 Option 3	GPIO[12] DCU_G4 eMIOSA[12] —	FP11	SIU DCU PWM/Timer —	I/O	M	None, None	3	3	H1
PA[13]	PCR[13]	Option 0 Option 1 Option 2 Option 3	GPIO[13] DCU_G5 eMIOSA[11] —	FP10	SIU DCU PWM/Timer —	I/O	M	None, None	4	4	H2
PA[14]	PCR[14]	Option 0 Option 1 Option 2 Option 3	GPIO[14] DCU_G6 eMIOSA[10] —	FP9	SIU DCU PWM/Timer —	I/O	M	None, None	5	5	J2
PA[15]	PCR[15]	Option 0 Option 1 Option 2 Option 3	GPIO[15] DCU_G7 eMIOSA[9] —	FP8	SIU DCU PWM/Timer —	I/O	M	None, None	6	6	H3

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PB[0]	PCR[16]	Option 0 Option 1 Option 2 Option 3	GPIO[16] CANTX_A PDI1 —	—	SIU CAN-A PDI —	I/O	M	None, None	106	130	T15
PB[1]	PCR[17]	Option 0 Option 1 Option 2 Option3	GPIO[17] CANRX_A PDI0 —	—	SIU CAN-A PDI —	I/O	S	None, None	105	129	T14
PB[2]	PCR[18]	Option 0 Option 1 Option 2 Option3	GPIO[18] TXD_A — —	—	SIU LIN_A — —	I/O	S	None, None	112	140	R14
PB[3]	PCR[19]	Option 0 Option 1 Option 2 Option3	GPIO[19] RXD_A — —	—	SIU LIN_A — —	I/O	S	None, None	111	139	R13
PB[4]	PCR[20]	Option 0 Option 1 Option 2 Option 3	GPIO[20] SCK_B MA0 —	—	SIU SPI_1 ADC —	I/O	M	None, None	48	62	P8
PB[5]	PCR[21]	Option 0 Option 1 Option 2 Option 3	GPIO[21] SOUT_B MA1 FABM	—	SIU SPI_1 ADC Control	I/O	M	Input, Pull-down	49	63	N8
PB[6]	PCR[22]	Option 0 Option 1 Option 2 Option 3	GPIO[22] SIN_B MA2 ABS[0]	—	SIU SPI_1 ADC Control	I/O	S	Input, Pull-up	50	66	R7
PB[7]	PCR[23]	Option 0 Option 1 Option 2 Option 3	GPIO[23] SIN_A eMIOSB[22] —	—	SIU SPI_A PWM/Timer —	I/O	S	None, None	46	56	P7

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PB[8]	PCR[24]	Option 0 Option 1 Option 2 Option 3	GPIO[24] SOUT_A eMIOSB[21] —	—	SIU SPI_A PWM/Timer —	I/O	M	None, None	45	55	N7
PB[9]	PCR[25]	Option 0 Option 1 Option 2 Option 3	GPIO[25] SCK_A eMIOSB[20] —	—	SIU SPI_A PWM/Timer —	I/O	M	None, None	44	54	T6
PB[10]	PCR[26]	Option 0 Option 1 Option 2 Option 3	GPIO[26] CANRX_1 PDI2 eMIOSA[23]	—	SIU CAN-1 PDI PWM/Timer	I/O	S	None, None	107	131	P13
PB[11]	PCR[27]	Option 0 Option 1 Option 2 Option 3	GPIO[27] CANTX_1 PDI3 eMIOSA[16]	—	SIU CAN-1 PDI PWM/Timer	I/O	M	None, None	108	132	N12
PB[12]	PCR[28]	Option 0 Option 1 Option 2 Option 3	GPIO[28] RXD_B eMIOSB[19] PCS_A2	—	SIU LIN_B PWM/Timer SPI_0	I/O	S	None, None	40	48	R6
PB[13]	PCR[29]	Option 0 Option 1 Option 2 Option 3	GPIO[29] TXD_B eMIOSB[18] PCS_A1	—	SIU LIN_B PWM/Timer SPI_0	I/O	S	None, None	41	49	P6
PB[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PB[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PC[0]	PCR[30]	Option 0 Option 1 Option 2 Option 3	GPIO[30] AN[0] — —	—	SIU ADC — —	I/O	S	None, None	72	88	T13
PC[1]	PCR[31]	Option 0 Option 1 Option 2 Option 3	GPIO[31] AN[1] — —	—	SIU ADC — —	I/O	S	None, None	71	87	T12

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PC[2]	PCR[32]	Option 0 Option 1 Option 2 Option 3	GPIO[32] AN[2] — —	—	SIU ADC — —	I/O	S	None, None	70	86	R12
PC[3]	PCR[33]	Option 0 Option 1 Option 2 Option 3	GPIO[33] AN[3] — —	—	SIU ADC — —	I/O	S	None, None	69	85	P12
PC[4]	PCR[34]	Option 0 Option 1 Option 2 Option 3	GPIO[34] AN[4] — —	—	SIU ADC — —	I/O	S	None, None	68	84	R11
PC[5]	PCR[35]	Option 0 Option 1 Option 2 Option 3	GPIO[35] AN[5] — —	—	SIU ADC — —	I/O	S	None, None	67	83	P11
PC[6]	PCR[36]	Option 0 Option 1 Option 2 Option 3	GPIO[36] AN[6] — —	—	SIU ADC — —	I/O	S	None, None	66	82	N11
PC[7]	PCR[37]	Option 0 Option 1 Option 2 Option 3	GPIO[37] AN[7] — —	—	SIU ADC — —	I/O	S	None, None	65	81	R10
PC[8]	PCR[38]	Option 0 Option 1 Option 2 Option 3	GPIO[38] AN[8] — —	—	SIU ADC — —	I/O	S	None, None	62	78	P10
PC[9]	PCR[39]	Option 0 Option 1 Option 2 Option 3	GPIO[39] AN[9] — —	—	SIU ADC — —	I/O	S	None, None	61	77	N10

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PC[10]	PCR[40]	Option 0 Option 1 Option 2 Option 3	GPIO[40] AN[10] SOUND —	—	SIU ADC Sound —	I/O	J	None, None	60	76	T9
PC[11]	PCR[41]	Option 0 Option 1 Option 2 Option 3	GPIO[41] AN[11] MA0 PCS_B2	—	SIU ADC ADC SPI_B	I/O	J	None, None	59	75	R9
PC[12]	PCR[42]	Option 0 Option 1 Option 2 Option 3	GPIO[42] AN[12] MA1 PCS_B1	—	SIU ADC ADC SPI_B	I/O	J	None, None	58	74	P9
PC[13]	PCR[43]	Option 0 Option 1 Option 2 Option 3	GPIO[43] AN[13] MA2 PCS_B0	—	SIU ADC ADC SPI_B	I/O	J	None, None	57	73	N9
PC[14]	PCR[44]	Option 0 Option 1 Option 2 Option 3	GPIO[44] AN[14] OSC32K_EXTAL —	—	SIU ADC Osc —	I/O	J	None, None	56	72	T8
PC[15]	PCR[45]	Option 0 Option 1 Option 2 Option 3	GPIO[45] AN[15] OSC32K_XTAL —	—	SIU ADC Osc —	I/O	J	None, None	55	71	R8
PD[0]	PCR[46]	Option 0 Option 1 Option 2 Option 3	GPIO[46] M0C0M SSD0_0 eMIOSB[23]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	73	89	R16
PD[1]	PCR[47]	Option 0 Option 1 Option 2 Option 3	GPIO[47] M0C0P SSD0_1 eMIOSB[22]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	74	90	P16

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PD[2]	PCR[48]	Option 0 Option 1 Option 2 Option 3	GPIO[48] M0C1M SSD0_2 eMIOSB[21]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	75	91	P15
PD[3]	PCR[49]	Option 0 Option 1 Option 2 Option 3	GPIO[49] M0C1P SSD0_3 eMIOSB[20]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	76	92	N16
PD[4]	PCR[50]	Option 0 Option 1 Option 2 Option 3	GPIO[50] M1C0M SSD1_0 eMIOSB[19]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	79	95	N15
PD[5]	PCR[51]	Option 0 Option 1 Option 2 Option 3	GPIO[51] M1C0P SSD1_1 eMIOSB[18]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	80	96	M15
PD[6]	PCR[52]	Option 0 Option 1 Option 2 Option 3	GPIO[52] M1C1M SSD1_2 eMIOSB[17]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	81	97	M16
PD[7]	PCR[53]	Option 0 Option 1 Option 2 Option 3	GPIO[53] M1C1P SSD1_3 eMIOSB[16]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	82	98	K16
PD[8]	PCR[54]	Option 0 Option 1 Option 2 Option 3	GPIO[54] M2C0M SSD2_0 —	—	SIU SMD SSD —	I/O	SMD	None, None	83	99	J16
PD[9]	PCR[55]	Option 0 Option 1 Option 2 Option 3	GPIO[55] M2C0P SSD2_1 —	—	SIU SMD SSD —	I/O	SMD	None, None	84	100	K15

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PD[10]	PCR[56]	Option 0 Option 1 Option 2 Option 3	GPIO[56] M2C1M SSD2_2 —	—	SIU SMD SSD —	I/O	SMD	None, None	85	101	N14
PD[11]	PCR[57]	Option 0 Option 1 Option 2 Option 3	GPIO[57] M2C1P SSD2_3 —	—	SIU SMD SSD —	I/O	SMD	None, None	86	102	M14
PD[12]	PCR[58]	Option 0 Option 1 Option 2 Option 3	GPIO[58] M3C0M SSD3_0 —	—	SIU SMD SSD —	I/O	SMD	None, None	89	105	L14
PD[13]	PCR[59]	Option 0 Option 1 Option 2 Option 3	GPIO[59] M3C0P SSD3_1 —	—	SIU SMD SSD —	I/O	SMD	None, None	90	106	K14
PD[14]	PCR[60]	Option 0 Option 1 Option 2 Option 3	GPIO[60] M3C1M SSD3_2 —	—	SIU SMD SSD —	I/O	SMD	None, None	91	107	M13
PD[15]	PCR[61]	Option 0 Option 1 Option 2 Option 3	GPIO[61] M3C1P SSD3_3 —	—	SIU SMD SSD —	I/O	SMD	None, None	92	108	L13
PE[0]	PCR[62]	Option 0 Option 1 Option 2 Option 3	GPIO[62] M4C0M SSD4_0 eMIOSA[15]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	93	109	J15
PE[1]	PCR[63]	Option 0 Option 1 Option 2 Option 3	GPIO[63] M4C0P SSD4_1 eMIOSA[14]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	94	110	G15

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PE[2]	PCR[64]	Option 0 Option 1 Option 2 Option 3	GPIO[64] M4C1M SSD4_2 eMIOSA[13]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	95	111	J14
PE[3]	PCR[65]	Option 0 Option 1 Option 2 Option 3	GPIO[65] M4C1P SSD4_3 eMIOSA[12]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	96	112	K13
PE[4]	PCR[66]	Option 0 Option 1 Option 2 Option 3	GPIO[66] M5C0M SSD5_0 eMIOSA[11]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	99	115	J13
PE[5]	PCR[67]	Option 0 Option 1 Option 2 Option 3	GPIO[67] M5C0P SSD5_1 eMIOSA[10]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	100	116	H13
PE[6]	PCR[68]	Option 0 Option 1 Option 2 Option 3	GPIO[68] M5C1M SSD5_2 eMIOSA[9]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	101	117	H14
PE[7]	PCR[69]	Option 0 Option 1 Option 2 Option 3	GPIO[69] M5C1P SSD5_3 eMIOSA[8]	—	SIU SMD SSD PWM/Timer	I/O	SMD	None, None	102	118	G14
PE[8]	—	—	Reserved	—	—	—	—	—	—	—	—
PE[9]	—	—	Reserved	—	—	—	—	—	—	—	—
PE[10]	—	—	Reserved	—	—	—	—	—	—	—	—
PE[11]	—	—	Reserved	—	—	—	—	—	—	—	—
PE[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PE[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PE[14]	—	—	Reserved	—	—	—	—	—	—	—	—

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PE[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PF[0]	PCR[70]	Option 0 Option 1 Option 2 Option 3	GPIO[70] eMIOSA[13] PDI4 eMIOSA[22]	FP39	SIU PWM/Timer PDI PWM/Timer	I/O	S	None, None	113	143	A8
PF[1]	PCR[71]	Option 0 Option 1 Option 2 Option 3	GPIO[71] eMIOSA[12] PDI5 eMIOSA[21]	FP38	SIU PWM/Timer PDI PWM/Timer	I/O	S	None, None	114	144	B8
PF[2]	PCR[72]	Option 0 Option 1 Option 2 Option 3	GPIO[72] NMI — —	—	SIU NMI — —	I/O	S	None, None	37	45	L3
PF[3]	PCR[73]	Option 0 Option 1 Option 2 Option 3	GPIO[73] eMIOSA[11] PDI6 —	FP37	SIU PWM/Timer PDI —	I/O	M	None, None	115	145	C8
PF[4]	PCR[74]	Option 0 Option 1 Option 2 Option 3	GPIO[74] eMIOSA[10] PDI7 —	FP36	SIU PWM/Timer PDI —	I/O	M	None, None	116	146	D8
PF[5]	PCR[75]	Option 0 Option 1 Option 2 Option 3	GPIO[75] eMIOSA[9] DCU_TAG —	FP35	SIU PWM/Timer DCU —	I/O	M	None, None	117	147	A9
PF[6]	PCR[76]	Option 0 Option 1 Option 2 Option 3	GPIO[76] SDA_0 — —	FP34	SIU I^2C_0 — —	I/O	S	None, None	120	150	B9
PF[7]	PCR[77]	Option 0 Option 1 Option 2 Option 3	GPIO[77] SCL_0 PCS_B2 —	FP33	SIU I^2C_0 SPI_B —	I/O	S	None, None	121	151	C9

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PF[8]	PCR[78]	Option 0 Option 1 Option 2 Option 3	GPIO[78] SDA_1 PCS_B1 RXD_B	FP32	SIU I^2C_1 SPI_B LIN_B	I/O	S	None, None	122	152	T4
PF[9]	PCR[79]	Option 0 Option 1 Option 2 Option 3	GPIO[79] SCL_1 PCS_B0 TXD_B	FP31	SIU I^2C_1 SPI_B LIN_B	I/O	S	None, None	123	153	R4
PF[10]	PCR[80]	Option 0 Option 1 Option 2 Option 3	GPIO[80] eMIOSA[16] PCS_C0 —	FP29	SIU PWM/Timer QuadSPI —	I/O	M	None, None	127	157	A14
PF[11]	PCR[81]	Option 0 Option 1 Option 2 Option 3	GPIO[81] eMIOSB[23] PCS_C1 —	FP28	SIU PWM/Timer QuadSPI —	I/O	M	None, None	128	158	A15
PF[12]	PCR[82]	Option 0 Option 1 Option 2 Option 3	GPIO[82] eMIOSB[16] PCS_C2 —	FP27	SIU PWM/Timer QuadSPI —	I/O	M	None, None	129	159	A16
PF[13]	PCR[83]	Option 0 Option 1 Option 2 Option 3	GPIO[83] SIN_C CANRX_1 —	FP26	SIU QuadSPI CAN_1 —	I/O	M	None, None	130	160	B16
PF[14]	PCR[84]	Option 0 Option 1 Option 2 Option 3	GPIO[84] SOUT_C CANTX_B —	FP25	SIU QuadSPI CAN_B —	I/O	M	None, None	131	161	C16
PF[15]	PCR[85]	Option 0 Option 1 Option 2 Option 3	GPIO[85] SCK_C — —	FP24	SIU QuadSPI — —	I/O	F	None, None	132	162	D16

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PG[0]	PCR[86]	Option 0 Option 1 Option 2 Option 3	GPIO[86] DCU_B0 SCL_3 SOUND	FP7	SIU DCU I^{2}C_3 Sound	I/O	M	None, None	9	9	D3
PG[1]	PCR[87]	Option 0 Option 1 Option 2 Option 3	GPIO[87] DCU_B1 SDA_3 —	FP6	SIU DCU I^{2}C_3 —	I/O	M	None, None	10	10	E3
PG[2]	PCR[88]	Option 0 Option 1 Option 2 Option 3	GPIO[88] DCU_B2 eMIOSB[19] —	FP5	SIU DCU PWM/Timer —	I/O	M	None, None	11	11	E4
PG[3]	PCR[89]	Option 0 Option 1 Option 2 Option 3	GPIO[89] DCU_B3 eMIOSB[21] —	FP4	SIU DCU PWM/Timer —	I/O	M	None, None	12	12	F3
PG[4]	PCR[90]	Option 0 Option 1 Option 2 Option 3	GPIO[90] DCU_B4 eMIOSB[17] —	FP3	SIU DCU PWM/Timer —	I/O	M	None, None	13	13	F4
PG[5]	PCR[91]	Option 0 Option 1 Option 2 Option 3	GPIO[91] DCU_B5 eMIOSA[8] —	FP2	SIU DCU PWM/Timer —	I/O	M	None, None	14	14	G3
PG[6]	PCR[92]	Option 0 Option 1 Option 2 Option 3	GPIO[92] DCU_B6 — —	FP1	SIU DCU — —	I/O	M	None, None	15	15	G4
PG[7]	PCR[93]	Option 0 Option 1 Option 2 Option 3	GPIO[93] DCU_B7 — —	FP0	SIU DCU — —	I/O	M	None, None	16	16	H4

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PG[8]	PCR[94]	Option 0 Option 1 Option 2 Option 3	GPIO[94] DCU_VSYNC — —	BP0	SIU DCU — —	I/O	M	Input, None	17	17	J3
PG[9]	PCR[95]	Option 0 Option 1 Option 2 Option 3	GPIO[95] DCU_HSYNC — —	BP1	SIU DCU — —	I/O	M	Input, None	18	18	K3
PG[10]	PCR[96]	Option 0 Option 1 Option 2 Option 3	GPIO[96] DCU_DE — —	BP2	SIU DCU — —	I/O	M	None, None	19	19	J4
PG[11]	PCR[97]	Option 0 Option 1 Option 2 Option 3	GPIO[97] DCU_PCLK — —	BP3	SIU DCU — —	I/O	M	None, None	20	20	K4
PG[12]	PCR[98]	Option 0 Option 1 Option 2 Option 3	GPIO[98] eMIOSA[23] SOUND eMIOSA[8]	FP30	SIU PWM/Timer Sound PWM/Timer	I/O	S	None, None	126	156	D10
PG[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PG[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PG[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[0][5]	PCR[99]	Option 0 Option 1 Option 2 Option 3	GPIO[99] TCK — —	—	SIU JTAG — —	I/O	S	Input, Pull-up	36	43	R1
PH[1][5]	PCR[100]	Option 0 Option 1 Option 2 Option 3	GPIO[100] TDI — —	—	SIU JTAG — —	I/O	S	Input, Pull-up	33	36	P2

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PH[2][5]	PCR[101]	Option 0 Option 1 Option 2 Option 3	GPIO[101] TDO — —	—	SIU JTAG — —	I/O	M	Output, None	34	39	N3
PH[3][5]	PCR[102]	Option 0 Option 1 Option 2 Option 3	GPIO[102] TMS — —	—	SIU JTAG — —	I/O	S	Input, Pull-up	35	41	M3
PH[4]	PCR[103]	Option 0 Option 1 Option 2 Option 3	GPIO[103] PCS_A0 eMIOSB[16] CLKOUT	—	SIU SPI_0 PWM/Timer Control	I/O	F	None, None	47	61	R5
PH[5]	PCR[104]	Option 0 Option 1 Option 2 Option 3	GPIO[104] VLCD[6] — —	—	SIU LCD — —	I/O	S	None, None	21	21	N2
PH[6]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[7]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[8]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[9]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[10]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[11]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PJ[0]	PCR[105]	Option 0 Option 1 Option 2 Option 3	GPIO[105] PDI_DE — —	—	SIU PDI — —	I/O	S	None, None	—	119	A2

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PJ[1]	PCR[106]	Option 0 Option 1 Option 2 Option 3	GPIO[106] PDI_HSYNC — —	—	SIU PDI — —	I/O	S	None, None	—	120	A3
PJ[2]	PCR[107]	Option 0 Option 1 Option 2 Option 3	GPIO[107] PDI_VSYNC — —	—	SIU PDI — —	I/O	S	None, None	—	121	B3
PJ[3]	PCR[108]	Option 0 Option 1 Option 2 Option 3	GPIO[108] PDI_PCLK — —	—	SIU PDI — —	I/O	M	None, None	—	122	A4
PJ[4]	PCR[109]	Option 0 Option 1 Option 2 Option 3	GPIO[109] PDI[0] CANRX_0 —	—	SIU PDI CAN-0 —	I/O	S	None, None	—	57	B4
PJ[5]	PCR[110]	Option 0 Option 1 Option 2 Option 3	GPIO[110] PDI[1] CANTX_0 —	—	SIU PDI CAN-0 —	I/O	M	None, None	—	58	A5
PJ[6]	PCR[111]	Option 0 Option 1 Option 2 Option 3	GPIO[111] PDI[2] CANRX_1 eMIOSA[22]	—	SIU PDI CAN-1 PWM/Timer	I/O	S	None, None	—	59	B5
PJ[7]	PCR[112]	Option 0 Option 1 Option 2 Option 3	GPIO[112] PDI[3] CANTX_1 eMIOSA[21]	—	SIU PDI CAN-1 PWM/Timer	I/O	M	None, None	—	60	A6
PJ[8]	PCR[113]	Option 0 Option 1 Option 2 Option 3	GPIO[113] PDI[4] — —	—	SIU PDI — —	I/O	S	None, None	—	125	B6

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PJ[9]	PCR[114]	Option 0 Option 1 Option 2 Option 3	GPIO[114] PDI[5] — —	—	SIU PDI — —	I/O	S	None, None	—	126	C4
PJ[10]	PCR[115]	Option 0 Option 1 Option 2 Option 3	GPIO[115] PDI[6] — —	—	SIU PDI — —	I/O	S	None, None	—	127	C5
PJ[11]	PCR[116]	Option 0 Option 1 Option 2 Option 3	GPIO[116] PDI[7] — —	—	SIU PDI — —	I/O	S	None, None	—	128	D5
PJ[12]	PCR[117]	Option 0 Option 1 Option 2 Option 3	GPIO[117] PDI[8] eMIOSB[17] —	—	SIU PDI PWM/Timer —	I/O	M	None, None	—	135	C6
PJ[13]	PCR[118]	Option 0 Option 1 Option 2 Option 3	GPIO[118] PDI[9] eMIOSB[20] —	—	SIU PDI PWM/Timer —	I/O	M	None, None	—	136	D6
PJ[14]	PCR[119]	Option 0 Option 1 Option 2 Option 3	GPIO[119] PDI[10] eMIOSA[20] —	—	SIU PDI PWM/Timer —	I/O	M	None, None	—	137	A7
PJ[15]	PCR[120]	Option 0 Option 1 Option 2 Option 3	GPIO[120] PDI[11] eMIOSA[19] —	—	SIU PDI PWM/Timer —	I/O	M	None, None	—	138	B7
PK[0]	PCR[121]	Option 0 Option 1 Option 2 Option 3	GPIO[121] PDI[12] eMIOSA[18] DCU_TAG	—	SIU PDI PWM/Timer DCU	I/O	M	None, None	—	141	C7

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PK[1]	PCR[122]	Option 0 Option 1 Option 2 Option 3	GPIO[122] PDI[13] eMIOSA[17] —	—	SIU PDI PWM/Timer —	I/O	M	None, None	—	142	D7
PK[2]	PCR[123]	Option 0 Option 1 Option 2 Option 3	GPIO[123] MCKO PDI[10] —	—	SIU Nexus PDI —	I/O	F	None, None	—	33	B12
PK[3]	PCR[124]	Option 0 Option 1 Option 2 Option 3	GPIO[124] MSEO PDI[11] —	—	SIU Nexus PDI —	I/O	M	None, None	—	34	C12
PK[4]	PCR[125]	Option 0 Option 1 Option 2 Option 3	GPIO[125] EVTO PDI[12] —	—	SIU Nexus PDI —	I/O	M	None, None	—	35	D12
PK[5]	PCR[126]	Option 0 Option 1 Option 2 Option 3	GPIO[126] EVTI PDI[13] —	—	SIU Nexus PDI —	I/O	M	None, None	—	37	A11
PK[6]	PCR[127]	Option 0 Option 1 Option 2 Option 3	GPIO[127] MDO0 PDI[14] —	—	SIU Nexus PDI —	I/O	M	None, None	—	38	B11
PK[7]	PCR[128]	Option 0 Option 1 Option 2 Option 3	GPIO[128] MDO1 PDI[15] —	—	SIU Nexus PDI —	I/O	M	None, None	—	40	C11
PK[8]	PCR[129]	Option 0 Option 1 Option 2 Option 3	GPIO[129] MDO2 PDI[16] —	—	SIU Nexus PDI —	I/O	M	None, None	—	42	D11

Table 6. Port pin summary (continued)

Port Pin	PCR Register	Alternate Function[1]	Function	Special Function	Peripheral[2]	I/O Direction	Pad Type[3]	RESET Config.[4]	Pin Number		
									144 LQFP	176 LQFP	208 MAPBGA
PK[9]	PCR[130]	Option 0 Option 1 Option 2 Option 3	GPIO[130] MDO3 PDI[17] —	—	SIU Nexus PDI —	I/O	M	None, None	—	44	A10
PK[10]	PCR[131]	Option 0 Option 1 Option 2 Option 3	GPIO[131] SDA_1 eMIOSA[15] —	—	SIU I^2C_1 PWM/Timer —	I/O	S	None, None	—	52	N6
PK[11]	PCR[132]	Option 0 Option 1 Option 2 Option 3	GPIO[132] SCL_1 eMIOSA[14] —	—	SIU I^2C_1 PWM/Timer —	I/O	S	None, None	—	53	N5
PK[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[15]	—	—	Reserved	—	—	—	—	—	—	—	—

1 Alternate functions are chosen by setting the values of the PCR[n].PA bitfields inside the SIU module. PCR[n].PA = 00 -> Option 0; PCR[n].PA = 01 -> Option 1; PCR[n].PA = 10 -> Option 2; PCR[n].PA = 11-> Option 3. This is intended to select the output functions; to use one of the input functions, the PCR[n].IBE bit must be written to '1', regardless of the values selected in the PCR[n].PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2 USing the PSMI registers in the System Integration Unit (SIU), different pads can be multiplexed to the same peripheral input. Please see the MPC560xS *Reference Manual* for details.

3 S = Slow, M = Medium, F = Fast, J = Fast/Medium/Slow I/O pad with analog feature, SMD = Stepper motor driver, X = Oscillator

4 Reset configuration is given as I/O direction and pull, e.g., "Input, pullup".

5 Out of reset pins PH[0:3] are available as JTAG pins (TCK, TDI, TDO and TMS respectively). It is up to the user to configure pins PH[0:3] when needed.

6 This pin can be used for LCD supply pin VLCD. Refer Table 3 for details

2.4.7 Signal Details

Table 7. Signal details

Signal	Peripheral	Description
ABS[0]	BAM	Alternate Boot Select. Gives an option to boot by downloading code via CAN or LIN.
AN[0:15]	Analog-to-digital conversion (ADC)	Inputs used to bring into the device sensor-based signals for A/D conversion.
MA[0:2]	ADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
FABM		Force Alternate Boot mode. Forces the device to boot from the external bus (Can or LIN). If not asserted, the device boots up from the lowest flash sector containing a valid boot signature.
DCU_DE	Display Control Unit	Indicates that valid pixels are present when high; otherwise low to allow a subframe display for pixels.
DCU_HSYNC	Display Control Unit	Horizontal sync pulse for TFT-LCD display
DCU_PCLK	Display Control Unit	Output pixel clock for TFT-LCD display
DCU_R[0:7], DCU_G[0:7], DCU_B[0:7]	Display Control Unit	Red, green and blue color 8-bit Pixel values for TFT-LCD displays
DCU_TAG	Display Control Unit	High indicates certain pixels that can be called as tagged pixels, upon which internal CRC has been calculated based on pixel values and pixel position.
DCU_VSYNC	Display Control Unit	Vertical sync pulse for TFT-LCD display
PCS_A[0:2], PCS_B[0:2]	DSPI	Peripheral chip selects when device is in Master mode; not used in slave modes.
SCK_A, SCK_B	DSPI	SPI clock signal—bidirectional
SIN_A, SIN_B	DSPI	SPI data input signal
SOUT_A, SOUT_B	DSPI	SPI data output signal
eMIOSA[8:23], eMIOSB[16:23]	eMIOS	Enhanced Modular Input Output System. 16+8 channel eMIOS for timed input or output functions.
CANRX_0, CANRX_1	FlexCAN	Receive (RX) pins for the CAN bus transceiver
CANTX_0, CANTX_1	FlexCAN	Transmit (TX) pins for the CAN bus transceiver
SCL_0, SCL_1, SCL_2, SCL_3	I^2C	Bidirectional serial clock compatible with I^2C specifications
SDA_0, SDA_1, SDA_2, SDA_3	I^2C	Bidirectional serial data compatible with I^2C specifications

Table 7. Signal details (continued)

Signal	Peripheral	Description
TCK	JTAG	Debug port serial clock as per JTAG specifications
TDI	JTAG	Debug port serial data input port as per JTAG standards specifications
TDO	JTAG	Debug port serial data output port as per JTAG standards specifications
TMS	JTAG	Debug port Test Mode Select signal for the JTAG TAP controller state machine and indicates various state transitions for the TAP controller in the device
BP[0:3]	LCD	Backplane signals from the LCD controlling the backplane reference voltage for the LCD display
FP[0:39]	LCD	Frontplane signals for LCD segments
$\overline{\text{EVTI}}$	Nexus	Nexus2+ event input trigger
$\overline{\text{EVTO}}$	Nexus	Nexus2+ event output trigger
MCKO	Nexus	Output clock for the development tool
MDO[0:3]	Nexus	Message output port pins that send information bits to the development tools for messages such as Branch Trace Message (BTM), Ownership Trace Message (OTM), Data Trace Message (DTM). Only available in reduced port mode.
$\overline{\text{MSEO}}$	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins
PDI[0:17]	Parallel Data Interface	Video/graphic data in various RGB modes input to the DCU
PDI_DE	Parallel Data Interface	Input signal indicates the validity of pixel data on the Input PDI data bus. For valid Pixel Data this is high, otherwise low.
PDI_HSYNC	Parallel Data Interface	Input indicates the timing reference for the start of each frame line for the PDI Input data.
PDI_PCLK	Parallel Data Interface	Output pixel clock for PDI
PDI_VSYNC	Parallel Data Interface	Input indicates the timing reference for the start of a frame for the PDI input data.
RXD_A	LINFlex-UART	SCI/LIN Receive data signal—This port is used to download the code for the BAM boot sequence.
RXD_B	LINFlex-UART	SCI/LIN Receive data signal. Input pad for the LIN SCI module. Connects to the internal LIN second port.
TXD_A	LINFlex-UART	This port is used to download the code for the BAM boot sequence.
TXD_B	LINFlex-UART	SCI/LIN Transmit data signal—Transmit (output) port for the second LIN module in the chip

Table 7. Signal details (continued)

Signal	Peripheral	Description
SOUND	Sound generation logic (SGL)	Sound signal to the speaker/buzzer
SSD[0:5]_0 SSD[0:5]_1 SSD[0:5]_2 SSD[0:5]_3	SSD (Stepper Stall Detect) Interface	Bidirectional SSD inputs and control signals
M[0:5]C0M M[0:5]C0P M[0:5]C1M M[0:5]C1P	Stepper Motor Control (SMC) Interface	Controls stepper motors in various configuration
CLKOUT	Clock generation module (MC_CGM)	Output clock—It can be selected from several internal clocks of the device from the clock generation module.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by internal pull up and pull down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 8 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter Classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Non-Volatile User Options Register (NVUSRO) register.

3.3.1 NVUSRO[PAD3V5V] field description

Table 9 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 9. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 See the device reference manual for more information on the NVUSRO register.

2 Default manufacturing value before Flash initialization is ‘1’ (3.3 V)

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 9 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 10. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1 See the device reference manual for more information on the NVUSRO register.

2 Default manufacturing value before Flash initialization is ‘1’

The 4–16 MHz fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

3.4 Absolute Maximum Ratings

Table 11. Absolute Maximum Ratings

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SSA})		–0.3	5.5	V
		C		Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDPLL}	CC	C	Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground (V_{SSPLL})		1.08	1.32	V
		C		Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSPLL}	SR	C	Voltage on VSSMC (stepper motor supply ground) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDR}	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})		–0.3	5.5	V
		C		Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD12}	CC	C	Voltage on VDD12 pin with respect to ground (V_{SS12})		1.08	1.4	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDE_A}[1]	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})		–0.3	5.5	V
V_{DDE_B}[1]	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})		–0.3	5.5	V
V_{DDE_C}[1]	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})		–0.3	5.5	V
V_{DDE_E}[1]	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})		–0.3	5.5	V
V_{DDMA}[1]	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})		–0.3	5.5	V
V_{DDMB}[1]	SR	C	Voltage on VDDMB (stepper motor supply) pin with respect to ground (V_{SSMB})		–0.3	5.5	V
V_{DDMC}[1]	SR	C	Voltage on VDDMC (stepper motor supply) pin with respect to ground (V_{SSMC})		–0.3	5.5	V
V_{SS}[2]	SR	C	I/O supply ground		0	0	V
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}		0	V_{DDE_A} + 0.3	V

Table 11. Absolute Maximum Ratings (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{IN}	SR	C	Voltage on any GPIO pin with respect to ground (V_{SS})		–0.3	5.5	V
		C		Relative to V_{DD}	–0.3	V_{DD} + 0.3	
I_{INJPAD}	SR	C	Injected input current on any pin during overload condition		–10	10	mA
I_{INJSUM}	SR	C	Absolute sum of all injected input currents during overload condition		–50	50	
$T_{STORAGE}$	SR	C	Storage temperature		–55	150	°C

1 Throughout the remainder of this document V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}, unless otherwise noted.

2 Throughout the remainder of this document V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}, unless otherwise noted.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.4.1 Recommended Operating Conditions

NOTE

Minimum slew rate for the supplies to ramp up should be 1 second, which is slowest ramp-up time.

Table 12. Recommended Operating Conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})		3.0	3.6	V
		C		Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDPLL}	CC	C	Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground (V_{SSPLL})		1.08	1.32	V
V_{SSPLL}	SR	C	Voltage on VSSMC (stepper motor supply ground) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDR}[2]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})		3.0	3.6	V
		C		Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	

Table 12. Recommended Operating Conditions (3.3 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD12}[3,4]	CC	C	Voltage on VDD12 pin with respect to ground (V_{SS12})		1.08	1.4	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD}[5,6,7]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})		3.0	3.6	V
V_{SS}[8]	SR	C	I/O supply ground		0	0	V
V_{DDE_A}	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})		3.0	3.6	V
V_{DDE_B}	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})		3.0	3.6	V
V_{DDE_C}[9]	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})		3.0	3.6	V
V_{DDE_E}	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})		3.0	3.6	V
V_{DDMA}	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})		3.0	3.6	V
V_{DDMB}	SR	C	Voltage on VDDMB (stepper motor supply) pin with respect to ground (V_{SSMB})		3.0	3.6	V
V_{DDMC}	SR	C	Voltage on VDDMC (stepper motor supply) pin with respect to ground (V_{SSMC})		3.0	3.6	V
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}		0	0	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}		0	V_{DDE_A} + 0.3	V
TV_{DD}	SR	C	V_{DD} slope to ensure correct power up[10]		5 V/s	0.25	V/µs
T_A	SR	C	Ambient temperature under bias		–40	105	°C
T_J	SR	C	Junction temperature under bias		–40	150	

1 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.

2 200 µF capacitance must be connected between V_{DDR} and V_{SS12}. This is required because of sharp surge due to external ballast.

3 V_{DD12} cannot be used to drive any external component.

4 Each V_{DD12}/V_{SS12} supply pair should have a 10 µF capacitor. Absolute combined maximum capacitance is 40 µF.

5 V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}.

6 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair

7 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/O's DC electrical specification may not be guaranteed.
When voltage drops below V_{LVDHVL} device is reset.

[8] V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}) unless otherwise noted.

[9] V_{DDE_C} should be the same as V_{DDA} with a 100 mV variation, i.e., $V_{DDE\_C} = V_{DDA} \pm 100$ mV.

[10] Guaranteed by device validation

Table 13. Recommended Operating Conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})		4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDPLL}	CC	C	Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground (V_{SSPLL})		1.08	1.32	V
V_{SSPLL}	SR	C	Voltage on VSSMC (stepper motor supply ground) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDR}[3]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})		4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD12}[4,5]	CC	C	Voltage on VDD12 pin with respect to ground (V_{SS12})		1.08	1.4	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD}[6,7]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	Voltage drop[2]	4.5	5.5	V
V_{SS}[8]	SR	C	I/O supply ground		0	0	V
V_{DDE_A}	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})		4.5	5.5	V
V_{DDE_B}	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})		4.5	5.5	V
V_{DDE_C}[9]	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})		4.5	5.5	V
V_{DDE_E}	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})		4.5	5.5	V
V_{DDMA}	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})		4.5	5.5	V
V_{DDMB}	SR	C	Voltage on VDDMB (stepper motor supply) pin with respect to ground (V_{SSMB})		4.5	5.5	V
V_{DDMC}	SR	C	Voltage on VDDMC (stepper motor supply) pin with respect to ground (V_{SSMC})		4.5	5.5	V

Table 13. Recommended Operating Conditions (5.0 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}		0	0	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}		0	V_{DDE_A} + 0.3	V
TV_{DD}	SR	C	V_{DD} slope to ensure correct power up			0.25	V/µs
T_A	SR	C	Ambient temperature under bias		–40	105	°C
T_J	SR	C	Junction temperature under bias		–40	150	°C

1 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.

2 Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, I/O DC and ADC electrical characteristics may not be guaranteed below 4.5 V during the voltage drop sequence.

3 200 µF capacitance must be connected between V_{DDR} and V_{SS12}. This is required because of sharp surge due to external ballast.

4 V_{DD12} cannot be used to drive any external component.

5 Each V_{DD12}/V_{SS12} supply pair should have a 10 µF capacitor. Absolute combined maximum capacitance is 40 µF.

6 V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}.

7 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair

8 V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}) unless otherwise noted.

9 V_{DDE_C} should be the same as V_{DDA} with a 100 mV variation, i.e., V_{DDE_C} = V_{DDA} ±100 mV.

3.5 Thermal Characteristics

Table 14. LQFP Thermal Characteristics[1]

Symbol		C	Parameter	Conditions	Value		Unit
					144-pin	176-pin	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[2]	Single layer board—1s	50	43	°C/W
	CC			Four layer board—2s2p	41	35	°C/W
$R_{\theta JMA}$	CC	D	Thermal resistance, junction-to-moving-air ambient[2]	@ 200 ft./min., single layer board—1s	41	35	°C/W
	CC			@ 200 ft./min., four layer board—2s2p	35	30	°C/W
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[3]		29	24	°C/W
$R_{\theta JCtop}$	CC	D	Thermal resistance, junction-to-case (top)[4]		10	9	°C/W
Ψ_{JT}	CC	D	Junction-to-package top thermal characterization parameter, natural convection[5]		2	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

[2] Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[3] Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[4] Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[5] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General Notes for Specifications at Maximum Junction Temperature

An estimate of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using Equation 2:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \textit{Eqn. 2}$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8S

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ s device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using Equation 4:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043 USA
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

3.6 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.6.1 EMC requirements on board

The following practices help minimize noise in applications.

- A 10 µF capacitor should be placed between each of the three V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair.
- VDDR should have a 220 µF capacitor. Also, VDDR should be isolated with ballast emitter to avoid voltage droop during standby mode exit.
- PAD slew rate enabled as much as possible to eliminate I/O noise
- PLL modulation enabled for system clock.
- Decoupling capacitors for all HV supplies to be placed close to the pins.

3.6.2 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

3.6.3 Electromagnetic interference (EMI)

Table 15. EMI Testing Specifications[1]

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	SR	T	Scan range		TBD	TBD	TBD	MHz
—	SR	T	Operating frequency		TBD	TBD	TBD	MHz

Table 15. EMI Testing Specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	SR	T	VDD12, VDDPLL operating voltages		TBD	TBD	TBD	V
—	SR	T	VDD, VDDA operating voltages		TBD	TBD	TBD	V
—	SR	T	Maximum amplitude		TBD	TBD	TBD	dBµV
—	SR	T	Operating temperature		TBD	TBD	TBD	°C

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03.

3.6.4 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.6.4.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 16. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.6.4.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 17. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 105 °C conforming to JESD 78	II level A

3.7 Power Management Electrical Characteristics

3.7.1 Voltage Regulator Electrical Characteristics

The internal voltage regulator requires an external NPN (BCP56 or BCP68) ballast to be connected as shown in Figure 5 as well as an external capacitance (C_{REG}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 15 nH.

For the MPC560xS microcontroller, 10 µF should be placed between each of the three V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair. Additionally, 220 µF should be placed between the V_{DDR} pin and the adjacent V_{SS} pin.

V_{DDR} = 3.0 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 to 105 °C, unless otherwise specified.

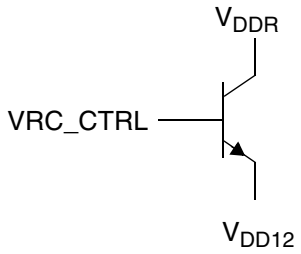


Figure 5. External NPN Ballast Connections

Table 18. Voltage Regulator Electrical Characteristics[1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	V_{DDR}	SR	C	Power supply		3.0	5.5	V
2	T_J	SR	C	Junction temperature		–40	150	°C
3	I_{REG}	CC	C	Current consumption	Reference included, @ 55 °C No load @ Full load	—	 2 11	mA
4	I_L	CC	C	Output current capacity	DC load current	—	200	mA
5	V_{DD12}	CC	C	Output voltage (value @ I_L = 0 @ 27 °C)	Pre-trimming sigma < 7 mV	—	1.330	V
			C		Post-trimming	1.260	1.290	
			C	Output voltage (value @ $I_L = I_{max}$)	Post-trimming	1.145	—	

Table 18. Voltage Regulator Electrical Characteristics[1] (continued)

No.	Symbol		C	Parameter		Conditions	Value		Unit
							Min	Max	
6		SR	C	External decoupling/stability capacitor		4 capacitances of 10 µF each	10 × 4		µF
			C			ESR of external cap	0.05	0.2	ohm
			C			1 bond wire R + 1 pad R	0.2	1	ohm
7	L_{BOND}	CC	D	Bonding Inductance for Bipolar Base Control pad			0	15	nH
8		CC	D	Power supply rejection	@ DC @ no load	C_L = 10 µF × 4	—	–30	dB
			D		@ 200 kHz @ no load			–100	
			D		@ DC @ 400 mA			–30	
			D		@ 200 kHz @ 400 mA			–30	
9		CC	D	Load current transient		C_L = 10 µF × 4	—	10% to 90% of I_L (max) in 100 ns	
10	t_{SU}	CC	C	Start-up time after input supply stabilizes[2]		C_L = 10 µF × 4	—	100	µs

1 All values in this table are PRELIMINARY.

2 Time after the input supply to the voltage regulator has ramped up (V_{DDR}) and the voltage regulator has asserted the Power OK signal.

Table 19. Low Power Voltage Regulator Electrical Characteristics [1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	V_{DDR}	SR	C	Power supply		3.0	5.5	V
2	T_J	SR	C	Junction temperature		–40	150	°C
3	I_{REG}	CC	C	Current consumption	Reference included, @ 55 °C No load @ Full load	—	 5 600	µA
4	I_L	CC	C	Output current capacity	DC load current	—	15	mA
5	V_{DD12}	CC	C	Output voltage (value @ I_L = 0 @ 27 °C)	Pre-trimming sigma < 7 mV	—	1.330	V
			C		Post-trimming	1.23	1.24	
			C	Output voltage (value @ $I_L = I_{max}$)	Post-trimming	1.13	—	

Table 19. Low Power Voltage Regulator Electrical Characteristics (continued)[1]

No.	Symbol		C	Parameter		Conditions	Value		Unit
							Min	Max	
6		SR	C	External decoupling/stability capacitor		4 capacitances of 10 µF each	10 × 4		µF
			C			ESR of external cap	0.1	0.6	ohm
			C			1 bond wire R + 1 pad R	0.2	1	ohm
7	L_{BOND}	CC	D	Bonding Inductance for Bipolar Base Control pad			0	15	nH
8		CC	D	Power supply rejection	@ DC @ no load	C_L = 10 µF × 4	—	55	dB
			D		any frequency @ no load			32	
			D		@ DC @ max load			24	
			D		any frequency @ max load			12	
9		CC	D	Load current transient		C_L = 10 µF × 4	—	10% to 90% of I_L in 10 µs	
10	t_{SU}	CC	C	Start-up time after input supply stabilizes[2]		C_L = 10 µF × 4	—	700	µs

1 All values in this table are PRELIMINARY.

2 Time after the input supply to the voltage regulator has ramped up (V_{DDR}) and the voltage regulator has asserted the Power OK signal.

Table 20. Ultra-Low Power Voltage Regulator Electrical Characteristics [1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	V_{DDR}	SR	C	Power supply		3.0	5.5	V
2	T_J	SR	C	Junction temperature		–40	150	°C
3	I_{REG}	CC	C	Current consumption	Reference included, @ 55 °C No load @ Full load	—	 2 100	µA
4	I_L	CC	C	Output current capacity	DC load current	—	5	mA
5	V_{DD12}	CC	C	Output voltage (value @ I_L = 0 @ 27 °C)	Pre-trimming sigma < 7 mV	—	1.330	V
			C		Post-trimming	1.23	1.24	
			C	Output voltage (value @ $I_L = I_{max}$)	Post-trimming	1.13	—	

Table 20. Ultra-Low Power Voltage Regulator Electrical Characteristics (continued)[1]

No.	Symbol		C	Parameter		Conditions	Value		Unit
							Min	Max	
6		SR	C	External decoupling/stability capacitor			N/A	N/A	—
			C			ESR of external cap	N/A	N/A	—
			C			1 bond wire R + 1 pad R	N/A	N/A	—
7	L_{BOND}	CC	D	Bonding Inductance for Bipolar Base Control pad			N/A	N/A	—
8		CC	D	Power supply rejection	@ DC @ no load		—	25	dB
			D		any frequency @ no load			7	
			D		@ DC @ max load			25	
			D		any frequency @ max load			8	
9		CC	D	Load current transient			—	10 to 90 µA in 70 µs	
10	t_{SU}	CC	C	Start-up time after input supply stabilizes[2]			—	100	µs

1 All values in this table are PRELIMINARY.

2 Time after the input supply to the voltage regulator has ramped up (V_{DDR}) and the voltage regulator has asserted the Power OK signal.

3.7.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD12} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

Table 21. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{PORH}	CC	C	Power-on reset threshold		1.5	—	2.7	V
$V_{LVDHV3H}$	CC	C	LVDHV3 low voltage detector high threshold		—	—	2.8	
$V_{LVDHV5H}$	CC	C	LVDHV5 low voltage detector high threshold		—	—	4.37	
$V_{LVDHV3L}$	CC	C	LVDHV3 low voltage detector low threshold	T_A = 25 °C, after trimming	2.7	—	—	
$V_{LVDHV5L}$	CC	C	LVDHV5 low voltage detector low threshold		4.2	—	—	
$V_{LVDLVCORH}$	CC	C	LVDLVCOR low voltage detector high threshold		—	—	1.185	
$V_{LVDLVCORL}$	CC	C	LVDLVCOR low voltage detector low threshold		1.095	—	—	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3.7.3 Low voltage domain power consumption

Table 22 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 22. DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{DDMAX}	SR	C	Maximum current			—	135	—	mA
I_{DDRUN}[3]	CC	C	RUN mode current			—	130	—	mA
I_{DDWAIT}	CC	C	WAIT mode current			—	30	—	mA
I_{DDHALT}	CC	C	HALT mode current			4.5	—	12	mA
I_{DDSTOP}	CC	C	STOP mode current	16 MHz fast internal RC oscillator off		—	1.5	—	mA
				HPVREG off		—	800	—	µA
				16 MHz fast internal RC oscillator on		—	4	—	mA
$I_{DDSTDBY}$	CC	C	STANDBY mode current	16 MHz fast internal RC oscillator off	T_A = 25 °C	—	29	—	µA
					T_A = 105 °C		500		
				16 MHz fast internal RC oscillator on	T_A = 25 °C	—	300	—	
$I_{DDSTDBY2}$	CC	C	STANDBY2 mode current	32 kHz slow external crystal oscillator and RTC running	T_A = 25 °C	TBD			µA
					T_A = 55 °C				
					T_A = 85 °C				
					T_A = 105 °C				

Table 22. DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{DDSTDBY1}$	CC	C	STANDBY1 mode current	32 kHz slow external crystal oscillator and RTC running	T_A = 25 °C	TBD			µA
					T_A = 55 °C				
					T_A = 85 °C				
					T_A = 105 °C				

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C

2 All values need to be confirmed during device validation.

3 Value is for maximum peripherals turned on. May vary significantly based on different configurations, active peripherals, operating frequency, etc.

3.8 DC Electrical Specifications

3.9 I/O Pad Electrical Characteristics

3.9.1 I/O Pad Types

The device provides three main I/O pad types depending of the associated alternate functions:

- Slow pads—These are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These provide maximum speed. There are used for improved NEXUS debugging capability.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.9.2 I/O Input DC Characteristics

Table 23 provides input DC electrical characteristics as described in Figure 6.

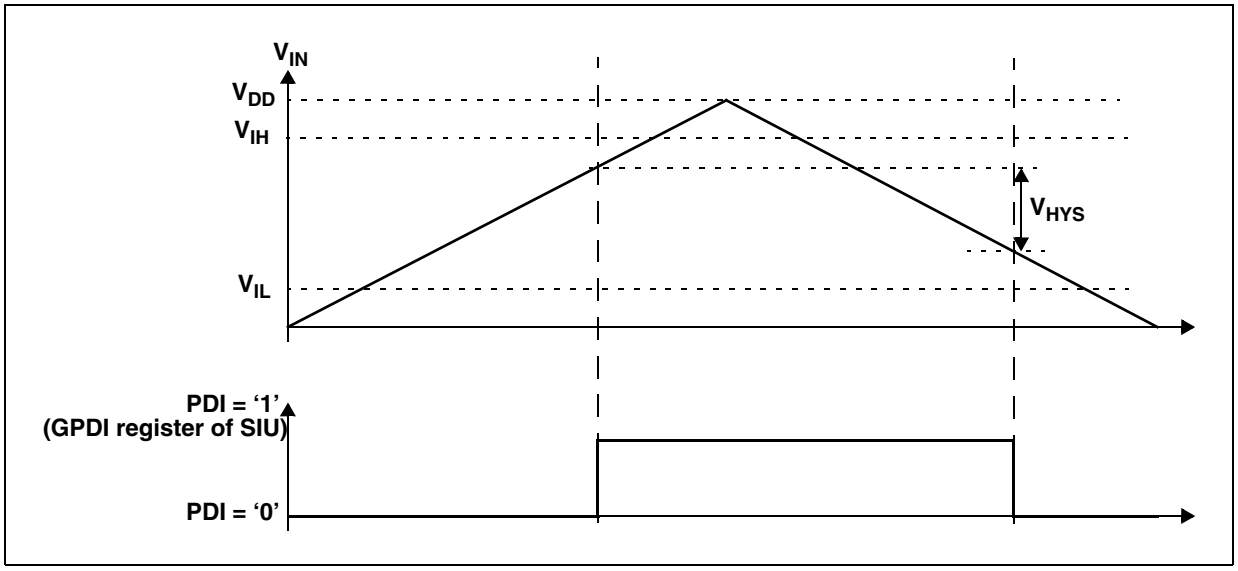


Figure 6. I/O Input DC Electrical Characteristics Definition

Table 23. I/O Input DC Electrical Characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS Schmitt Trigger		$0.65V_{DD}$		V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS Schmitt Trigger		–0.4		$0.35V_{DD}$	
V_{HYS}	CC[3]	D	Input hysteresis CMOS Schmitt Trigger		$0.1V_{DD}$			
I_{LKG}	CC	P	Input leakage current		<1			µA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C.
2 All values need to be confirmed during device validation.
3 Parameter value guaranteed by design.

3.9.3 I/O Output DC Characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 24 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 25 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 26 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 27 provides output driver characteristics for I/O pads when in FAST configuration.

Table 24. I/O Pull-up/Pull-down DC Electrical Characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value		10		150	µA
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value		10		150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

[2] All values need to be confirmed during device validation.

Table 25. SLOW Configuration Output Buffer Electrical Characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$			V
		D		Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$			
		C		Push Pull, I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8			
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)			$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]			$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)			0.5	
T_{tr}[4]	CC	T	Output transition time output pin[5] SLOW configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			50	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			100	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			125[4]	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			40	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			50	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			75[4]	
ΔI_{tr50}[4]	CC	D	Current slew at C_L = 50 pF SLOW configuration	recommended configuration at V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			2	mA/ns
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1			7	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

[2] All values need to be confirmed during device validation.

[3] This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.

[4] Data based on characterization results, not tested in production

[5] C_L calculation should include device and package capacitances (C_{PKG} < 5 pF).

Table 26. MEDIUM Configuration Output Buffer Electrical Characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level MEDIUM configuration	Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$			V
		D		Push Pull, I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$			
		C		Push Pull, I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8			
V_{OL}	CC	P	Output low level MEDIUM configuration	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)			$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]			$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)			0.5	
T_{tr}[4]	CC	T	Output transition time output pin[5] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			10	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			20	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			40	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			12	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			25	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			40	
ΔI_{tr50}[4]	CC	D	Current slew at C_L = 50 pF MEDIUM configuration	recommended configuration at V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			7	mA/ns
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1			16	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.

4 Data based on characterization results, not tested in production

5 C_L includes device and package capacitance (C_{PKG} < 5 pF).

Table 27. FAST Configuration Output Buffer Electrical Characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull, I_{OH} = –14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$			V
		D		Push Pull, I_{OH} = –7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$			
		C		Push Pull, I_{OH} = –11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8			
V_{OL}	CC	P	Output low level FAST configuration	Push Pull, I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)			$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]			$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)			0.5	
T_{tr}[4]	CC	T	Output transition time output pin[5] FAST configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			4	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			6	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			12	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			4	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			7	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			12	
ΔI_{tr50}[4]	CC	D	Current slew at C_L = 50 pF FAST configuration	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended configuration)			55	mA/ns
		D		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended configuration)			40	
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1			100	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.

4 Data based on characterization results, not tested in production

5 C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.9.4 I/O Pad Current Specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 28.

Table 29 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 28. I/O Supply Segment

Package	Supply segment				
	A[1]	B[2]	C[3,4]	D[5]	E[6]
144 LQFP	pins 1–21 pins 113–144	pins 22– 52	pins 53–72	pins 73–102	pins 103–112
176 LQFP	pins 1–21 pins 143–176	pins 22–68	pins 69–88	pins 89–118	pins 119–142

1 LCD pad segment containing pad supplies V_{DDE_A}
2 Miscellaneous pad segment containing pad supplies V_{DDE_B}
3 ADC pad segment containing pad supplies V_{DDE_C}
4 V_{DDE_C} should be the same as V_{DDA} with a 100 mV variation, i.e., $V_{DDE\_C} = V_{DDA} \pm 100$ mV.
5 Stepper Motor pad segment containing I/O supplies V_{DDMA}, V_{DDMB}, V_{DDMC}
6 Miscellaneous pad segment containing pad supplies V_{DDE_E}

Table 29. I/O Consumption

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
I_{SWTSLW}	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			20	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			16	
I_{SWTMED}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			29	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			17	
I_{SWTFST}[3]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			110	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			50	

Table 29. I/O Consumption (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			2.3	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			3.2	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			6.6[3]	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			1.6	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			2.3	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			4.7[3]	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			6.6	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			13.4	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			18.3[3]	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			5.0	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			8.5	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			11.0[3]	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			22.0	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			33.0	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			56.0[3]	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			14.0	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			20.0	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			25.0[3]	
I_{DYNSEG}	SR	D	Sum of all the dynamic and static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			110	mA
		D		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			65	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			70	mA
		D		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2 All values need to be confirmed during device validation.
3 Data based on characterization results, not tested in production

3.10 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 7. Start-up reset requirements

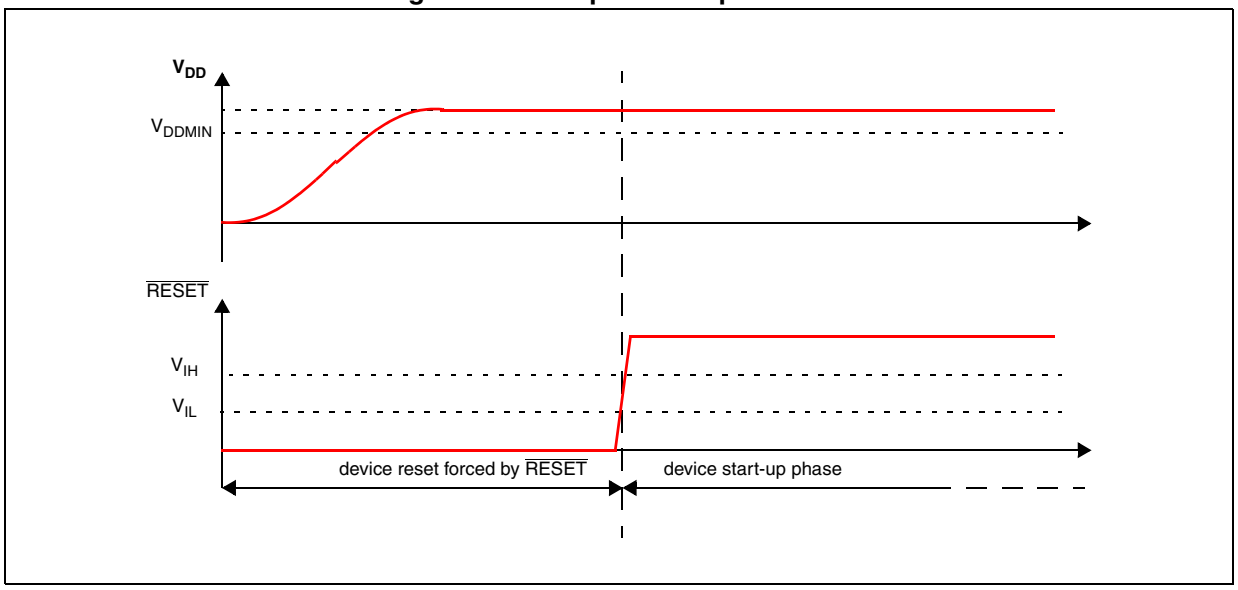


Figure 8. Noise filtering on reset signal

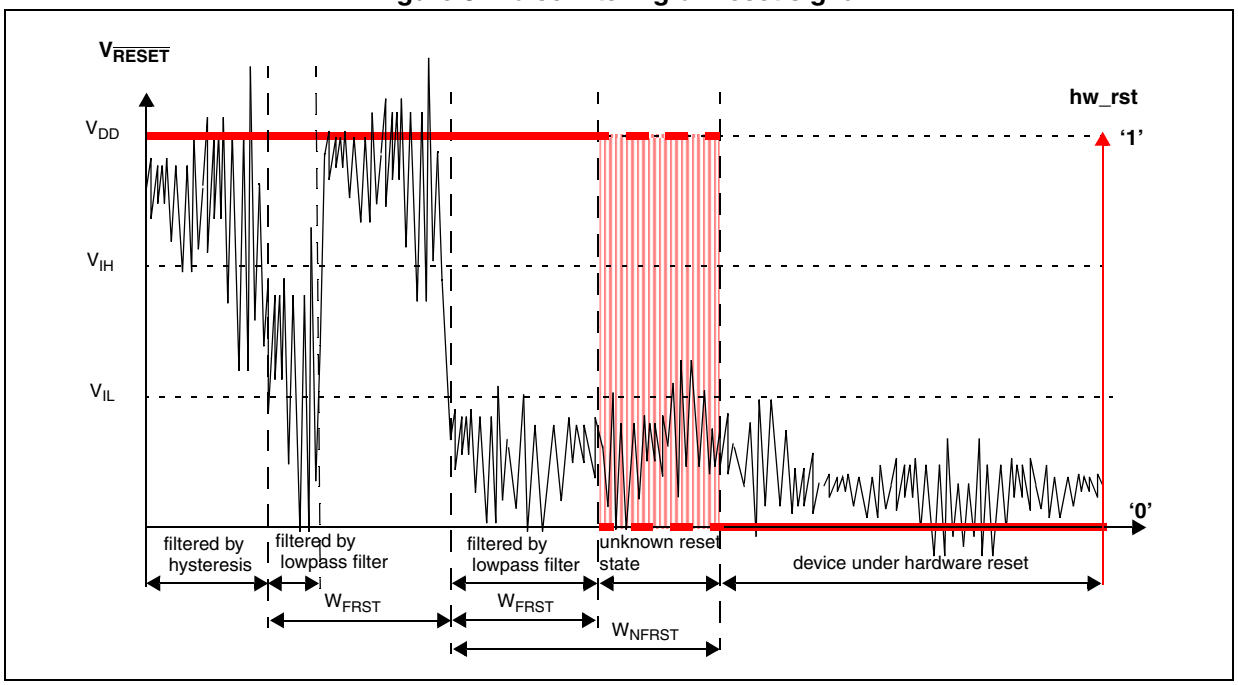


Table 30. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS Schmitt Trigger		$0.65V_{DD}$		$V_{DD} + 0.4$	V
V_{IL}	SR	P	Input low level CMOS Schmitt Trigger		–0.4		$0.35V_{DD}$	V
V_{HYS}[3]	CC	D	Input hysteresis CMOS Schmitt Trigger		$0.1V_{DD}$			V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)			$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]			$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)			0.5	
T_{tr}	CC	T	Output transition time output pin[5] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			10	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			20	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0			40	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			12	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			25	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1			40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse		—		40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse		1000	—	—	ns
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value		10		150	µA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Data based on characterization results, not tested in production

4 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to reset generation module (RGM) section of the device reference manual).

5 C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.11 Fast external crystal oscillator (4–16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 9 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

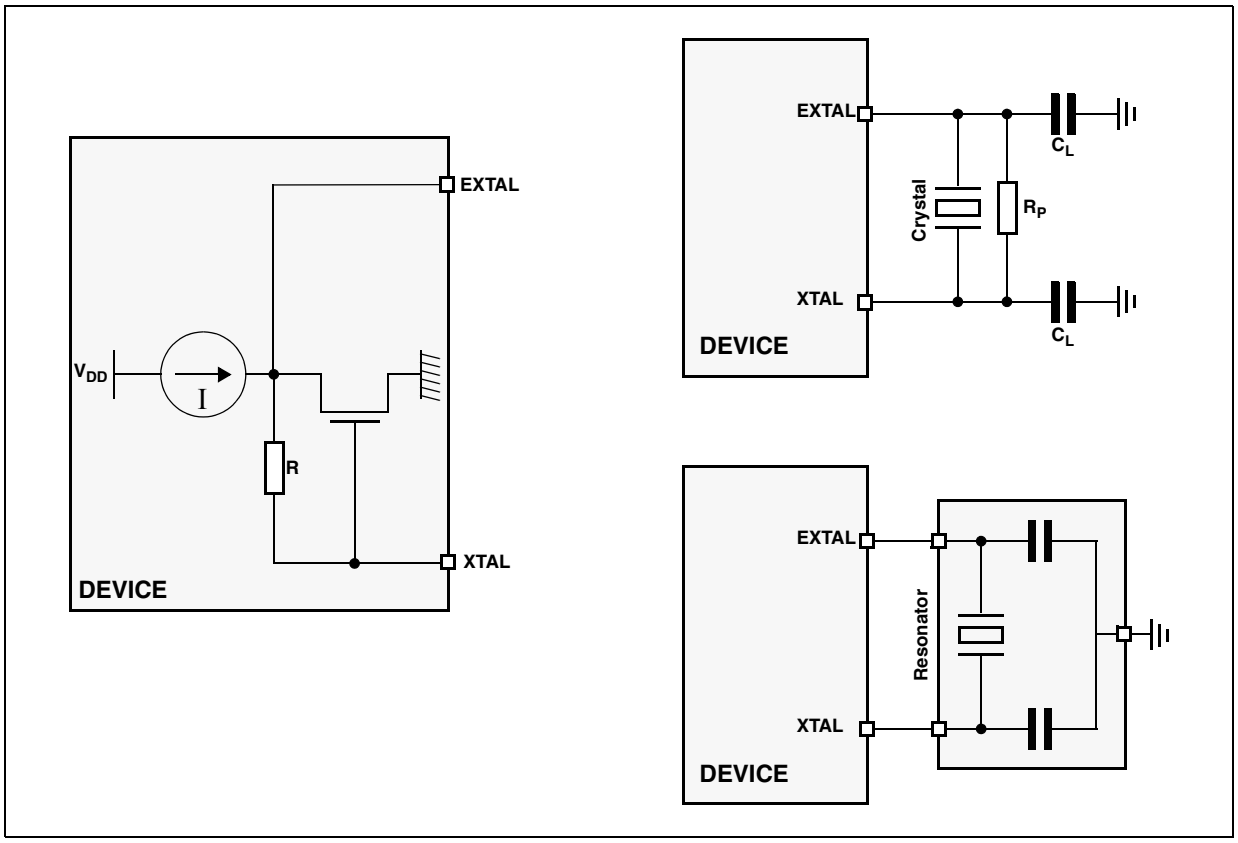


Figure 9. Crystal Oscillator and Resonator Connection Scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

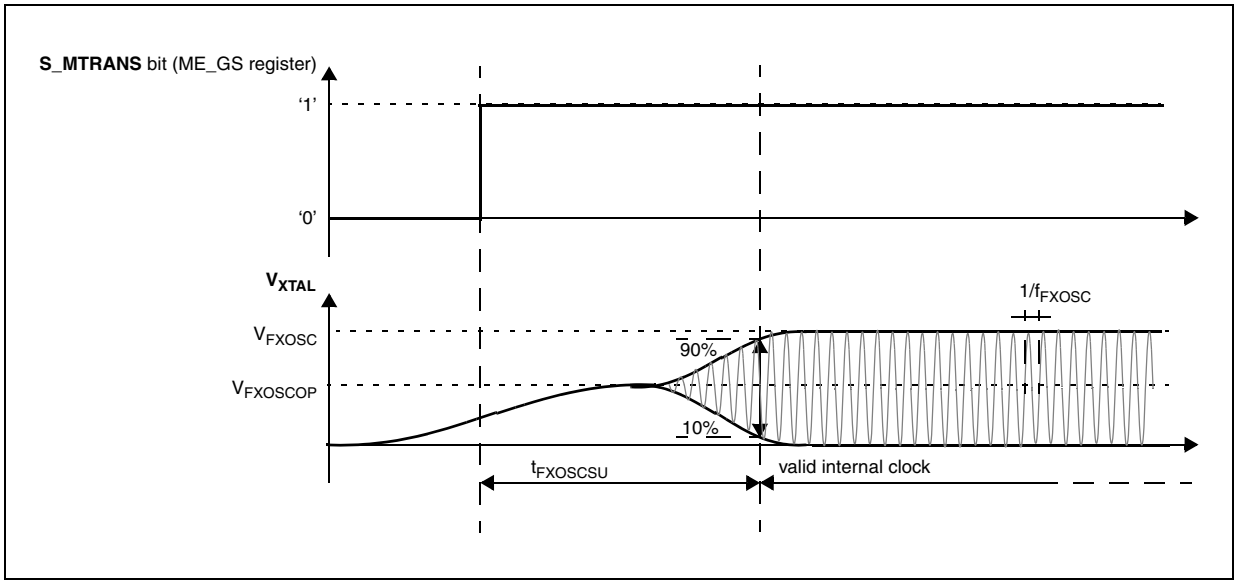


Figure 10. Fast external crystal oscillator (4–16 MHz) electrical characteristics

Table 31. Fast external crystal oscillator (4–16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
f_{FXOSC}	SR	T	Fast external crystal oscillator frequency			4.0	—	16.0	MHz
g_{mFXOSC}	CC	P	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, OSCILLATOR_MARGIN = 0		4.11	5.59	7.38	mA/V
		D		V_{DD} = 5.0 V ± 10%, OSCILLATOR_MARGIN = 0		3.67	5.04	6.73	
		D		V_{DD} = 3.3 V ± 10%, OSCILLATOR_MARGIN = 1		4.93	6.70	8.86	
		D		V_{DD} = 5.0 V ± 10%, OSCILLATOR_MARGIN = 1		4.54	6.22	8.31	
V_{FXOSC}	CC	T	Oscillation amplitude	f_{OSC} = 4 MHz, V_{DD} = 3.3 V ± 10%		2.51	—	—	V
		T		f_{OSC} = 16 MHz, V_{DD} = 3.3 V ± 10%		1.68	—	—	
		T		f_{OSC} = 4 MHz, V_{DD} = 5.0 V ± 10%		4.74	—	—	
		T		f_{OSC} = 16 MHz, V_{DD} = 5.0 V ± 10%		3.02	—	—	
$V_{FXOSCOP}$	CC	P	Oscillation operating point	V_{DD} = 3.3 V ± 10%	V_{EXTAL}	0.894	—	1.143	V
		P			V_{XTAL}	0.894	—	1.146	
		D		V_{DD} = 5.0 V ± 10%	V_{EXTAL}	0.904	—	1.166	
		D			V_{XTAL}	0.904	—	1.169	

Table 31. Fast external crystal oscillator (4–16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
I_{FXOSC}	CC	D	Fast external crystal oscillator consumption	f_{OSC} = 4 MHz	—	—	2.43	mA
		D		f_{OSC} = 16 MHz	—	—	2.52	
$t_{FXOSCSU}$	CC	C	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6.0	ms
		C		f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	D	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	$0.65V_{DD}$		V_{DD} + 0.4	V
V_{IL}	SR	D	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4		$0.35V_{DD}$	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3.12 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

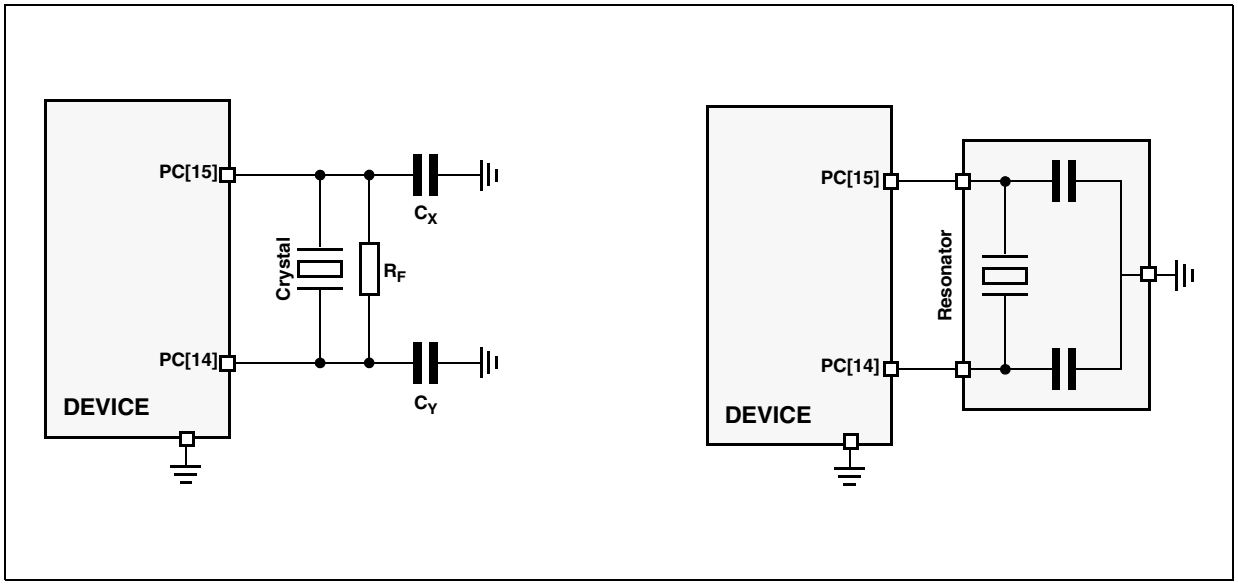


Figure 11. Crystal Oscillator and Resonator Connection Scheme

NOTE

PC[14]/PC[15] must not be directly used to drive external circuits.

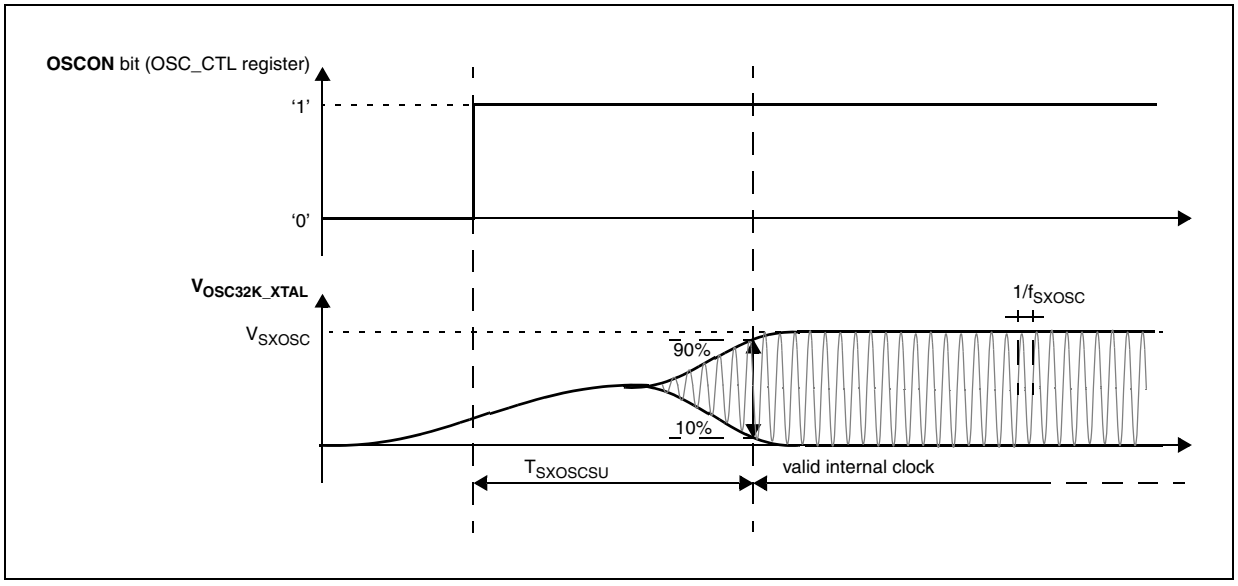


Figure 12. Slow external crystal oscillator (32 kHz) electrical characteristics

Table 32. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	T	Slow external crystal oscillator frequency		32	—	40	kHz
V_{SXOSC}	CC[3]	T	Oscillation amplitude	V_{DD} = 3.3 V ± 10%	1.12	1.33	1.74	V
		T		V_{DD} = 5.0 V ± 10%	1.12	1.37	1.74	
I_{SXOSC}	CC[3]	D	Slow external crystal oscillator consumption				5	µA
$T_{SXOSCSU}$	CC[3]	T	Slow external crystal oscillator start-up time				2	s
V_{IH}	SR	D	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	$0.65V_{DD}$		V_{DD} + 0.4	V
V_{IL}	SR	D	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4		$0.35V_{DD}$	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Granted by device validation

3.13 FMPLL Electrical Characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 33. FMPLL Electrical Characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	T	FMPLL reference clock[3]		4		64	MHz
Δ_{PLLIN}	SR	T	FMPLL reference clock duty cycle[3]		40		60	%
f_{PLLOUT}	CC	T	FMPLL output clock frequency		16		64	MHz
f_{CPU}	CC	T	System clock frequency				64[4]	MHz
t_{LOCK}	CC	T	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)			200	µs
Δt_{PKJIT}	CC	T	FMPLL jitter (peak to peak)	f_{PLLIN} = 16 MHz (resonator)			500	ps
Δt_{LTJIT}	CC	T	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator)			1.5	ns
I_{PLL}	CC[5]	D	FMPLL consumption	T_A = 25 °C			4	mA

1 V_{DDPLL} = 1.2 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

4 f_{CPU} 64 MHz can be achieved only at up to 105 °C

5 Data based on characterization results, not tested in production

3.14 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 34. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed		-2%	16	+2%	MHz
$\Delta_{FIRCVAR}$	CC[3]	P	Fast internal RC oscillator variation in temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	T_A = 25 °C		–5		+5	%
$I_{FIRCRUN}$	CC	D	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed				200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C				10	µA

Table 34. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{FIRCSTOP}$	CC	D	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off		0.3		mA
		D			sysclk = 2 MHz		2		
		D			sysclk = 4 MHz		2.5		
		D			sysclk = 8 MHz		3.3		
		D			sysclk = 16 MHz		5.2		
t_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	T_A = 25 °C	V_{DD} = 5.0 V ± 10%				µs
		C			V_{DD} = 3.3 V ± 10%				
		C		T_A = -40 to 105 °C	V_{DD} = 5.0 V ± 10%				
		C			V_{DD} = 3.3 V ± 10%				

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 Guaranteed by device characterization, not tested in production

3.15 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 35. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	-2%	128	+2%	kHz
$\Delta_{SIRCVAR}$	CC	P	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 25 °C in high frequency configuration		-10%	128	+10%	kHz
I_{SIRC}	CC	D	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed			5	µA
t_{SIRCSU}	CC	C	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%				µs

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3.16 Flash Memory Electrical Characteristics

Table 36. Program and Erase Specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	P	Double Word (64 bits) program time[4]		—	22	500	µs
$T_{16kpperase}$	CC	P	16 KB block pre-program and erase time		—	500	5000	ms
$T_{32kpperase}$	CC	P	32 KB block pre-program and erase time		—	600	5000	ms
$T_{128kpperase}$	CC	P	128 KB block pre-program and erase time		—	1300	7500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 37. Flash Module Life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T_J)	—	10,000	100,000[1]	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000[1]	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[2]	Blocks with 0–1,000 P/E cycles	20	—	years
				Blocks with 10,000 P/E cycles	10	—	years
				Blocks with 100,000 P/E cycles	1–5[1]	—	years

1 To be confirmed

2 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

3.17 Analog to Digital Converter (ADC) Electrical Characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog to Digital Converter.

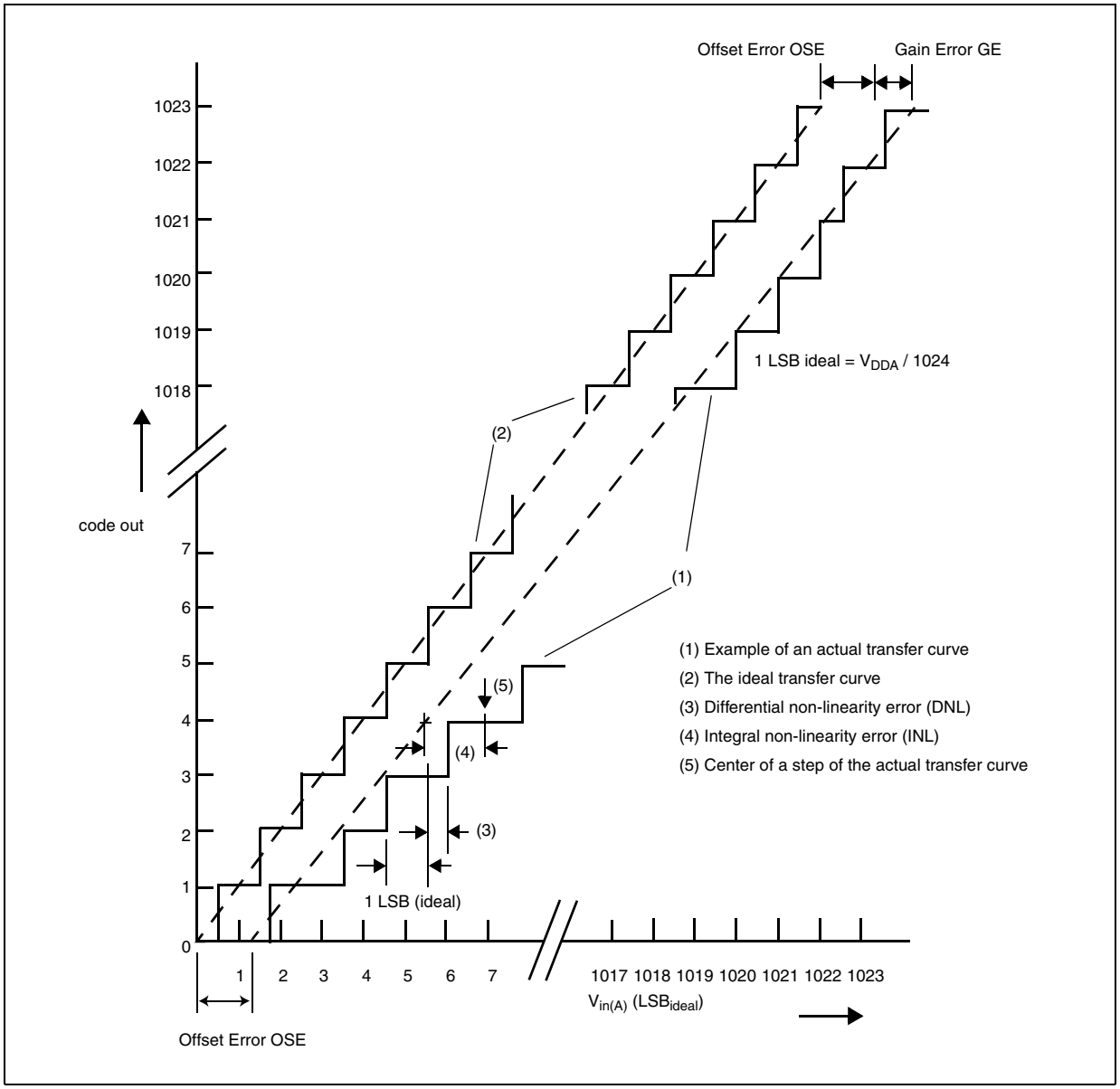


Figure 13. ADC Characteristics and Error Definitions

3.17.1 Input Impedance and ADC Accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330k Ω is obtained ($R_{EQ} = 1 / (f_c \times C_S)$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 5:

Eqn. 5

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 5 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

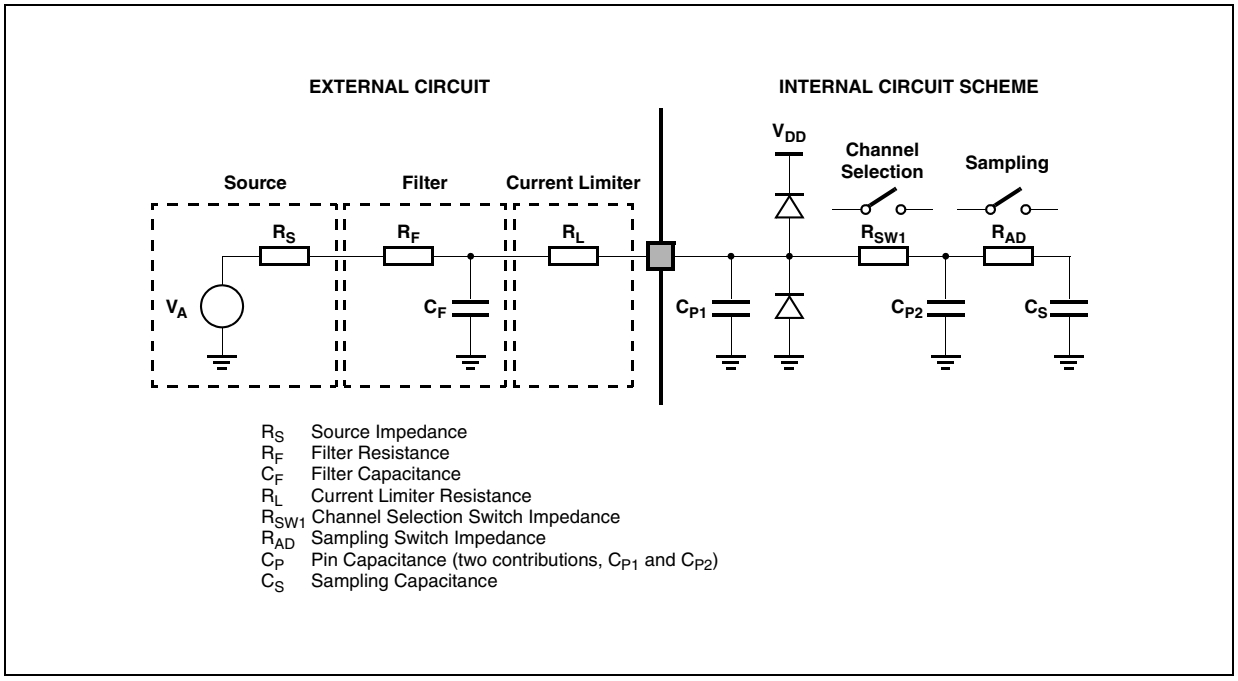


Figure 14. Input Equivalent Circuit (Precise Channels)

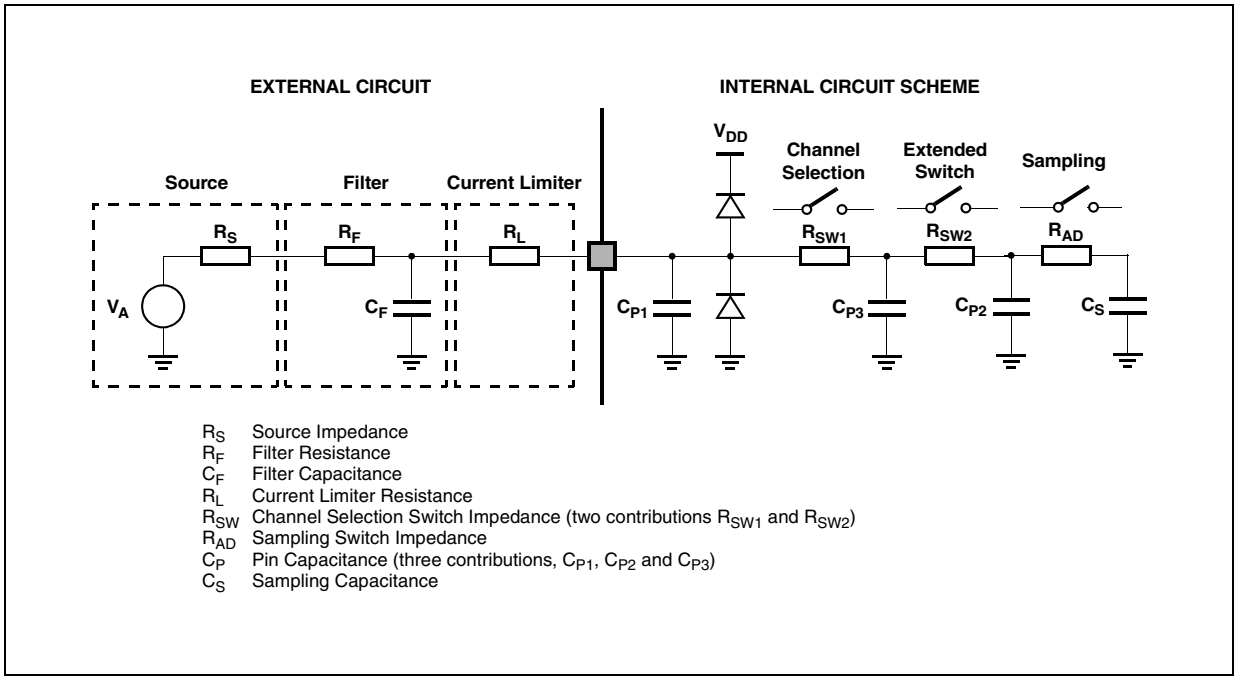


Figure 15. Input Equivalent Circuit (Extended Channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 14): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

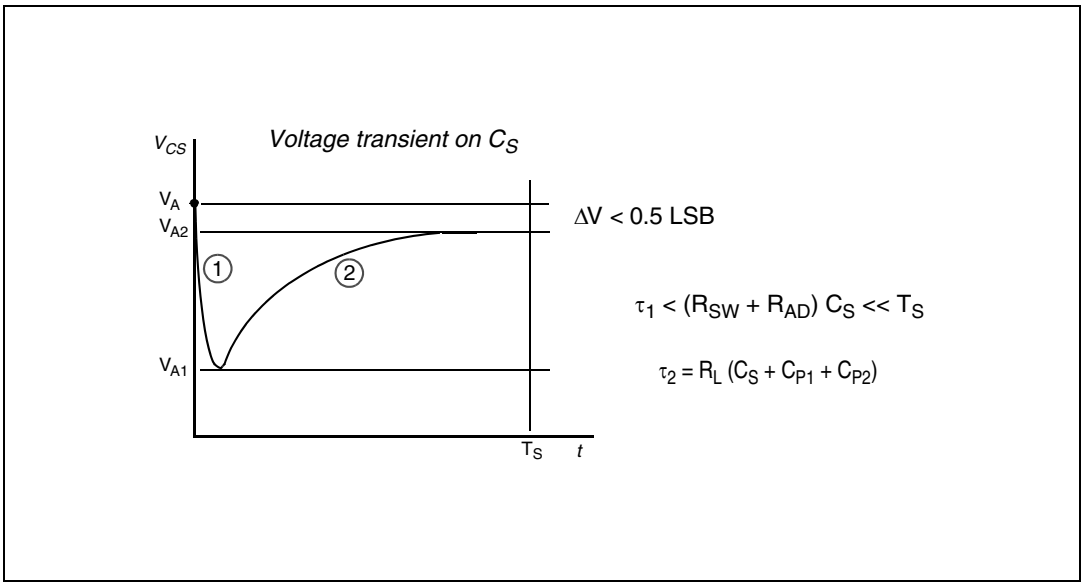


Figure 16. Transient Behavior during Sampling Phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 6

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 6 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 7

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 8:

Eqn. 8

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 9

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 10

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 11 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 11

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

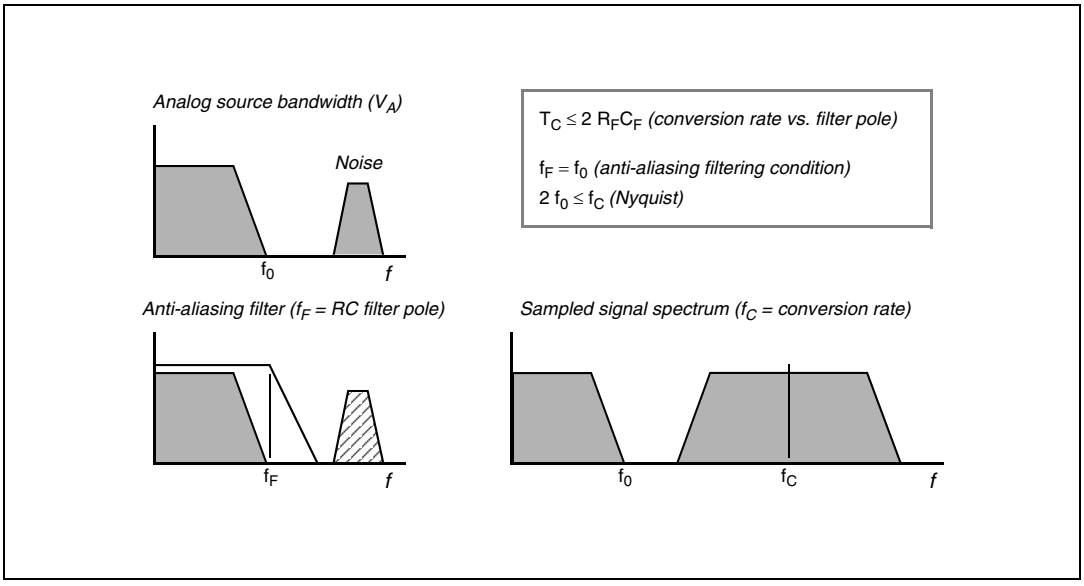


Figure 17. Spectral Representation of Input Signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 12 between the ideal and real sampled voltage on C_S:

Eqn. 12

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 13

$$C_F > 2048 \bullet C_S$$

3.17.2 ADC Electrical Characteristics

NOTE

For input leakage current specification see Table 23 on on page 55.

Table 38. ADC Conversion Characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{SSA}	SR	D	Voltage on VSSA (ADC reference) pin with respect to ground (V_{SS})[3]		–0.1		0.1	V
V_{DDA}	SR	D	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})		V_{DD} – 0.1		V_{DD} + 0.1	V
V_{AINx}	SR	D	Analog input voltage[4]		V_{SSA} – 0.1		V_{DDA} + 0.1	V
f_{ADC}	SR	D	ADC analog frequency		6		32	MHz
t_{ADC_PU}	SR	D	ADC power up delay				1.5	µs
t_{ADC_S}	CC	T	Sample time[5,6]	f_{ADC} = 32 MHz, ADC_conf_sample_input = 17	0.5			µs
		T		f_{ADC} = 6 MHz, ADC_conf_sample_input = 127			21	
t_{ADC_C}	CC	T	Conversion time[7]	f_{ADC} = 32 MHz, ADC_conf_comp = 2	0.625			µs
C_S	CC	D	ADC input sampling capacitance				3	pF
C_{P1}	CC	D	ADC input pin capacitance 1				3	pF
C_{P2}	CC	D	ADC input pin capacitance 2				1	pF
C_{P3}	CC	D	ADC input pin capacitance 3				1	pF
R_{SW1}	CC	D	Internal resistance of analog source				3	kΩ
R_{SW2}	CC	D	Internal resistance of analog source				2	kΩ
R_{AD}	CC	D	Internal resistance of analog source				0.1	kΩ
I_{INJ}	SR	T	Input current Injection	Current injection on one ADC input, different from the converted one	–10		10	mA
INL	CC	P	Integral Non Linearity	No overload	–1.5		1.5	LSB
DNL	CC	P	Differential Non Linearity	No overload	–1.0		1.0	LSB
OFS	CC	T	Offset error	After offset cancellation		0.5		LSB
GNE	CC	T	Gain error			0.6		LSB

Table 38. ADC Conversion Characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
TUEp	CC	P	Total unadjusted error[8] for precise channels	Without current injection	-2	0.6	2	LSB
		T		With current injection	-3		3	
TUEx	CC	T	Total unadjusted error[8] for extended channel	Without current injection	-3		3	LSB
		T		With current injection	-4		4	

1 V_{DDA} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 Analog and digital V_{SS} **must** be common (to be tied together externally).

4 V_{AINx} may exceed V_{SSA} and V_{DDA} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF

5 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

6 The maximum sample rate is 1million samples per second, provided the source impedance and current limiter(>1Kohms) are calculated adequately.

- Filter capacitor at analog source output must meet the criteria Cf (filter capacitor) > 2048*Cs (sampling capacitor which is 3 pF)

7 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

8 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

3.18 Pad AC Specifications

Table 39. Pad AC specifications (5.0 V, PAD3V5V = 1)[1]

No.	Pad	Tswitchon[1,2] (ns)			Rise/Fall[2,3] (ns)			Frequency[2] (MHz)			Current slew[2] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	1.5	—	30	6	—	50	—	—	4	0.04	—	2	25
		1.5	—	30	9	—	100	—	—	2	0.04	—	2	50
		1.5	—	30	12	—	125	—	—	2	0.04	—	2	100
		1.5	—	30	16	—	150	—	—	2	0.04	—	2	200
2	Medium	1	—	15	3	—	10	—	—	40	2.5	—	7	25
		1	—	15	5	—	20	—	—	20	2.5	—	7	50
		1	—	15	9	—	40	—	—	13	2.5	—	8	100
		1	—	15	12	—	70	—	—	7	2.5	—	8	200

Table 39. Pad AC specifications (5.0 V, PAD3V5V = 1)[1] (continued)

No.	Pad	Tswitchon[1,2] (ns)			Rise/Fall[2,3] (ns)			Frequency[2] (MHz)			Current slew[2] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	1	—	6	1	—	4	—	—	100	18	—	55	25
		1	—	6	1.5	—	6	—	—	80	18	—	55	50
		1	—	6	3	—	12	—	—	40	18	—	55	100
		1	—	6	5	—	16	—	—	25	18	—	55	200
4	Symmetric	1	—	5	1	—	4	—	—	50	10	—	25	25
5	Pull Up/Down (5.5 V max)	—	—	—	—	—	5000	—	—	—	—	—	—	50

1 Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition

2 Data based on characterization results, not tested in production

3 Slope at rising/falling edge

Table 40. Pad AC specifications (3.3 V, PAD3V5V = 0)[1]

No.	Pad	Tswitchon[1,3] (ns)			Rise/Fall[2,3] (ns)			Frequency[3] (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	3	—	40	50
		1	—	6	3	—	12	—	—	40	3	—	40	100
		1	—	6	5	—	18	—	—	25	3	—	40	200
4	Symmetric	1	—	6	2	—	6	—	—	50	3	—	25	25
5	Pull Up/Down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50

1 Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition

2 Slope at rising/falling edge

3 Data based on characterization results, not tested in production

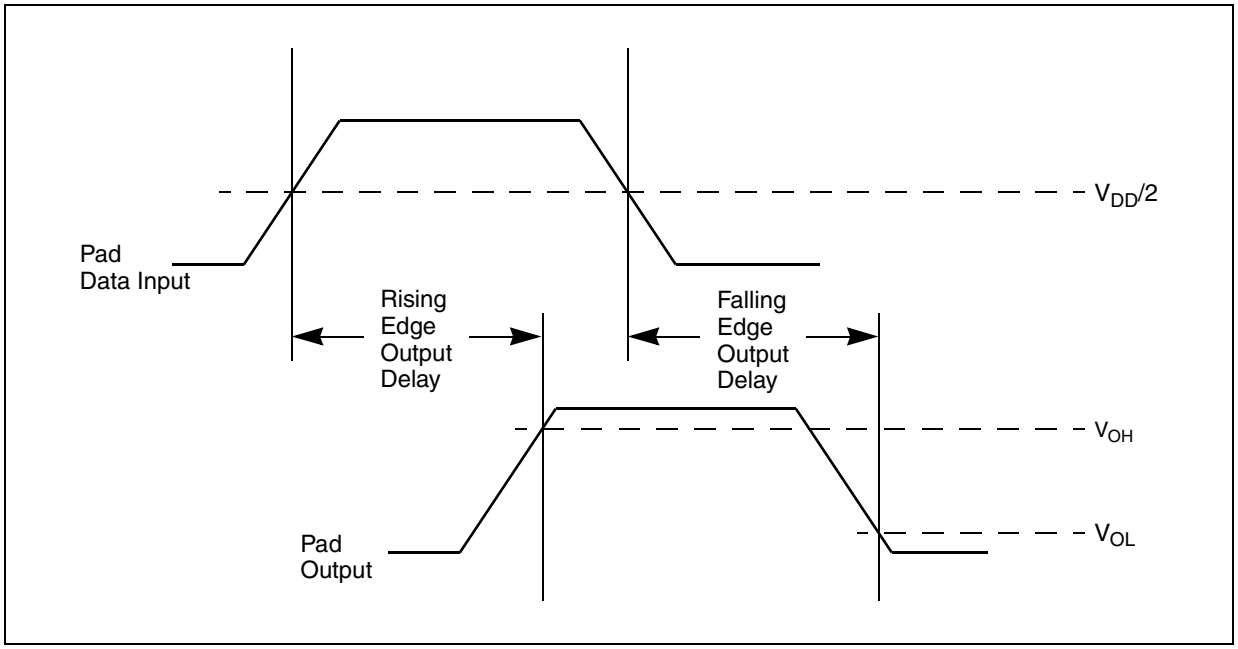


Figure 18. Pad Output Delay

3.19 AC Timing

3.19.1 IEEE 1149.1 Interface Timing

Table 41. JTAG Interface Timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width (measured at $V_{DD}/2$)	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	35	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	30	ns
9	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	35	ns
10	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	50	ns
11	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	50	ns
12	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	50	—	ns
13	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at V_{DD} = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b11.

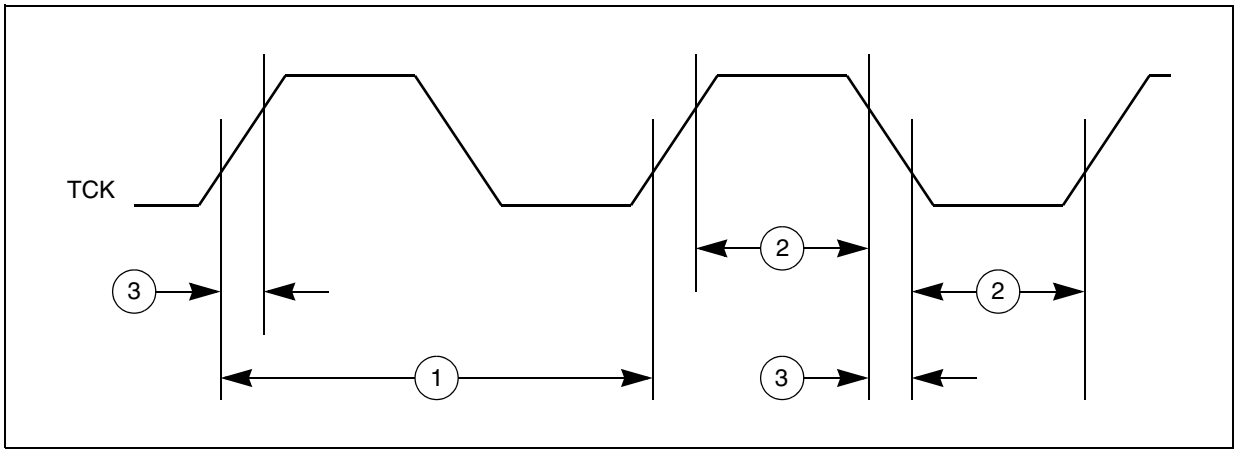


Figure 19. JTAG Test Clock Input Timing

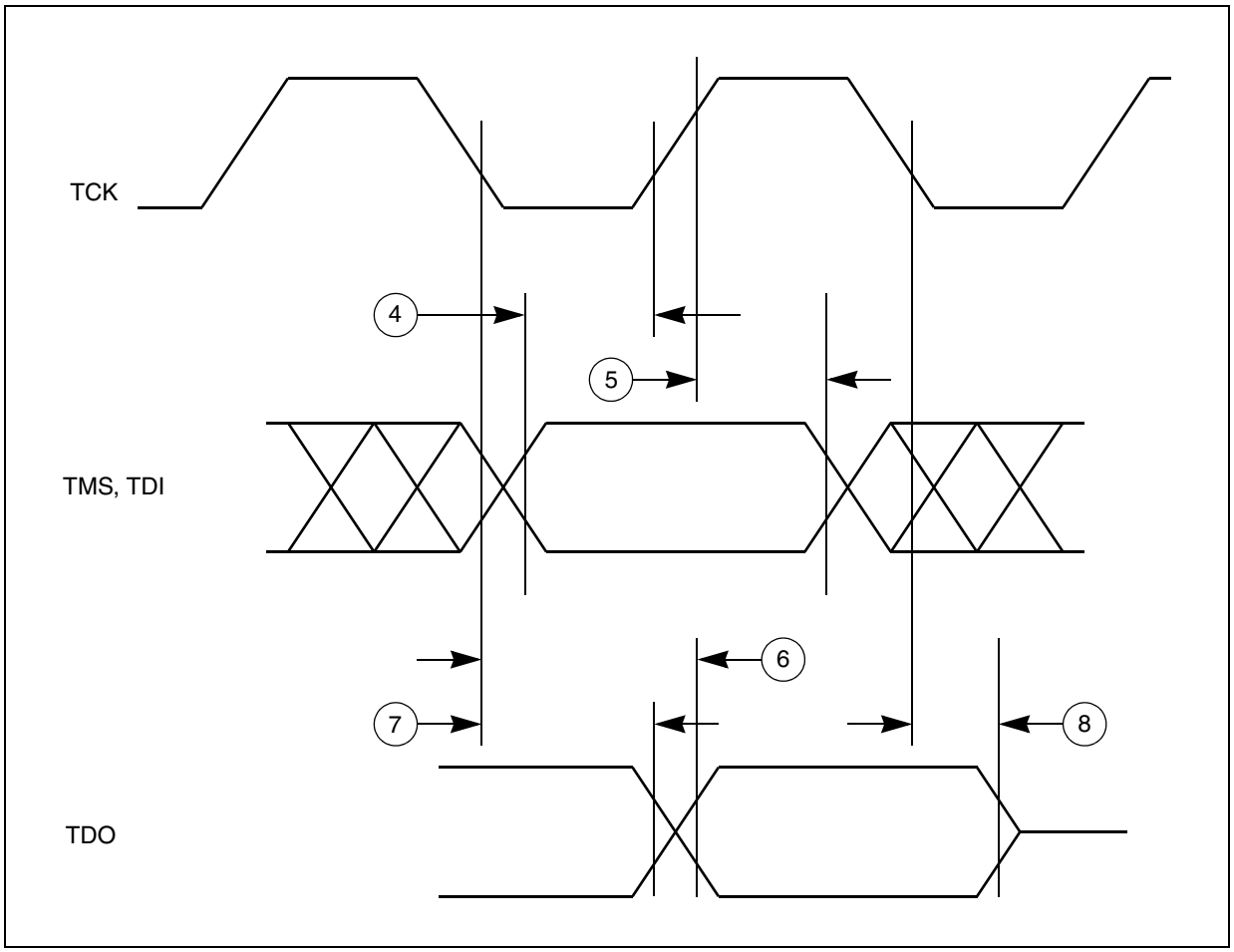


Figure 20. JTAG Test Access Port Timing

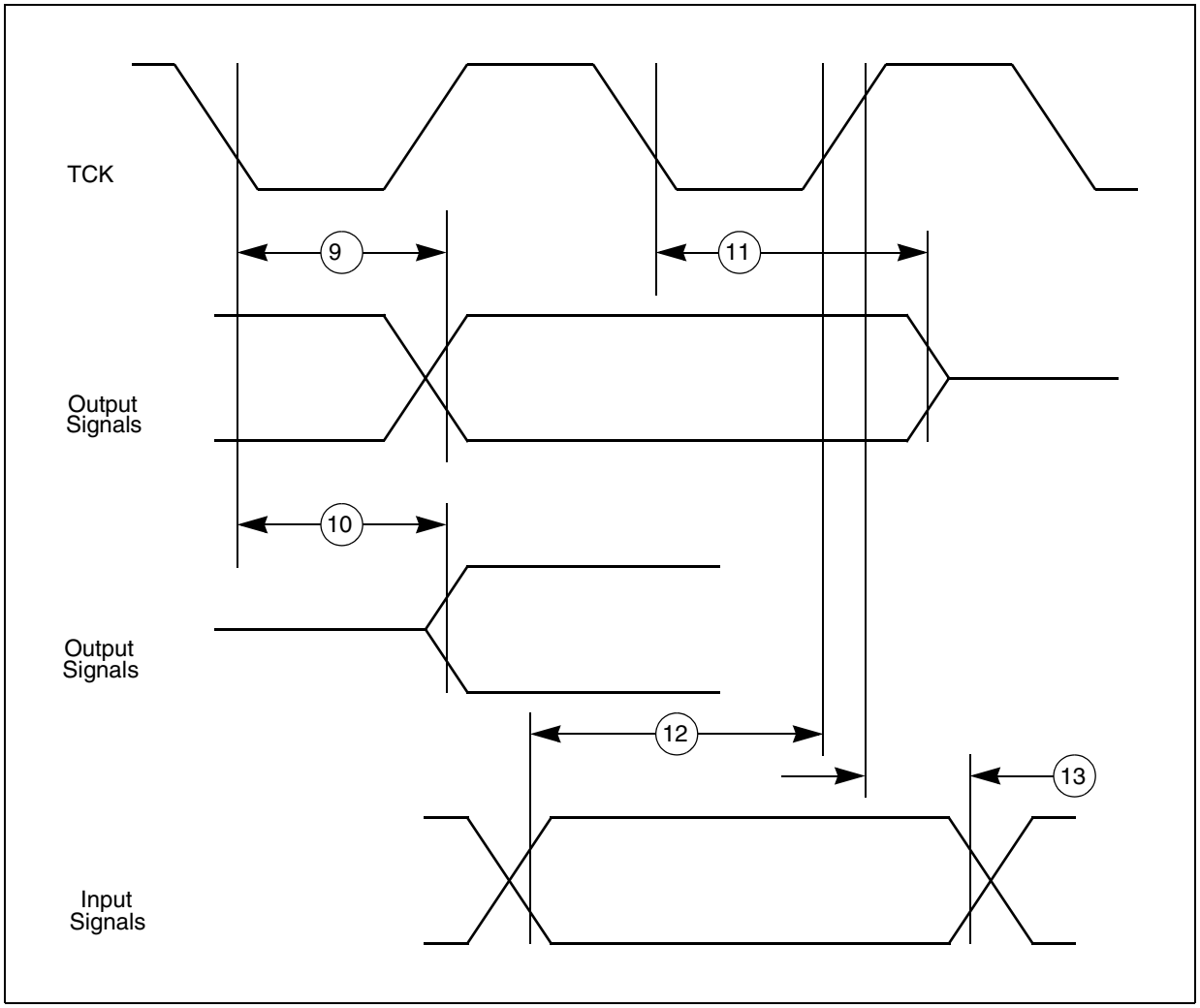


Figure 21. JTAG Boundary Scan Timing

3.19.2 Nexus Debug Interface

Table 42. Nexus Debug Port Timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{MCYC}	CC	D	MCKO Cycle Time	22	—	ns
2	Δ_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid[2]	–2	14	ns
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	–2	14	ns
5	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	–2	14	ns
6	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4	—	t_{TCYC}
7	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ Pulse Width	1	—	t_{MCYC}
8	t_{TCYC}	CC	D	TCK Cycle Time[3]	100	—	ns
9	Δ_{TDC}	CC	D	TCK Duty Cycle	40	60	%
10	t_{NTDIS}, t_{NTMSS}	CC	D	TDI, TMS Data Setup Time	25	—	ns
11	t_{NTDIH}, t_{NTMSH}	CC	D	TDI, TMS Data Hold Time	5	—	ns
12	t_{JOV}	CC	D	TCK Low to TDO Data Valid	0	35	ns

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 3.0 V to 5.5V, T_A = –40 to 105 °C, and C_L = 50 pF (C_L = 30 pF on MCKO), with SRC = 0b11.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3 The system clock frequency needs to be three times faster than the TCK frequency.

Figure 22. Nexus Clock Timing

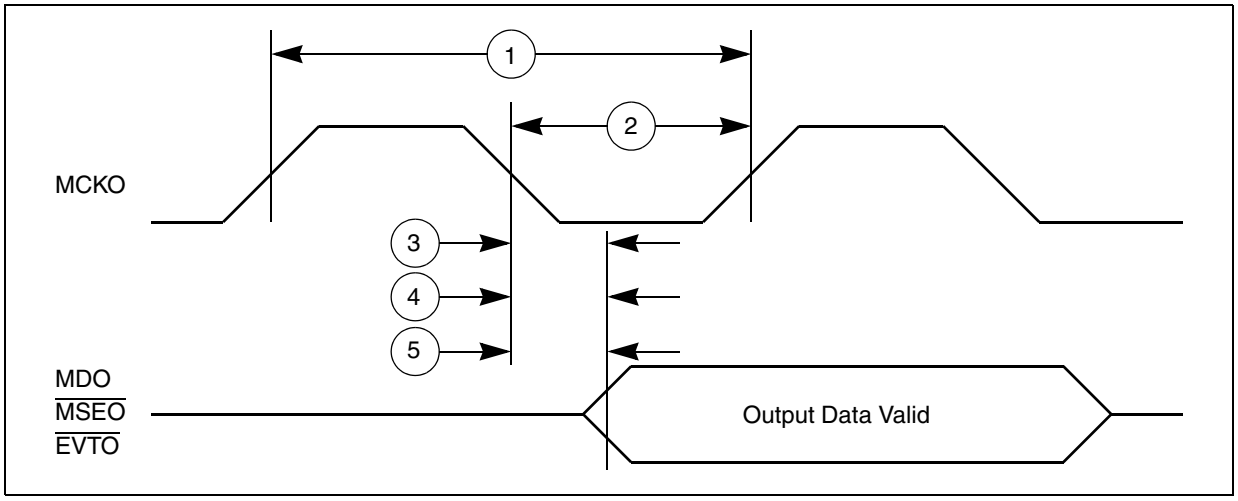


Figure 23. Nexus Output Timing

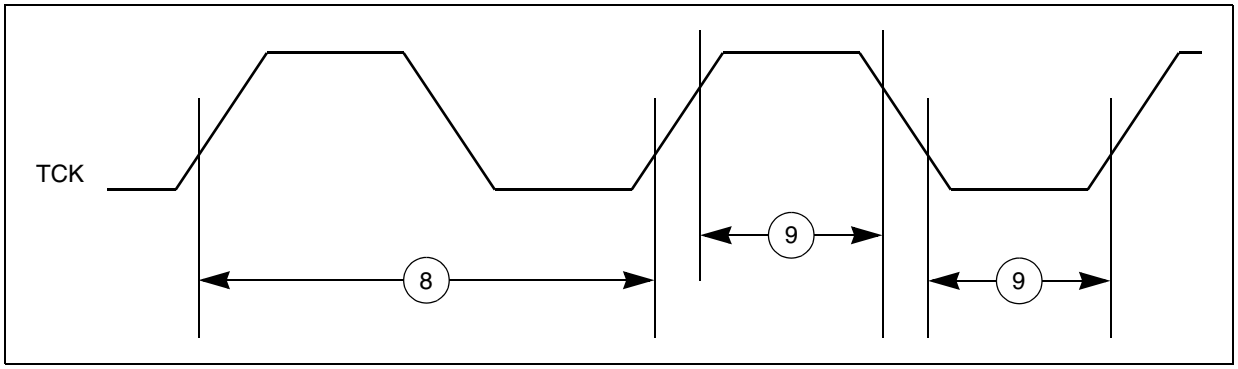


Figure 24. Nexus TCK Timing

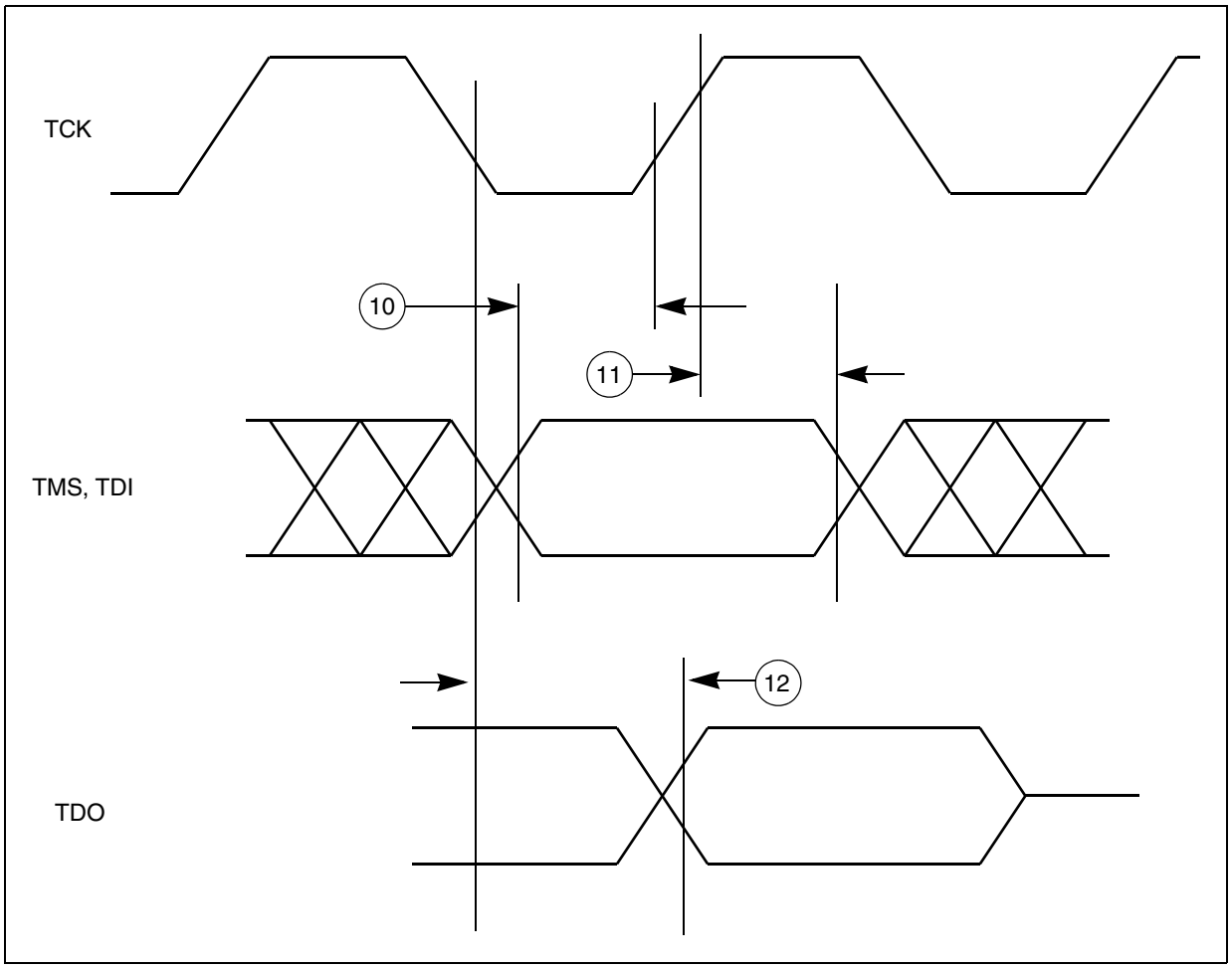


Figure 25. Nexus TDI, TMS, TDO Timing

3.19.3 Interface to TFT LCD Panels

Figure 26 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

1. DCU_CLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, DCU_CLK runs continuously.

2. DCU_HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
3. DCU_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
4. DCU_DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

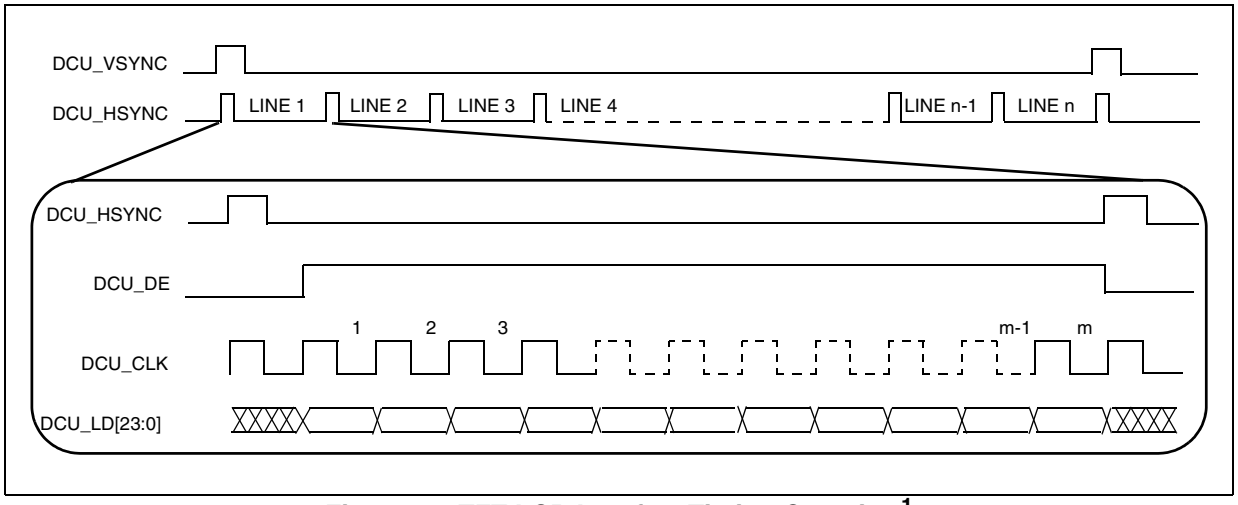


Figure 26. TFT LCD InterfaceTiming Overview[1]

3.19.3.1 Interface to TFT LCD Panels—Pixel Level Timings

Figure 27 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DCU_CLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the DCU_HSYNC, DCU_VSYNC and DCU_DE signals. The user can select the polarity of the DCU_HSYNC and DCU_VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DCU_DE signal is always active-high.

Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the DCU Clock Confide Register (DCCR) in the system clock module.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 43. LCD Interface Timing Parameters—Horizontal and Vertical

No.	Symbol		C	Parameter	Value	Unit
1	t_{PCP}	CC	D	Display pixel clock period	—	ns
2	t_{PWH}	CC	D	HSYNC pulse width	PW_H × t_{PCP}	ns
3	t_{BPH}	CC	D	HSYNC back porch width	BP_H × t_{PCP}	ns
4	t_{FPH}	CC	D	HSYNC front porch width	FP_H × t_{PCP}	ns
5	t_{SW}	CC	D	Screen width	DELTA_X × t_{PCP}	ns
6	t_{HSP}	CC	D	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) × t_{PCP}	ns
7	t_{PWV}	CC	D	VSYNC pulse width	PWV × t_{HSP}	ns

1. In Figure 26, the “DCU_LD[23:0]” signal is an aggregation of the DCU’s RGB signals—DCU_R[0:7], DCU_G[0:7] and DCU_B[0:7].

Table 43. LCD Interface Timing Parameters—Horizontal and Vertical (continued)

No.	Symbol		C	Parameter	Value	Unit
8	t_{BPV}	CC	D	VSYNC back porch width	BP_V × t_{HSP}	ns
	t_{FPV}	CC	D	VSYNC front porch width	FP_V × t_{HSP}	ns
	t_{SH}	CC	D	Screen height	DELTA_Y × t_{HSP}	ns
	t_{VSP}	CC	D	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) × t_{HSP}	ns

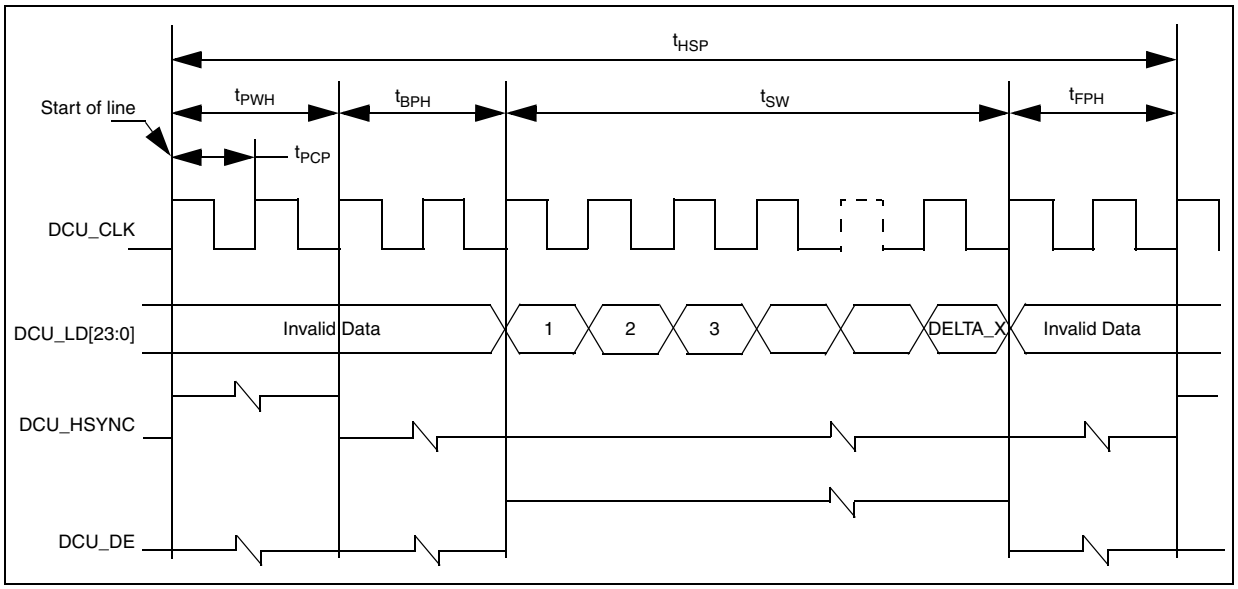


Figure 27. Horizontal Sync Timing

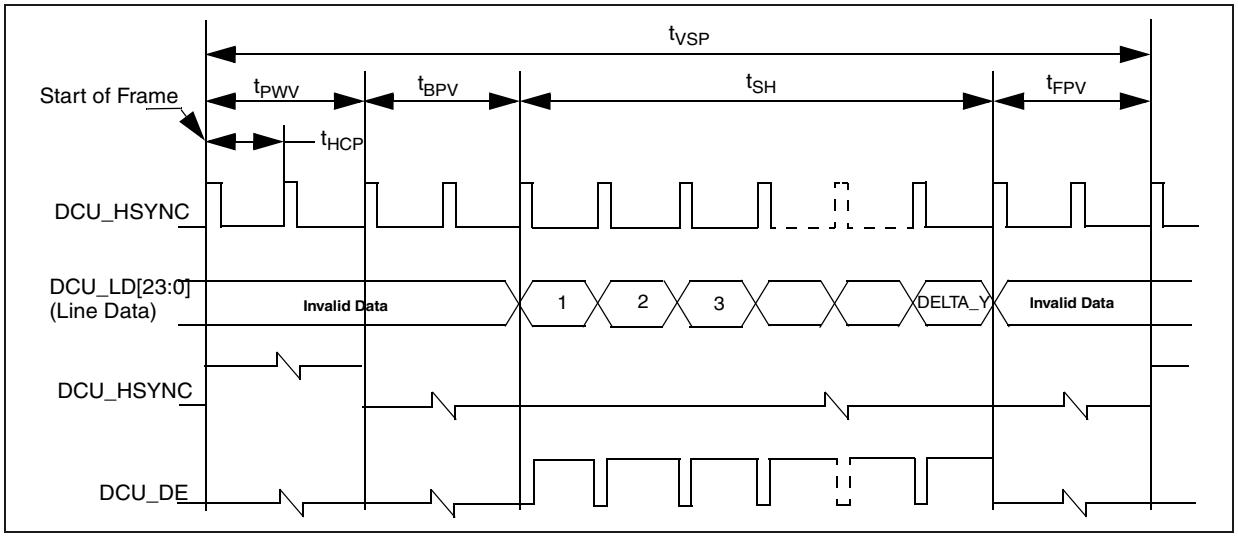


Figure 28. Vertical Sync Pulse

3.19.3.2 Interface to TFT LCD Panels—Access Level

Table 44. LCD Interface Timing Parameters[1,2,3,4]—Access Level

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{CKP}	CC	D	PDI clock period	31.25	—		ns
2	Δ_{CK}	CC	D	PDI clock duty cycle	40	—	60	%
3	t_{DSU}	CC	D	PDI data setup time	6	—		ns
4	t_{DHD}	CC	D	PDI data access hold time	1	—		ns
5	t_{CSU}	CC	D	PDI control signal setup time	3	—		ns
6	t_{CHD}	CC	D	PDI control signal hold time	1	—		ns
7		CC	D	TFT interface data valid after pixel clock		—	6	ns
8		CC	D	TFT interface HSYNC valid after pixel clock		—	5	ns
9		CC	D	TFT interface VSYNC valid after pixel clock		—	5.5	ns
10		CC	D	TFT interface DE valid after pixel clock		—	5.6	ns
11		CC	D	TFT interface hold time for data and control bits	2	—		ns
12		CC	D	Relative skew between the data bits		—	3.7	ns

1 The characteristics in this table are based on the assumption that data is output at +ve edge and displays latch data on –ve edge

2 Intra bit skew is less than 2 ns

3 Load C_L = 50 pF for frequency up to 20 MHz

4 Load C_L = 25 pF for display frequency from 20 to 32 MHz

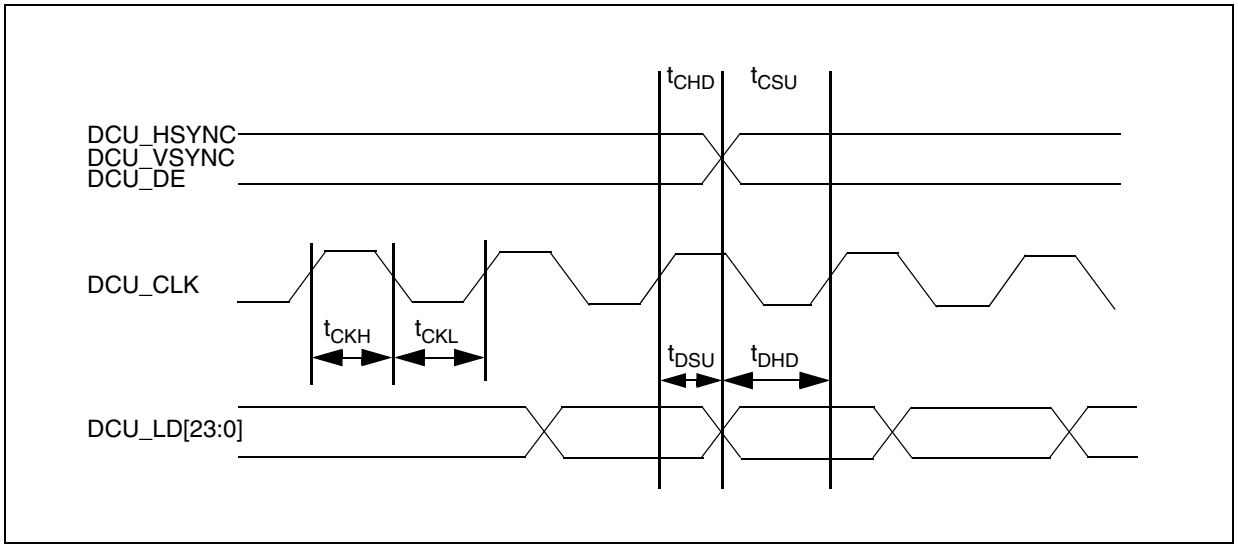


Figure 29. LCD Interface Timing Parameters—Access Level

3.19.4 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Timing

Table 45. IRQ and NMI Timing

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{IPWL}	CC	T	IRQ/NMI Pulse Width Low	200	—	ns
2	t_{IPWH}	CC	T	IRQ/NMI Pulse Width High	200	—	ns
3	t_{ICYC}	CC	T	IRQ/NMI Edge to Edge Time[1]	400	—	ns

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

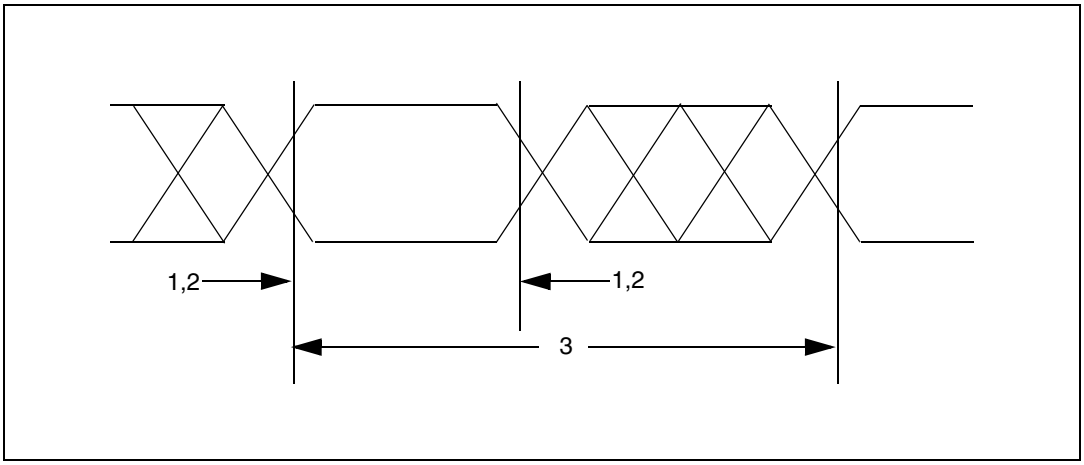


Figure 30. IRQ and NMI Timing

3.19.5 Enhanced Modular I/O Subsystem (eMIOS) Timing

Table 46. eMIOS Timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min[2]	Max	
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

[1] eMIOS timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00

[2] There is no limitation on the peripheral for setting the minimum pulse width, the actual width is restricted by the pad delays. Refer to the pad specification section for the details.

3.19.6 FlexCAN Timing

The CAN functions are available as TX pins at normal IO pads and as RX pins at the always on domain. There is no filter for the wakeup dominant pulse. Any high-to-low edge can cause wakeup if configured.

Table 47. FlexCAN Timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{CANOV}	CC	D	CTNX Output Valid after CLKOUT Rising Edge (Output Delay)	—	22.48	ns
2	t_{CANSU}	CC	D	CNRX Input Valid to CLKOUT Rising Edge (Setup Time)	—	12.46	ns

1 FlexCAN timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00.

3.19.7 Deserial Serial Peripheral Interface (DSPI)

Table 48. DSPI Timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{SCK}	CC	D	SCK Cycle TIme[2,3]	60	—	ns
2	t_{CSC}	CC	D	PCS to SCK Delay[4]	—	—	ns
3	t_{ASC}	CC	D	After SCK Delay[5]	20	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle	$t_{SCK}/2 – 2ns$	$t_{SCK/2 + 2ns}$	ns
5	t_A	CC	D	Slave Access Time (PCSx active to SOUT driven)	—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time (PCSx inactive to SOUT High-Z or invalid)	—	25	ns
7	t_{SUI}	CC	D	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	 35 5 5 35	 — — — —	 ns ns ns ns
8	t_{HI}	CC	D	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	 –4 10 26 –4	 — — — —	 ns ns ns ns
9	t_{SUO}	CC	D	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	 — — — —	 15 35 30 15	 ns ns ns ns
10	t_{HO}	CC	D	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	 –15 5.5 0 –15	 — — — —	 ns ns ns ns

1 DSPI timing specified at VDDE_x = 3.0 V to 5.5V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b11.

2 The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate.

3 The actual minimum SCK Cycle Time is limited by pad performance.

4 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK], program PSSCK = 2 and CSSCK = 2

5 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC]

6 This delay value is corresponding to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

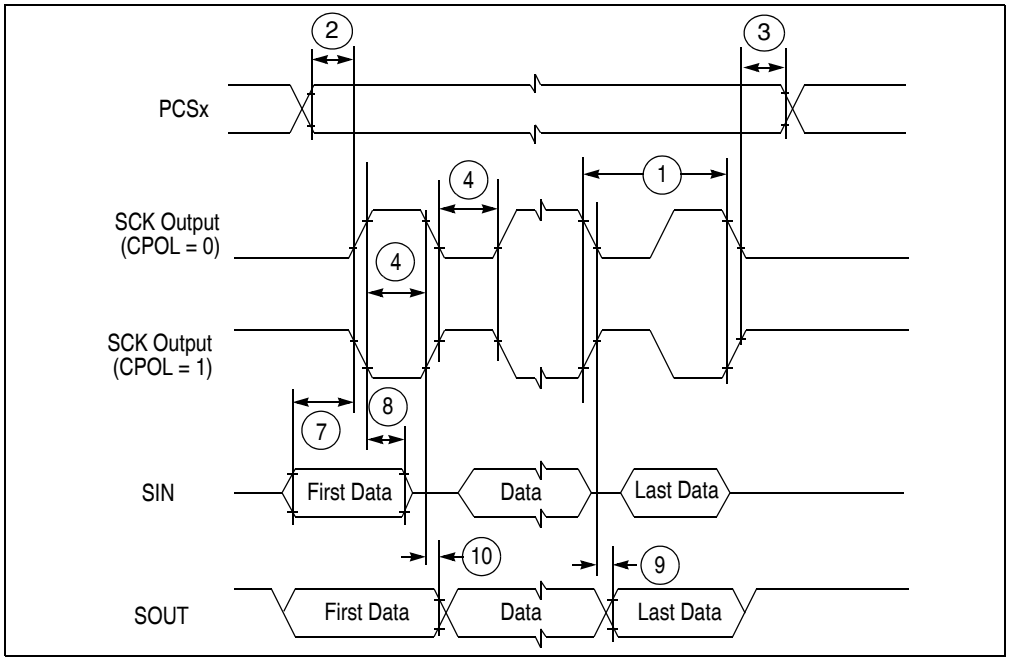


Figure 31. DSPI Classic SPI Timing — Master, CPHA = 0

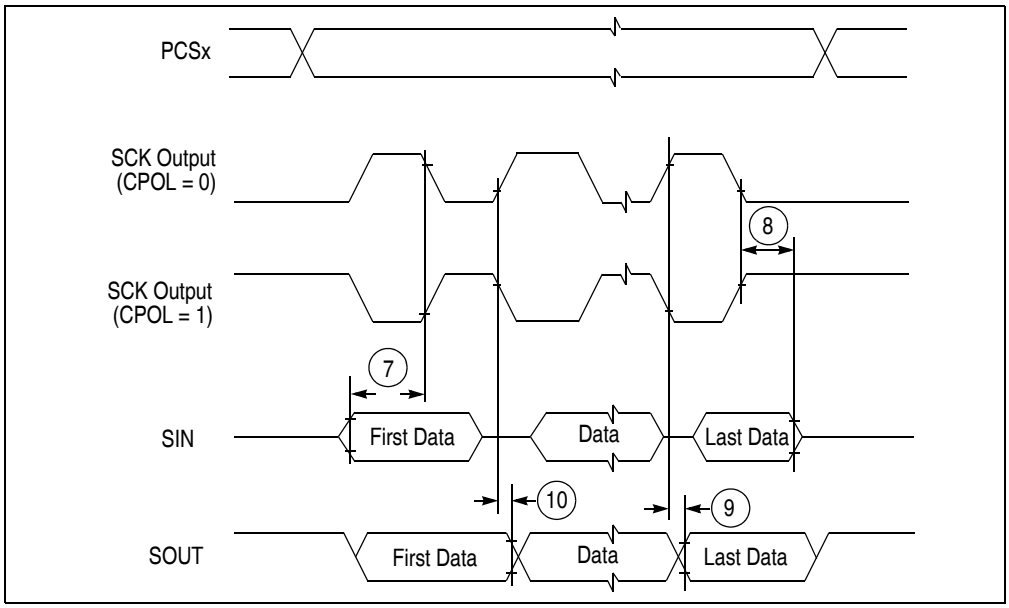


Figure 32. DSPI Classic SPI Timing — Master, CPHA = 1

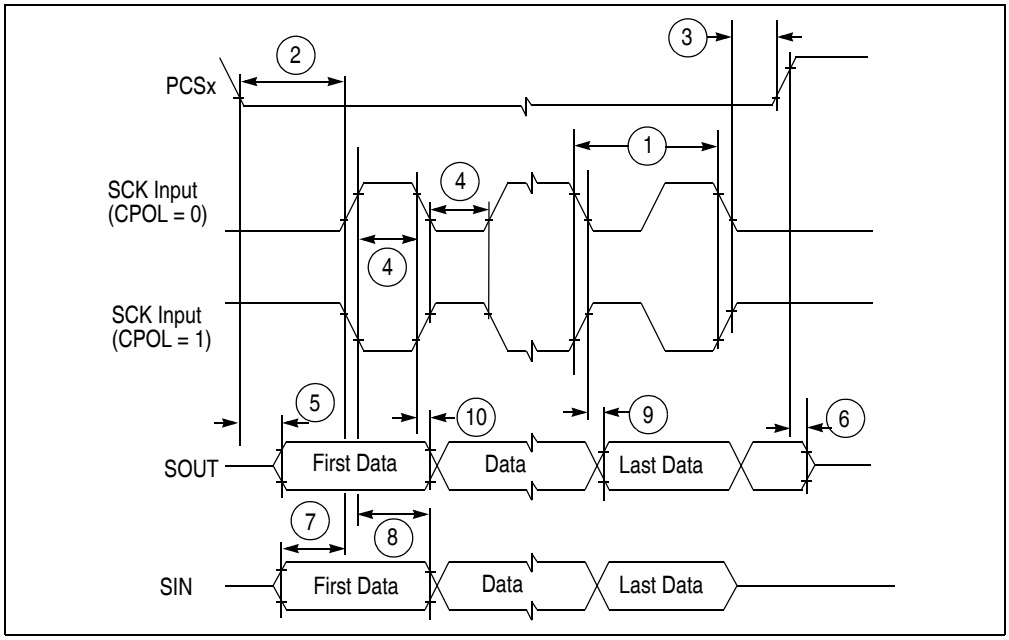


Figure 33. DSPI Classic SPI Timing — Slave, CPHA = 0

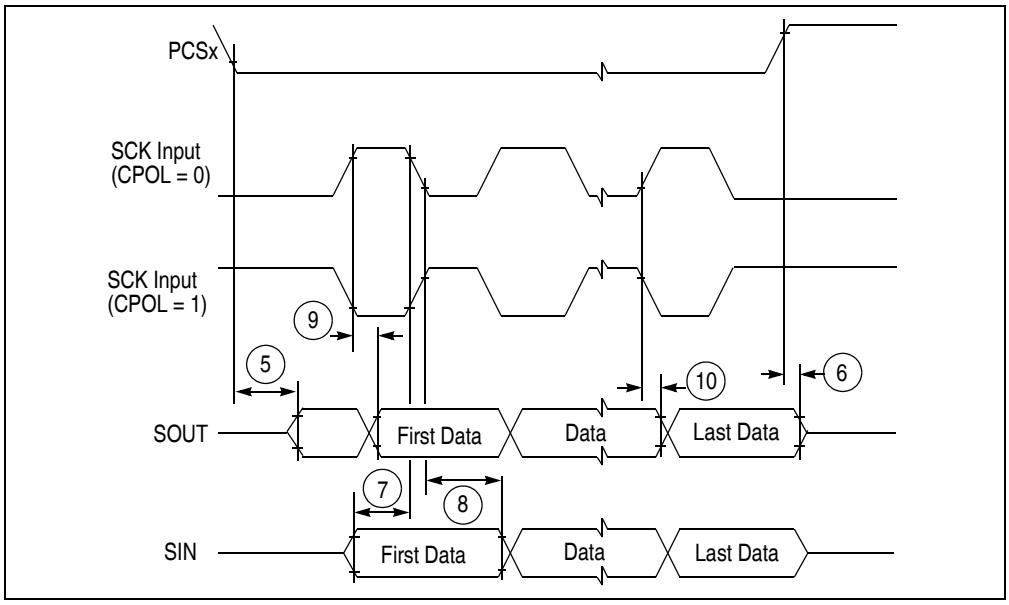


Figure 34. DSPI Classic SPI Timing — Slave, CPHA = 1

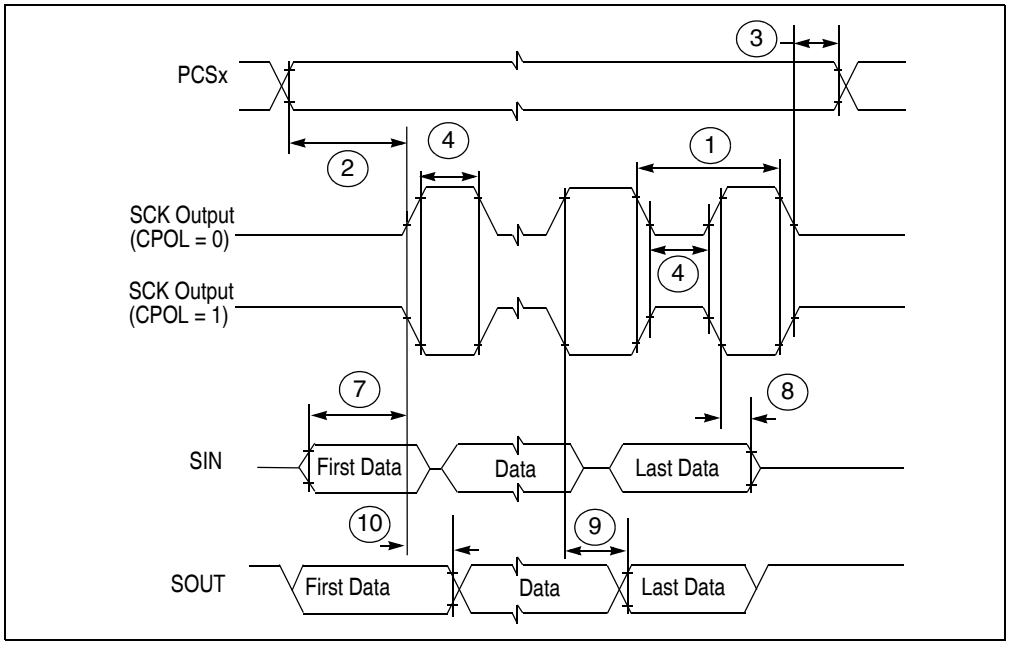


Figure 35. DSPI Modified Transfer Format Timing — Master, CPHA = 0

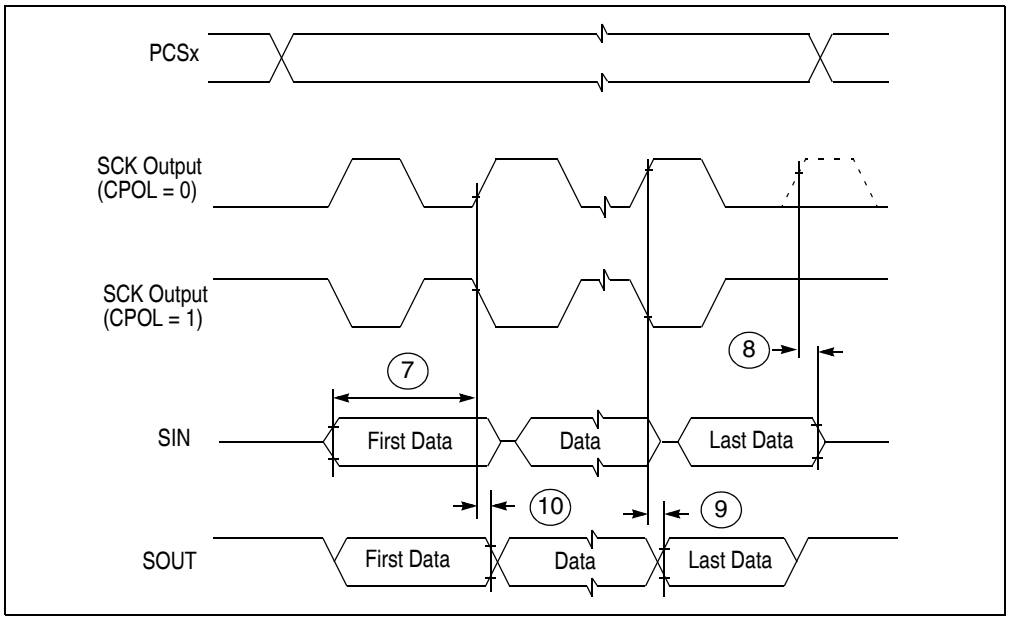


Figure 36. DSPI Modified Transfer Format Timing — Master, CPHA = 1

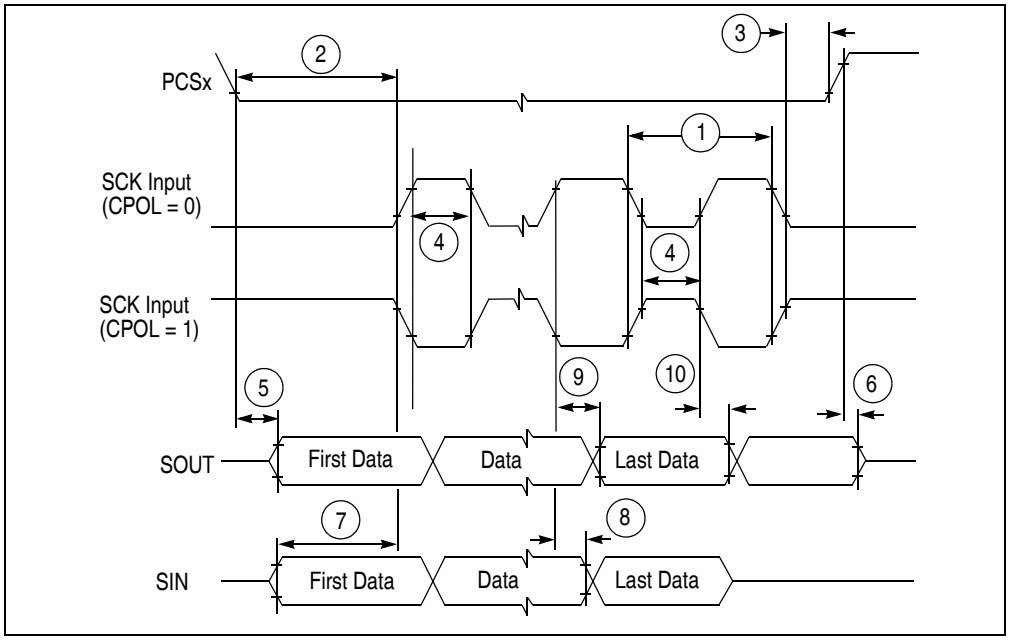


Figure 37. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

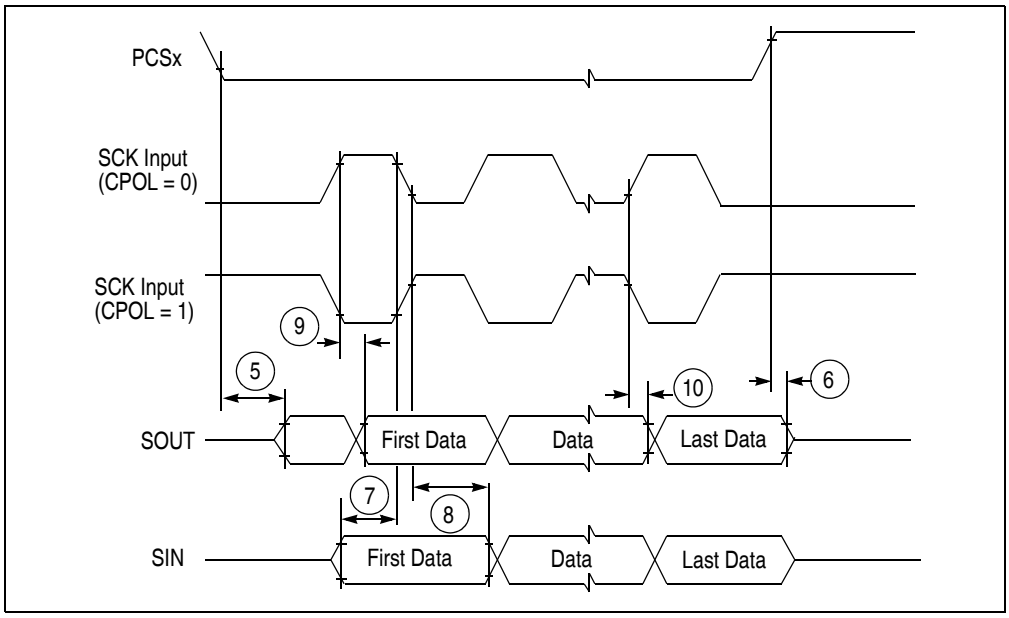


Figure 38. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

3.19.8 I²C Timing

Table 49. I²C Input Timing Specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	IP-Bus Cycle[1]
2	—	CC	D	Clock low time	8	—	IP-Bus Cycle[1]
4	—	CC	D	Data hold time	0.0	—	ns
6	—	CC	D	Clock high time	4	—	IP-Bus Cycle[1]
7	—	CC	D	Data setup time	0.0	—	ns
8	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]
9	—	CC	D	Stop condition setup time	2	—	IP-Bus Cycle[1]

1 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device

Table 50. I²C Output Timing Specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1[1]	—	CC	D	Start condition hold time	6	—	IP-Bus Cycle[2]
2[1]	—	CC	D	Clock low time	10	—	IP-Bus Cycle[1]
3[3]	—	CC	D	SCL/SDA rise time	—	99.6	ns
4[1]	—	CC	D	Data hold time	7	—	IP-Bus Cycle[1]
5[1]	—	CC	D	SCL/SDA fall time	—	99.5	ns
6[1]	—	CC	D	Clock high time	10	—	IP-Bus Cycle[1]
7[1]	—	CC	D	Data setup time	2	—	IP-Bus Cycle[1]
8[1]	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[1]
9[1]	—	CC	D	Stop condition setup time	10	—	IP-Bus Cycle[1]

1 Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device

3 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

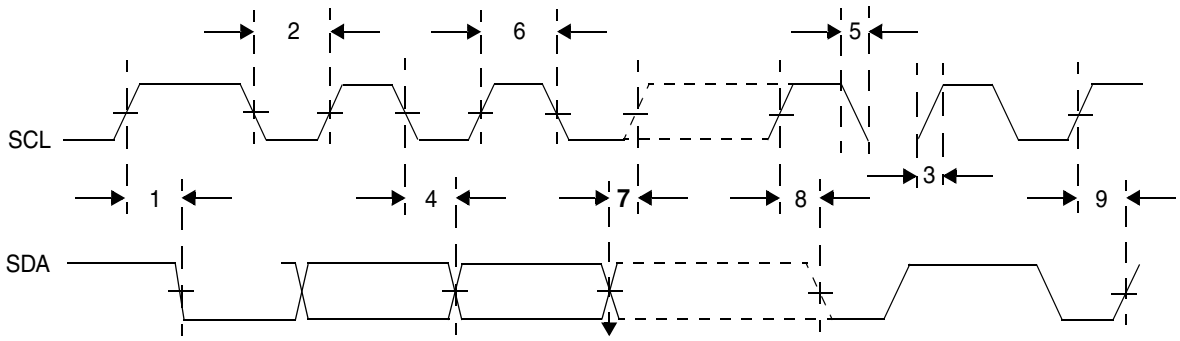
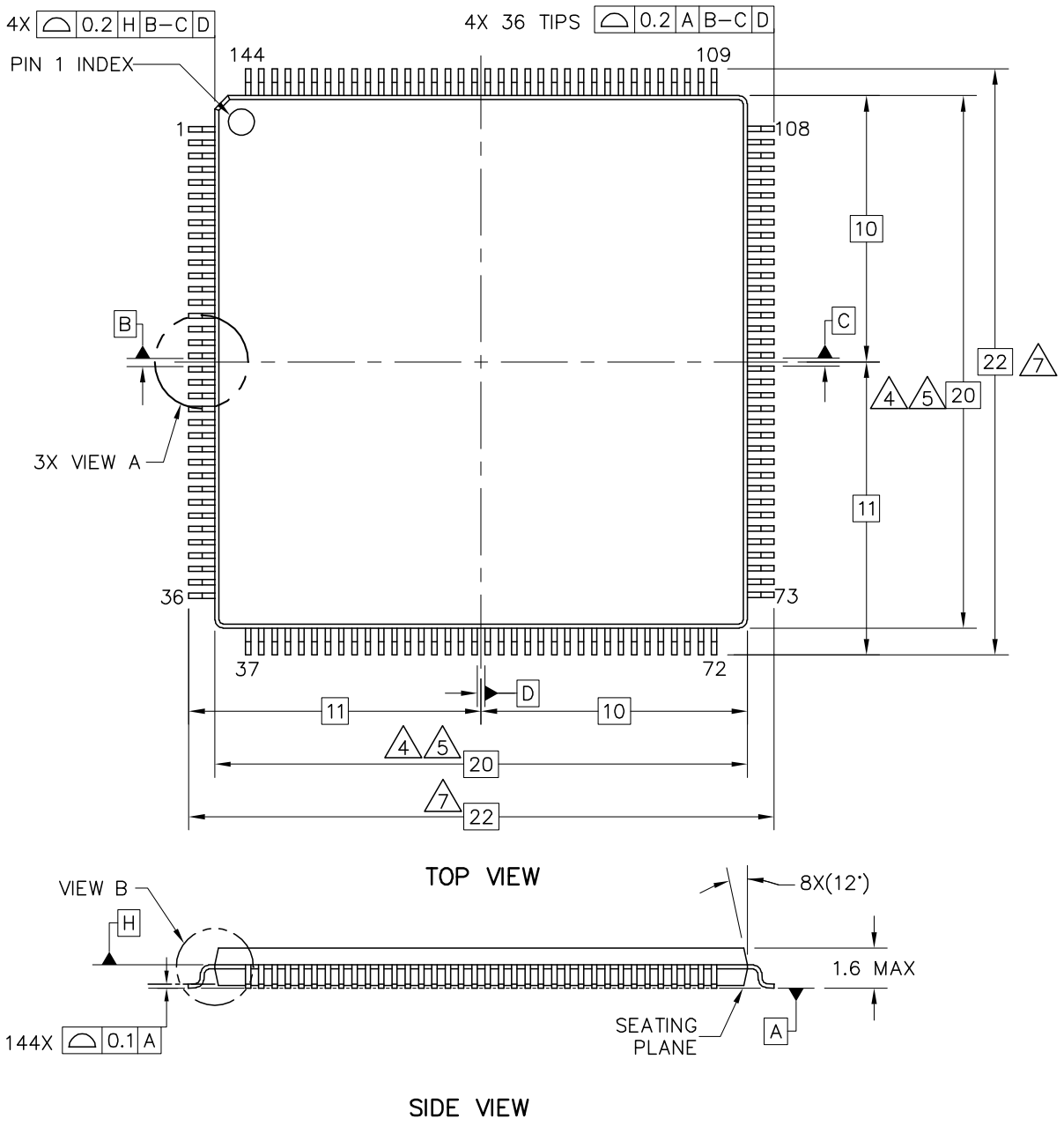


Figure 39. I²C Input/Output Timing

4 Package mechanical data

4.1 144 LQFP



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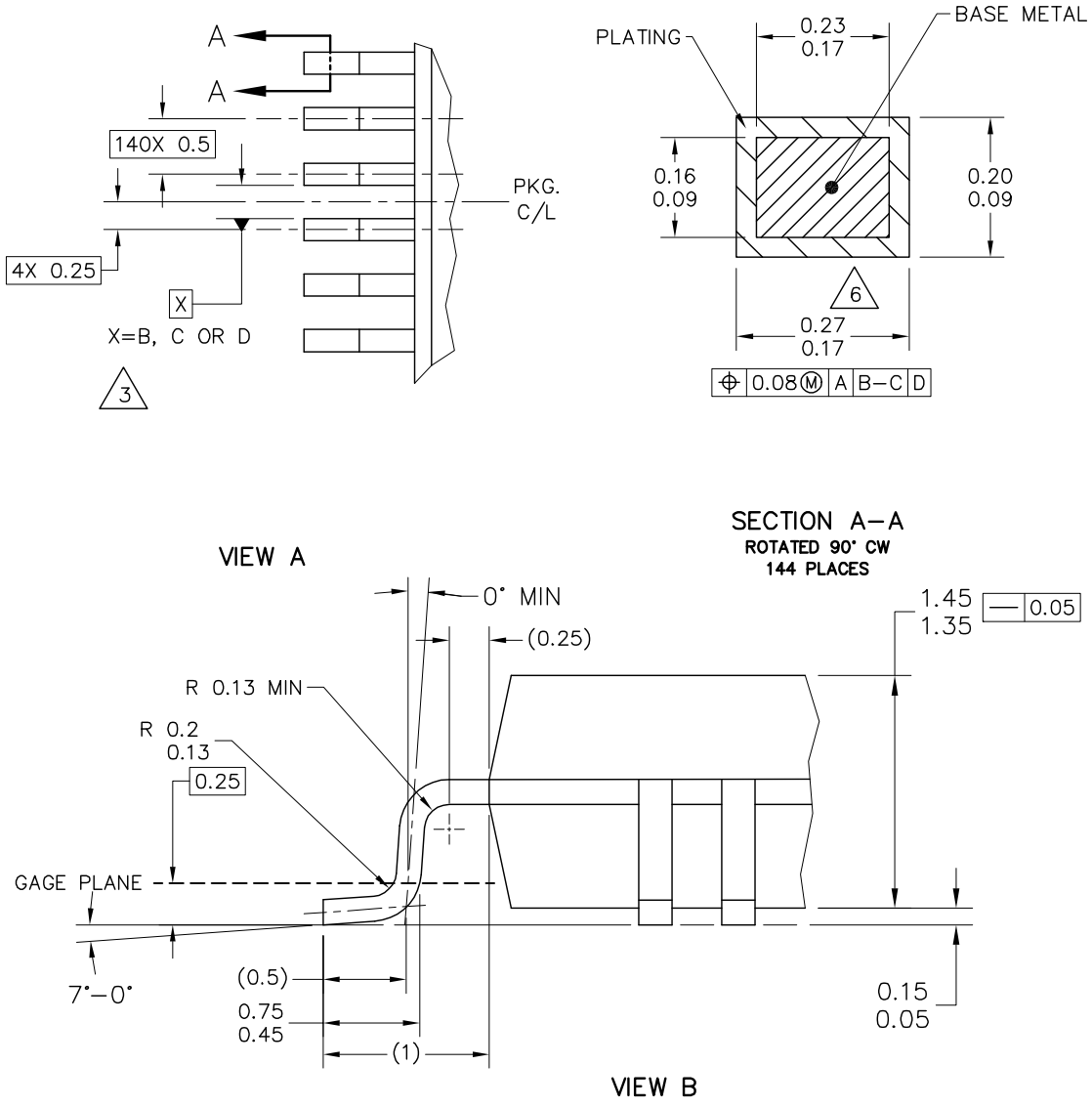
TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

Figure 40. LQFP144 Mechanical Drawing (Part 1 of 3)



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	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

Figure 41. LQFP144 Mechanical Drawing (Part 2 of 3)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.

5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

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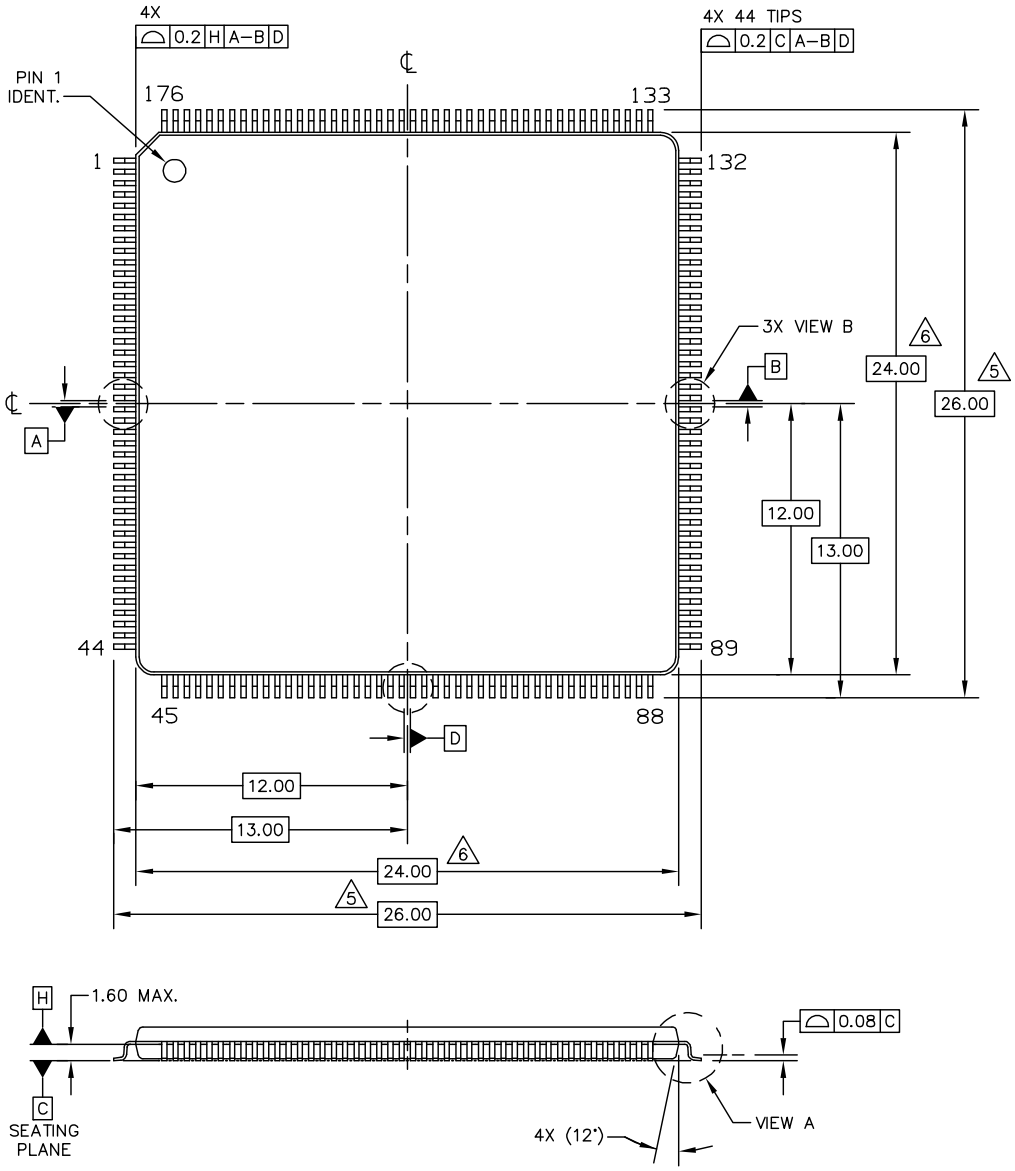
TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

Figure 42. LQFP144 Mechanical Drawing (Part 3 of 3)

4.2 176 LQFP



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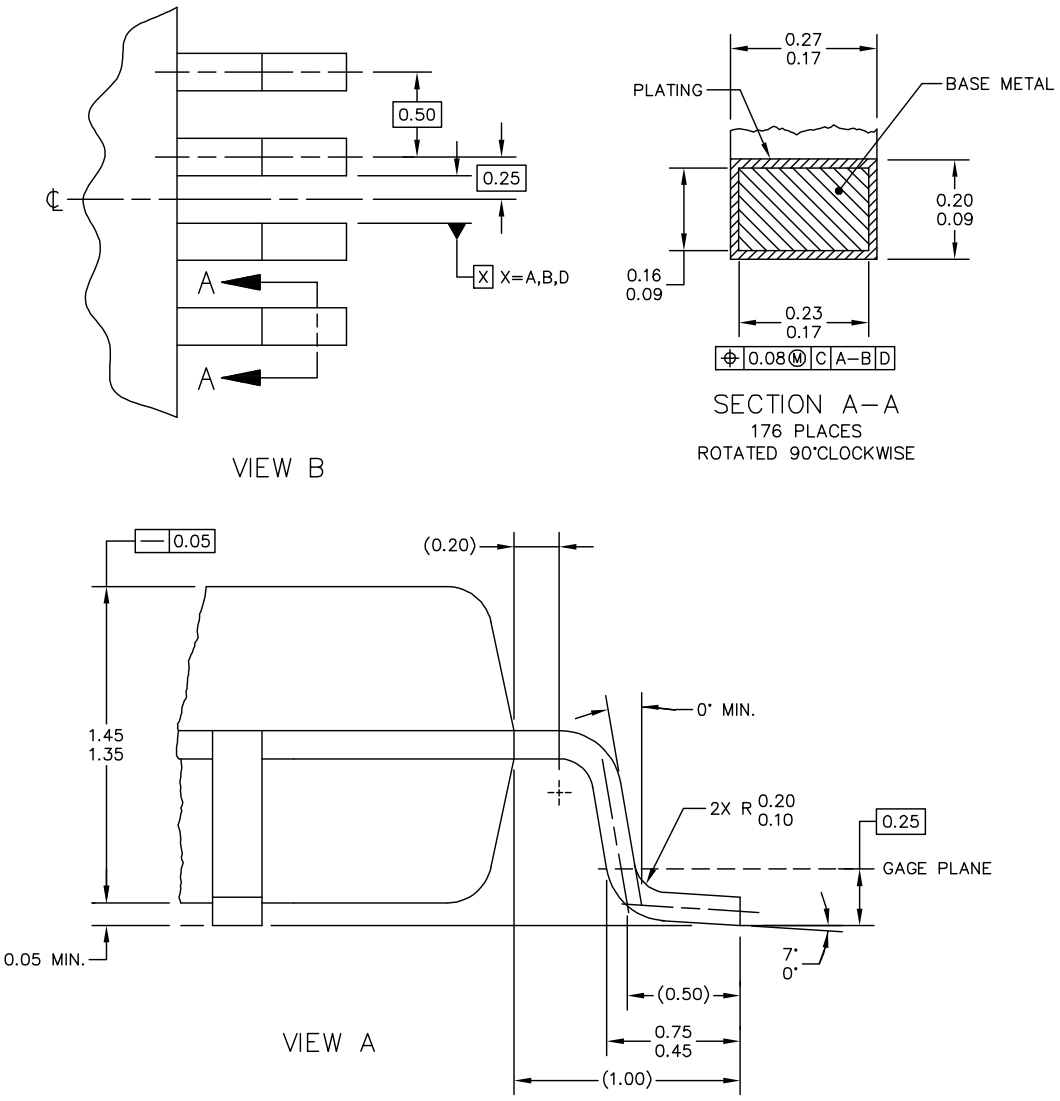
TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 43. LQFP176 Mechanical Drawing (Part 1 of 3)



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	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 44. LQFP176 Mechanical Drawing (Part 2 of 3)

NOTES:

1 DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.

2 DIMENSIONS IN MILLIMETERS.

3 DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4 DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

5 THIS DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM C.

6 THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. THIS DIMENSIONS INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7 THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07.

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	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 45. LQFP176 Mechanical Drawing (Part 3 of 3)

5 Ordering Information

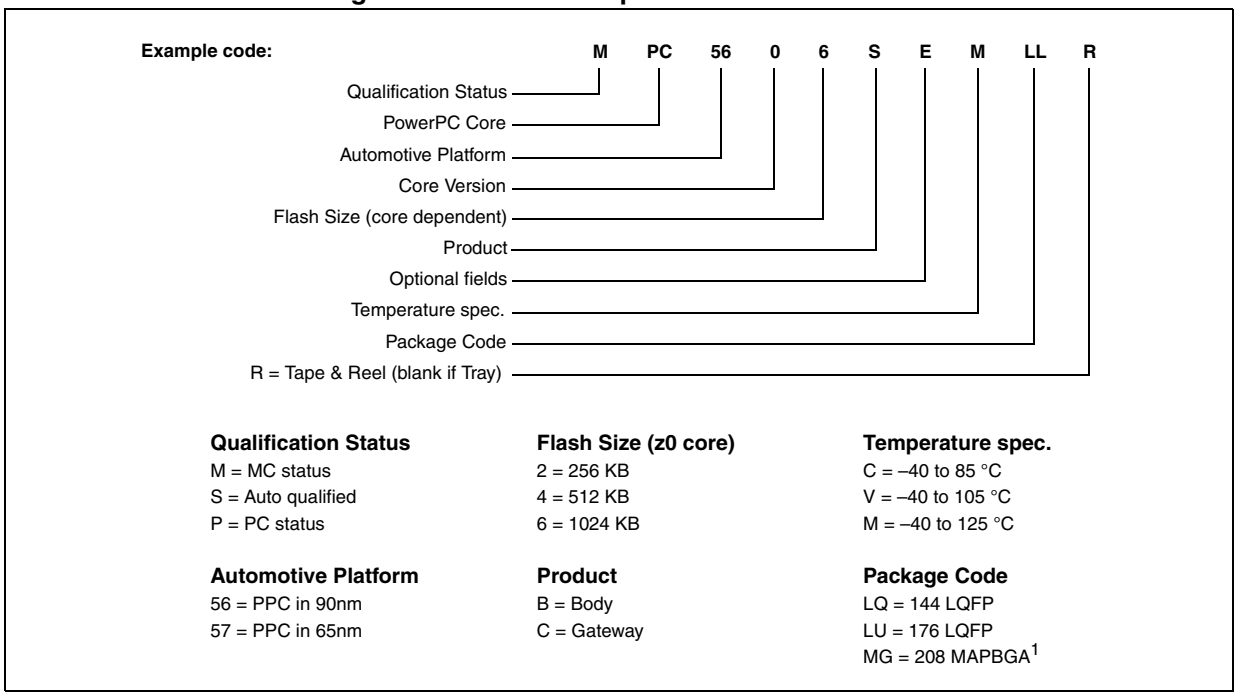
Table 51 shows the orderable part numbers for the MPC560xS series.

Table 51. Orderable Part Number Summary

Part Number	Flash/SRAM	Package	Speed (MHz)
MPC5602SEMLQ	256 KB/24 KB	144 LQFP	64
MPC5604SEMLQ	512 KB/48 KB	144 LQFP	64
MPC5604SEMLQ	512 KB/48 KB	144 LQFP	64
MPC5606SEMLQ	1 MB/48 KB[1]	144 LQFP	64
MPC5606SEMLU	1 MB/48 KB[1]	176 LQFP	64

1 Device also includes 160 KB of graphics SRAM.

Figure 46. Commercial product code structure



1 208 MAPBGA available only as development package for Nexus2+

6 Revision history

Date	Revision	Changes
10-2008	1	Initial release
May-2009	2 Draft B	Minor editing and formatting changes to improve readability Harmonized oscillator naming throughout document Section 1.2, “MPC560xS Features: Updated description of ADC channels Table 1: Changed max number of GPIOs from 132 to 133 for LQFP176 Table 2: Corrected “Peripheral interrupt timer (PIT)” to “Periodic interrupt timer (PIT)” Figure 2: – Added GPIOs to pin function names – Changed function of pin 32: was NC—is VREG_BYPASS – Pin 55: Changed XTAL32 to OSC32K_XTAL – Pin 56: Changed EXTAL32 to OSC32K_EXTAL Figure 3: – Added GPIOs to pin function names – Changed function of pin 32: was NC—is VREG_BYPASS – Pin 71: Changed XTAL32 to OSC32K_XTAL – Pin 72: Changed EXTAL32 to OSC32K_EXTAL Table 4: – Removed pins EXTAL32, XTAL32 and NMI – Updated VRC_CTL I/O direction and pad type Table 7: - Replaced “A” with “I” in pad type column - Modified table footnote 3 to replace pad type “A” definition with pad type “I” definition Table 8: Moved MA[0:2] to follow AN[0:15] Added Section 3.2, “Parameter Classification and added classification tags to electrical characteristics tables where appropriate Added Section 3.3, “NVUSRO register Table 11: Removed ESD_{HBM} Table 14: Merged 144- and 176-pin LQFP characteristics into single table Added Section 3.6, “Electromagnetic compatibility (EMC) characteristics Table 21: Removed “T_A = 25 °C, after trimming” from conditions for V_{PORH}, V_{LVDH3V} and V_{LVDH5V} Table 22: – Changed T_A = –40 to 125 °C to T_A = –40 to 105 °C in note 1 – Added STANDBY1 and STANDBY2 mode current characteristics Figure 6: Updated to reference GPDI register and values for bit PDI Section 3.9.1, “I/O Pad Types: Corrected “four main I/O pad types” to read “three main I/O pad types” Section 3.9.3, “I/O Output DC Characteristics: Replaced ipp_hve with PAD3V5V Table 29: – I_{RMSMED}: Replaced SLOW with MEDIUM in parameter column – I_{RMSFST}: Replaced SLOW with FAST in parameter column Section 3.9.4, “I/O Pad Current Specification: Replaced ipp_hve with PAD3V5V Section 3.10, “RESET electrical characteristics: Replaced ipp_hve with PAD3V5V

Date	Revision	Changes
04-Mar-2009	2 Draft B	Updated Figure 7 Updated Figure 10 Updated Figure 12 Section 3.18, “Pad AC Specifications: Replaced IPP_HVE with PAD3V5V Table 34: Added rows $I_{FIRCSTOP}$ and t_{FIRCSU} Table 35: – Added rows t_{SIRCSU} and $\Delta_{SIRCTRIM}$ – Updated conditions for $\Delta_{SIRCVAR}$ Added Table 40 “ADC input leakage current” Table 38: Updated TUEp and TUEx Made minor editing and formatting changes following review of Rev. 2 Draft B Table 7: Modified PC[0] to PC[9]: – I/O direction: was I, is I/O – pad type: was I, is S Table 38: Updated values for ‘Input current injection’ Section 3.19.3, “Interface to TFT LCD Panels: Modified description of event No. 1 in sequence for active matrix interface timing Table 43: Removed value for Display pixel clock period Table 53: Removed duplicated row for part number MPC5604SEMLQ Section 2.4.2, “Voltage Supply Pins”: Added preferred power up sequence. Section 2.4.6, “Functional Ports A, B, C, D, E, F, G, H, I, J, K”: Changed reset configuration on ADC pins. Section 3, “Electrical Characteristics: Made updates to data. All data is still considered preliminary. Section 3.7.1, “Voltage Regulator Electrical Characteristics”: Added lower power voltage regulator and ultra-low power voltage regulator characteristics.

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
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China
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