High Efficiency Synchronous DC/DC Buck Converter

DESCRIPTION

The TS33000 is a DC/DC synchronous switching regulator with fully integrated power switches, internal compensation, and full fault protection. The switching frequency of 2.25MHz enables the use of extremely small filter components, resulting in smaller board space and reduced BOM costs.

When the input current is greater than approximately 50mA, the TS33000 utilizes PWM voltage mode feedback with input voltage feed-forward to provide a wide input voltage range without the need for external compensation.

For the Fixed Output option, when the input current is less than 50mA, the device uses a PFM mode to provide increased efficiency at light loads. The cross over between PFM mode and PWM is automatic and has hysteresis to prevent oscillation between the modes. Additionally, the nLP mode pin can be used to force the device into PWM mode to reduce the output ripple, if needed (Fixed Output only).

The TS33000 integrates a wide range of protection circuitry; including input supply under-voltage lockout, output under-voltage, output over-voltage, soft start, high side FET and low side FET current limits, and thermal shutdown.

FEATURES

- **Fixed Output option has automatic low power PFM mode for reduced quiescent current at light loads**
- **2.25MHz +/- 10% fixed switching frequency**
- **Adjustable version output voltage range: 0.6V to 5V with +/- 1.5% reference across temperature**
- **Fixed output voltages: 0.8V, 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V with +/- 2% output tolerance**
- **Input voltage range: 2.0V to 5.5V (6.0V Abs Max)**
- Voltage mode PWM control with input voltage feed-forward compensation
- Voltage supervisor for V_{OUT} reported at the PG pin
- Input supply under voltage lockout
- Soft start for controlled startup with no overshoot
- Full protection for over-current, over-temperature, and V_{OUT} overvoltage
- Less than 100nA in shutdown mode
- Multiple enable pins for flexible system sequencing
- Low external component count
- Junction operating temperature -40C to 125C
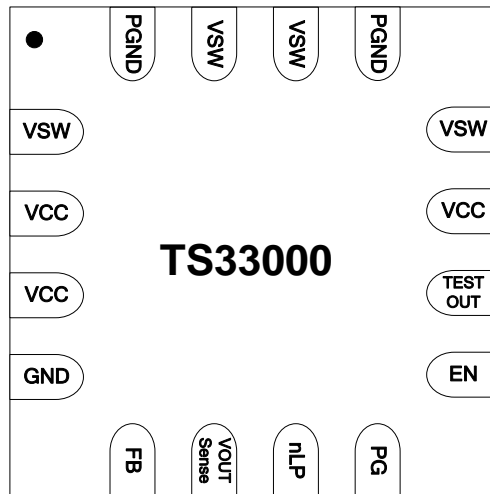- Packaged in a 16 pin QFN (3x3)

APPLICATIONS

- Point of load
- Systems with deep submicron ASICs/FPGAs
- Set-top box
- Communications equipment
- Portable and handheld equipment

TYPICAL APPLICATION
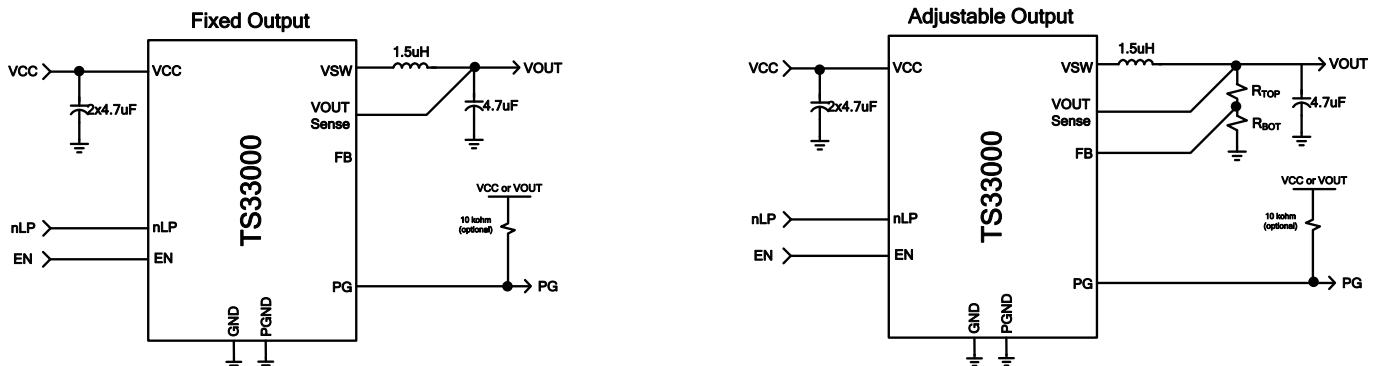
PINOUT

PIN DESCRIPTION

Pin Symbol	Pin #	Function	Description
VSW	1	Switching Voltage Node	Connect to 1.5uH inductor. Short to Pins 12, 14, & 15
VCC	2	Input Voltage	Input voltage supply. Short to Pins 3 & 11
VCC	3	Input Voltage	Input voltage supply. Short to Pins 2 & 11
GND	4	GND	Ground for the internal circuitry of the device
FB	5	Feedback Input	Feedback voltage for the regulator when used in adjustable mode. Connect to the output voltage resistor divider for adjustable mode and No Connection for fixed output modes
V_{OUT} Sense	6	Output Voltage Sense	Output Voltage Sense. Requires kelvin connection to 4.7uF output capacitor
nLP	7	nLP Input	Forcing this pin high prevents the device from going into Low Power PFM mode operation
PG	8	PG Output	Power Good indicator Open-drain output.
EN	9	Enable Input	Input high voltage enables the device. Input low disables the device.
TEST OUT	10	Test Mode Output	Connect to GND. For internal testing use only.
VCC	11	Input Voltage	Input voltage supply. Short to Pins 2 & 3
VSW	12	Switching Voltage Node	Connect to 1.5uH inductor. Short to Pins 1, 14, & 15
PGND	13	Power GND	GND supply for internal low-side FET/integrated diode. Short to Pin 16
VSW	14	Switching Voltage Node	Connect to 1.5uH inductor. Short to Pins 1, 12, & 15
VSW	15	Switching Voltage Node	Connect to 1.5uH inductor. Short to Pins 1, 12, & 14
PGND	16	Power GND	GND supply for internal low-side FET/integrated diode. Short to Pin 13

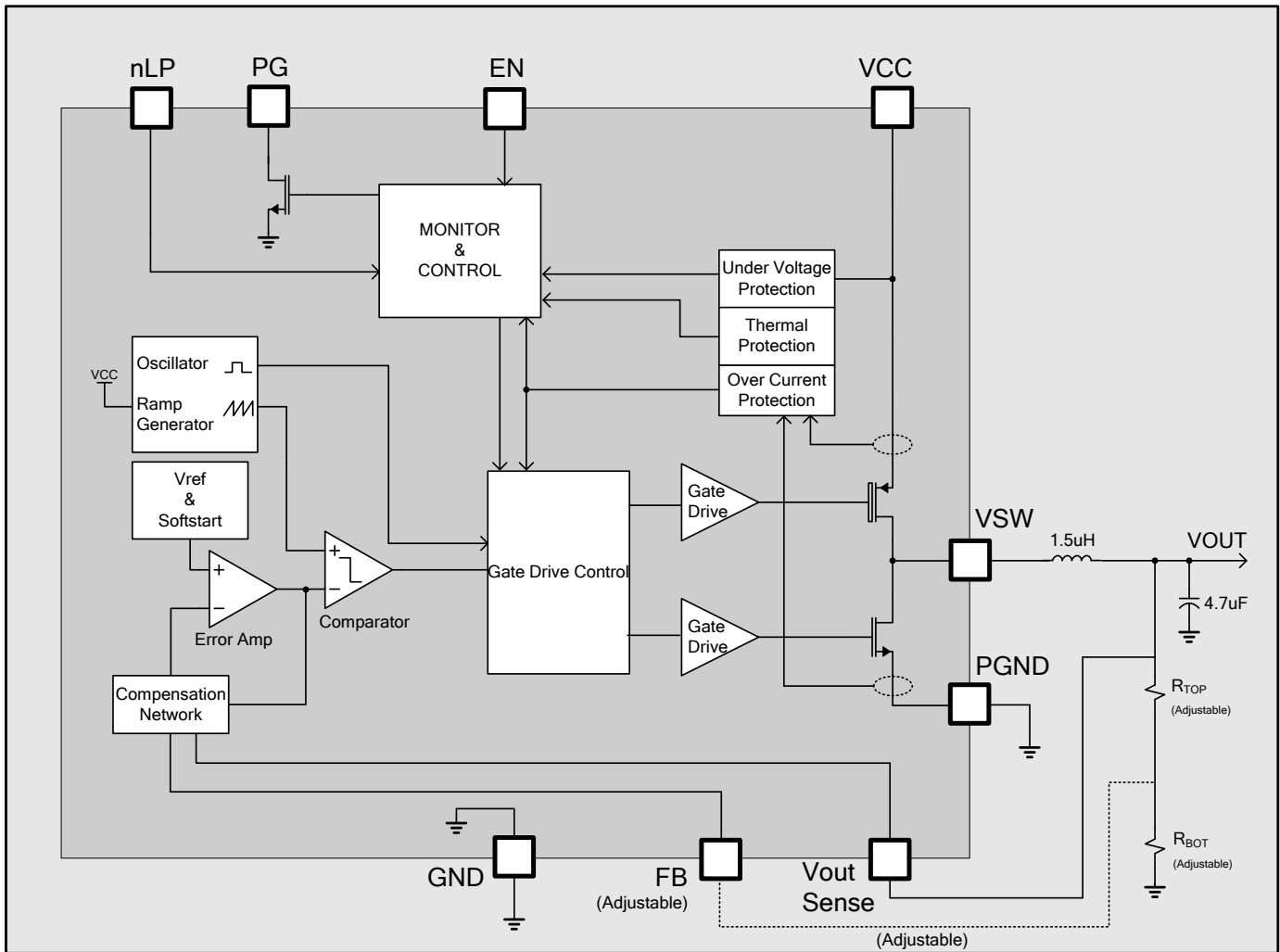# FUNCTIONAL BLOCK DIAGRAM

Figure 1: TS33000 Block Diagram for fixed and adjustable mode devices

PRODUCT FAMILY MATRIX

Package Options – QFN16
Output Voltage –0.8V, 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, Adjustable (0.6V – 5V)

ABSOLUTE MAXIMUM RATINGS

Over operating free–air temperature range unless otherwise noted[1,2]

		UNIT
VCC	-0.3 to 6.0	V
VSW	-1 to 6.0	V
EN, PG,FB, nLP, TEST OUT, V_{OUT} Sense	-0.3 to 6	V
Electrostatic Discharge – Human Body Model	±2k	V
Electrostatic Discharge – Charge Device Model	±500	V
Lead Temperature (soldering, 10 seconds)	260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air (Note 1)	50	°C/W
T_{STG}	Storage Temperature Range	-65 to 150	°C
$T_{J\,MAX}$	Maximum Junction Temperature	150	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes QFN16 1 in^2 area of 2 oz copper and 25°C ambient temperature.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input Operating Voltage	2.0	3.3	5.5	V
L_{OUT}	Output Filter Inductor Typical Value (Note 1,3)	1.2	1.5	1.8	uH
C_{OUT}	Output Filter Capacitor Typical Value (Note 2,3)	3.76	4.7	5.64	uF
$C_{OUT-ESR}$	Output Filter Capacitor ESR	0	5	20	mΩ
C_{BYPASS}	Input Supply Bypass Capacitor Typical Value (Note 2)		2x4.7uF		uF

Note 1: For best performance, an inductor with a saturation current rating higher than the maximum V_{OUT} load requirement plus the inductor current ripple.
　　　See the inductor current ripple calculations in inductor calculations sections.
Note 2: For best performance, a low ESR ceramic capacitor should be used – X7R or X5R types should be used. Y5V should be avoided.
Note 3: Min and max listed are to account for +/-20% variation of the typical value. Typical values of 4.7uF and 1.5uH are recommended.

CHARACTERISTICS

Electrical Characteristics, T_J = -40C to 125C, VCC = 5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC Supply Voltage						
VCC	Input Supply Voltage		2.0		5.5	V
$I_{CC\text{-}NORM}$	Quiescent current Normal Mode	VCC = 3.3V, I_{LOAD} = 0A, EN=3.3V, nLP=3.3V		18		mA
$I_{CC\text{-}LPM}$	Quiescent current Low Power PFM Mode	VCC = 3.3V, I_{LOAD} = 0A, EN=3.3V, nLP=0V		45		uA
$I_{CC\text{-}SHUTDOWN}$	Quiescent current Shutdown Mode	VCC = 3.3V, EN=0V		0.1		uA
VCC Under Voltage Lockout						
$VCC_{\text{-}UV}$	Input Supply Under Voltage Threshold	VCC Increasing		1.9	2.0	V
$VCC_{\text{-}UV\_HYST}$	Input Supply Under Voltage Threshold Hysteresis			100		mV
OSC						
F_{OSC}	Oscillator Frequency		2.0	2.25	2.5	MHz
PG Open Drain Outputs						
T_{PG}	PG Release Timer			10		ms
$I_{OH\text{-}PG}$	High-Level Output Leakage	V_{PG}=5V VCC=5V		0.1		uA
$V_{OL\text{-}PG}$	Low-Level Output Voltage	I_{PG} = -0.3mA			0.1	V
EN/nLP Input Voltage Thresholds						
$V_{IH\text{-}EN/nLP}$	High Level Input Voltage	VCC=2V to 5V	1.0			V
$V_{IL\text{-}EN/nLP}$	Low Level Input Voltage	VCC=2V to 5V			0.4	V
$V_{HYST\text{-}EN/nLP}$	Input Hysteresis	VCC=2V to 5V		100		mV
$I_{IN\text{-}EN}$	EN Input Leakage	V_{EN}=5V VCC=5V		0.1		uA
		V_{EN}=0V VCC=5V		0.1		uA
nLP_{PD}	nLP Pulldown Resistor	Pulldown to GND		100		KΩ
Thermal Shutdown						
TSD	Thermal Shutdown Junction Temperature		150	170	190	C
TSD_{HYST}	TSD Hysteresis			10		C

REGULATOR CHARACTERISTICS

Electrical Characteristics, T_J = -40C to 125C, VCC = 5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Switch Mode Regulator: L=1.5uH and C=4.7uF						
$V_{OUT-PWM}$	Output Voltage Tolerance in Mode		V_{OUT} - 2%	V_{OUT}	V_{OUT} + 2%	V
R_{DSON}	High Side Switch On Resistance	I_{VSW} = -300mA		110		mΩ
	Low Side Switch On Resistance	I_{VSW} = 300mA		75		mΩ
I_{OUT}	Output Current	TS33000			300	mA
I_{OCDHS}	Over Current Detect HS	TS33000		600		mA
I_{OCDLS}	Over Current Detect LS	TS33000		600		mA
$V_{OUT-LINE}$	Output Line Regulation	VCC = 2.5V to 5V, V_{OUT} = 1.8V, I_{LOAD} = 300mA	-10		10	mV
$V_{OUT-LOAD}$	Output Load Regulation	I_{LOAD} = 10mA to 300mA, VCC = 5V, V_{OUT} = 1.8V	V_{OUT} - 0.5%	V_{OUT}	V_{OUT} + 0.5%	V
FB_{TH}	Feedback Reference	FB Switch Point		0.6		V
FB_{TH-TOL}	Feedback Reference Tolerance		-1.5		1.5	%
I_{FB}	Feedback Input Current			100nA		nA
T_{SS}	Softstart Ramp Time			500		Us
V_{OUT-PG}	V_{OUT} Power Good Threshold			85% V_{OUT}		
V_{OUT-PG_HYST}	V_{OUT} Power Good Hysteresis			2% V_{OUT}		
V_{OUT-OV}	V_{OUT} Over Voltage Threshold			106% V_{OUT}		
V_{OUT-OV_HYST}	V_{OUT} Over Voltage Hysteresis			2% V_{OUT}		

FUNCTIONAL DESCRIPTION

This voltage-mode Point of Load (POL) synchronous step-down power supply product can be used in the consumer, industrial, and automotive market segments. It includes flexibility to be used for a wide range of output voltages and is optimized for high efficiency power conversion with low R_{DSON} integrated synchronous switches. A 2.25MHz internal switching frequency facilitates low cost LC filter combinations and improved transient response. Additionally, the fixed output version, with integrated Power on Reset and Fault circuitry enables a minimal external component count to provide a complete power supply solution for a variety of applications.

DETAILED PIN DESCRIPTION

Unregulated input, VCC
This terminal is the unregulated input voltage source for the IC. It is recommended that 2 4.7uF bypass capacitors be placed close as possible to the VCC pins for best performance. Since this is the main supply for the IC, good layout practices need to be followed for this connection.

Feedback, FB
This is the voltage feedback input terminal for the adjustable version. For the fixed mode versions, this pin should be left floating and not connected.
The connection on the PCB should be kept as short as possible from the feedback resistors, kept away from the VSW connections or other switching/high frequency nodes, and should not be shared with any other connection. This should minimize stray coupling, reduce noise injection, and minimize voltage shift cause by output load.

To choose the resistors for the adjustable version, use the following equation:

$$V_{OUT} = 0.6 \ (1 + R_{TOP}/R_{BOT})$$

For stability, RTOP should be 270K Ohms to 330K Ohms.

Output Voltage Sense, V_{OUT} Sense
This is the input terminal for the voltage output feedback and is needed for both adjustable and fixed voltage versions. This should be connected to the main output capacitor, and the same good layout practices should be followed as for the FB connection. Keep this line as short as possible, keep it away from the VSW and other switching or high frequency traces, and do not share this connection with any other connection on the PCB.

Switching output, VSW
This is the switching node of the regulator. It should be connected directly to the 1.5uH inductor with a wide, short trace. It is switching between VCC and PGND at the switching frequency.

Ground, GND
This ground is used for the majority of the device including the analog reference, control loop, and other circuits.

Power Ground, PGND
This is a separate ground connection used for the low side synchronous FET to isolate switching noise from the rest of the device.

Enable, EN
This is an input terminal to activate the entire device. This will enable the internal reference, oscillator, TSD, etc, and allow the fault detection circuitry to work correctly. Notice that the EN needs to low for the part to exhibit 100nA quiescent current.

Power Good Output, PG

This is an open drain, active high output. The switched mode output voltage is monitored and the PG line will remain low until the output voltage reaches the V_{OUT-UV} threshold, approximately 85% of the final regulation output. Once the internal comparator detects the output voltage is above the desired threshold, an internal 10mSec delay timer is activated and the PG line is de-asserted to high when this delay timer expires. In the event the output voltage decreases below V_{OUT-UV}, the PG line will be asserted low immediately and remain low until the output rises above V_{OUT-UV} and the delay timer times out again. If EN is pulled low, the VCC input undervoltage trips, or Thermal Shutdown is reached, the PG pin will immediately be pulled low.

nLow Power Mode Output, nLP

This is an input to force the PWM mode when light load is on the output. The PFM low power mode has higher output voltage ripple, which is some applications may be unacceptable. If low ripple is needed on the output this pin can be tied to VCC input, or switched above 1.0V during operation to force the device into normal PWM mode.

INTERNAL PROTECTION DETAILS

Internal Current Limit

Current limit is always active when the regulator is enabled. High side current limit will shorten the high side on time and tri-state the high side. Additionally, low side current limit will protect the low side FET and turn off the switch if current limit is sensed on the low side switch. Since the output is fully synchronous, the current limit is protected on the low side in both the positive and negative direction.

Soft Start

Soft start ensures current limit does not prevent regulator startup and minimize overshoot at startup. The typical startup time is 925us. These values do not change with output voltage, current limit settings, or adjustable/fixed mode. The soft start is re-triggered with the any rising edge that enables the regulator, including the EN input pins, thermal shutdown, VCC Undervoltage, or a VCC Power cycle.

Thermal Shutdown

If the temperature of the die exceeds 170C, the VSW outputs will tri-state to protect the device from damage. The PG and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160C, the device will attempt to start up again, following the normal soft start sequence with 10ms delay on PG. If the device reaches 170C, the shutdown/restart sequence will repeat.

Output Overvoltage

If the output of the regulator exceeds 106% of the regulation voltage, the VSW outputs will tri-state to protect the device from damage. This check occurs at the start of each switching cycle. If it occurs during the middle of a cycle, the switching for that cycle will complete, and the VSW outputs will tri-state at the beginning of the next cycle.

VCC Under-Voltage Lockout

The device is held in the off state until VCC reaches 1.9V. There is a 100mV hysteresis on this input, which requires the input to fall below 1.8V before the device will disable.

PERFORMANCE RESULTS

Startup Plots - TBD
Switching Plots -TBD
Load Transient Plots - TBD
Line Transient Plots - TBD
Efficiency Plots - TBD
OSC frequency across temp -TBD
Output voltage across temp –TBD
Line Regulation – TBD
Load Regulation – TBD

EXTERNAL COMPONENT SELECTION

The internal compensation is optimized for a 4.7uF output capacitor and a 1.5uH inductor.   To keep the output ripple low, a low ESR (less than 20mOhm) ceramic is recommended. For optimal over-current protection, inductor should be able to handle the 400mA without saturation.

LAYOUT GUIDELINES
TBD

RECOMMENDED COMPONENTS / DESIGN EXAMPLE
TBD

PACKAGE MECHANICAL DRAWINGS (all dimensions in mm)

TOP VIEW

BOTTOM VIEW
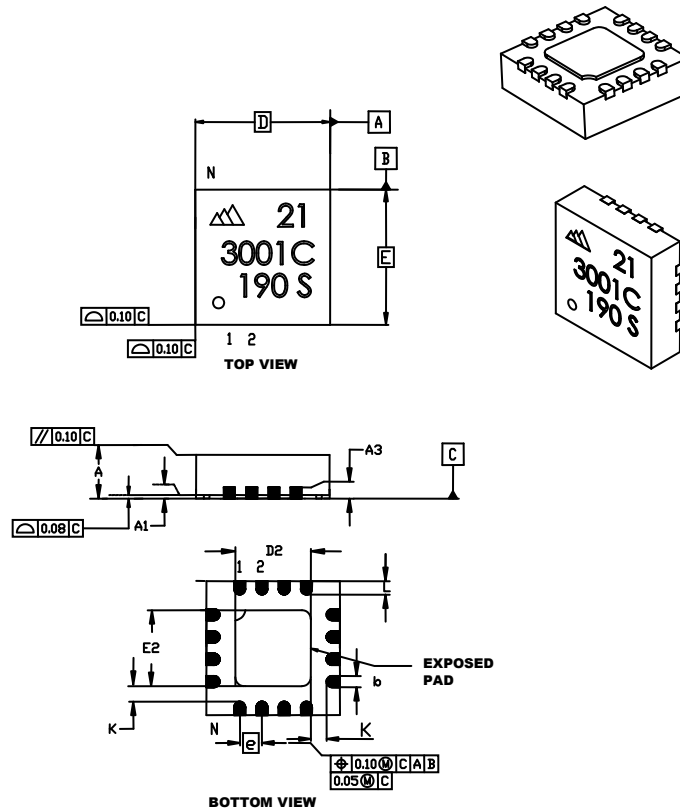
EXPOSED PAD

Units		MILLIMETERS		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.55	1.70	1.80
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.30	0.40
Contact-to-Exposed Pad	K	0.20	-	-

RECOMMEDED PCB LAND PATTERN

**RECOMMENDED
LAND PATTERN**
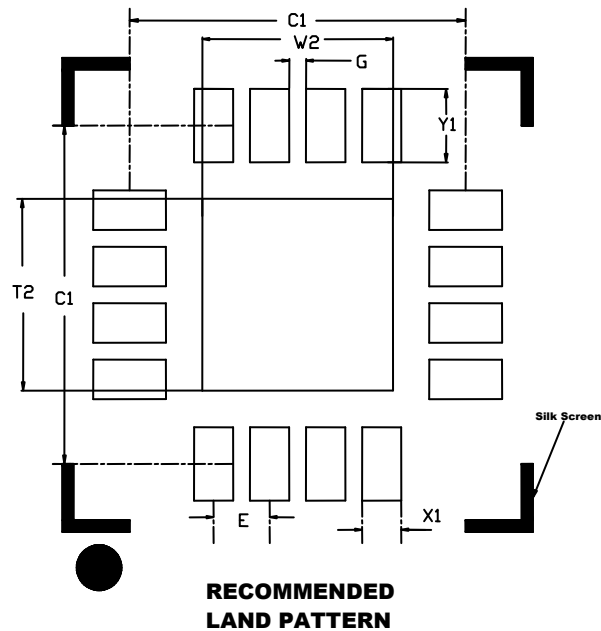
DIMENSIONS IN MILLIMETERS

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2	-	-	1.70
Optional Center Pad Length	T2	-	-	1.70
Contact Pad Spacing	C1	-	3.00	-
Contact Pad Spacing	C2	-	3.00	-
Contact Pad Width (X16)	X1	-	-	0.35
Contact Pad Length (X16)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

Notes:
Dimensions and tolerances per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact values shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information only.

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