

SI1917EDH

PRODUCT SUMMARY

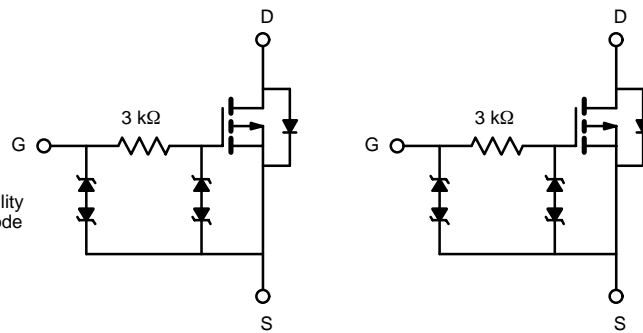
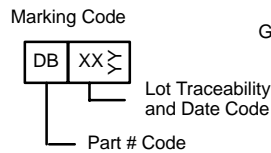
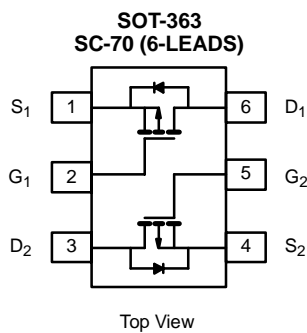
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.370 @ $V_{GS} = -4.5$ V	-1.15
	0.575 @ $V_{GS} = -2.5$ V	-0.92
	0.800 @ $V_{GS} = -1.8$ V	-0.78

FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- ESD Protected: 3000 V
- Thermally Enhanced SC-70 Package

APPLICATIONS

- Load Switching
- PA Switch
- Level Switch



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-12		V	
Gate-Source Voltage	V_{GS}	± 12			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-1.15	-1.00	A
		$T_A = 85^\circ\text{C}$	-0.83	-0.73	
Pulsed Drain Current	I_{DM}	-3			
Continuous Diode Current (Diode Conduction) ^a	I_S	-0.61	-0.47		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	0.73	0.57	W
		$T_A = 85^\circ\text{C}$	0.38	0.30	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ sec	130	170	$^\circ\text{C/W}$
		Steady State	170	220	
Maximum Junction-to-Foot (Drain)	R_{thJF}	80	100		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.



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SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -100 μA	-0.45			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±4.5 V			±1.5	μA
		V _{DS} = 0 V, V _{GS} = ±12 V			±10	mA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -9.6 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -9.6 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-2			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -1.0 A		0.300	0.370	Ω
		V _{GS} = -2.5 V, I _D = -0.81 A		0.470	0.575	
		V _{GS} = -1.8 V, I _D = -0.2 A		0.660	0.800	
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -1.0 A		1.7		S
Diode Forward Voltage ^a	V _{SD}	I _S = -0.47 A, V _{GS} = 0 V		-0.85	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -6 V, V _{GS} = -4.5 V, I _D = -1.0 A		1.3	2.0	nC
Gate-Source Charge	Q _{gs}			0.31		
Gate-Drain Charge	Q _{gd}			0.31		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -6 V, R _L = 12 Ω I _D ≅ -0.5 A, V _{GEN} = -4.5 V, R _G = 6 Ω		0.17	0.26	μs
Rise Time	t _r			0.47	0.71	
Turn-Off Delay Time	t _{d(off)}			0.96	1.4	
Fall Time	t _f			1.0	1.5	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.