

FQA8N90C_F109

N-Channel QFET® MOSFET

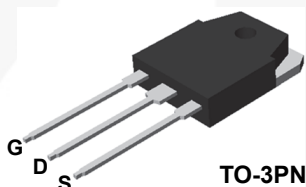
900 V, 8 A, 1.9 Ω

Features

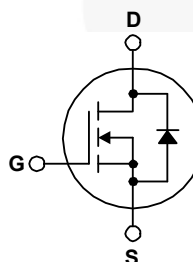
- 8 A, 900 V, $R_{DS(on)} = 1.9 \Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 4 \text{ V}$
- Low Gate Charge (Typ. 35 nC)
- Low Crss (Typ. 12 pF)
- 100% Avalanche Tested
- RoHS Compliant

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



TO-3PN



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQA8N90C_F109	Unit
V_{DSS}	Drain-Source Voltage	900	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	8.0	A
		5.1	A
I_{DM}	Drain Current - Pulsed (Note 1)	32	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	850	mJ
I_{AR}	Avalanche Current (Note 1)	8.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	24	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	240	W
	- Derate above 25°C	1.92	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQA8N90C_F109	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.52	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA8N90C_F109	FQA8N90C	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
Off Characteristics							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	900	--	--	V	
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.95	--	V/°C	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 900 V, V _{GS} = 0 V	--	--	10	μA	
		V _{DS} = 720 V, T _C = 125°C	--	--	100	μA	
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA	
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA	
On Characteristics							
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3.0	--	5.0	V	
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 4.0 A	--	1.6	1.9	Ω	
g _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 4.0 A	--	5.5	--	S	
Dynamic Characteristics							
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	1600	2080	pF	
C _{oss}	Output Capacitance		--	130	170	pF	
C _{rss}	Reverse Transfer Capacitance		--	12	15	pF	
Switching Characteristics							
t _{d(on)}	Turn-On Delay Time	V _{DD} = 450 V, I _D = 11.0A, R _G = 25 Ω	--	40	90	ns	
t _r	Turn-On Rise Time		--	110	230	ns	
t _{d(off)}	Turn-Off Delay Time		(Note 4)	--	70	150	ns
t _f	Turn-Off Fall Time		(Note 4)	--	70	150	ns
Q _g	Total Gate Charge	V _{DS} = 720 V, I _D = 11.0A, V _{GS} = 10 V	--	35	45	nC	
Q _{gs}	Gate-Source Charge		(Note 4)	--	10	--	nC
Q _{gd}	Gate-Drain Charge		(Note 4)	--	14	--	nC
Drain-Source Diode Characteristics and Maximum Ratings							
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	8.0	A	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	32.0	A	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 8.0 A	--	--	1.4	V	
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 8.0 A, di _F / dt = 100 A/μs	--	530	--	ns	
Q _{rr}	Reverse Recovery Charge		--	5.8	--	μC	

Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. L = 25 mH, I_{AS} = 8 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 8 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

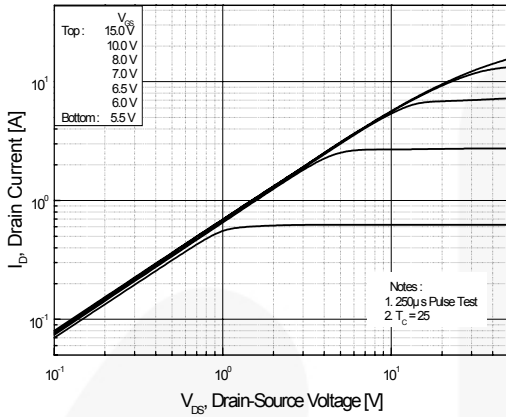


Figure 2. Transfer Characteristics

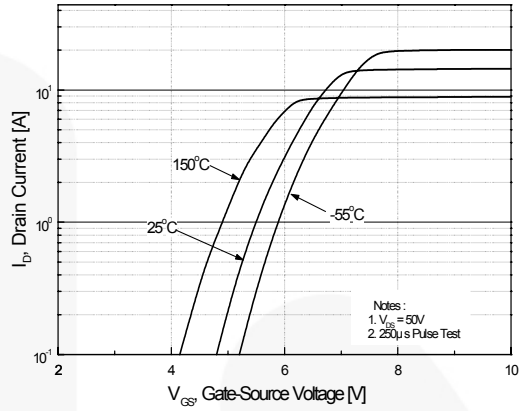


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

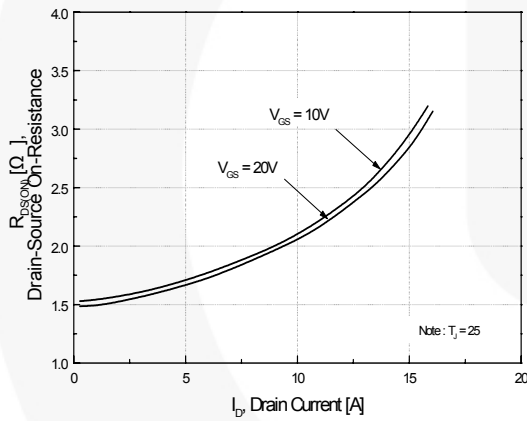


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

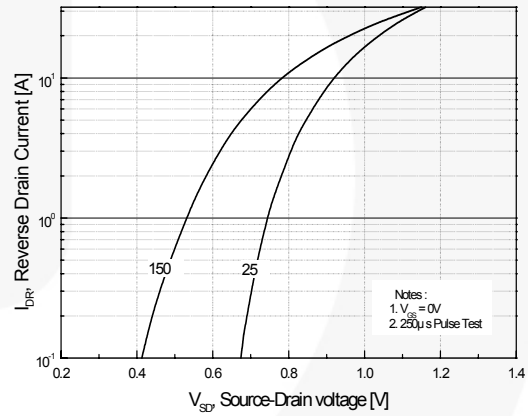


Figure 5. Capacitance Characteristics

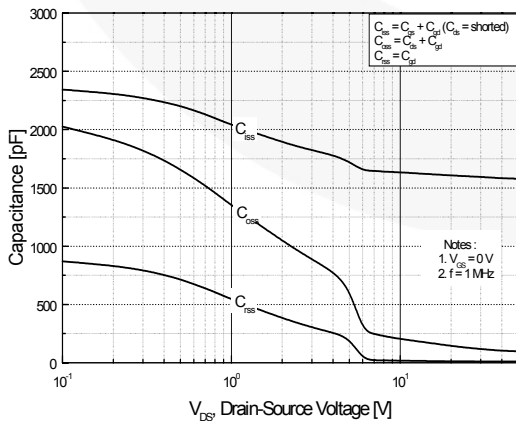
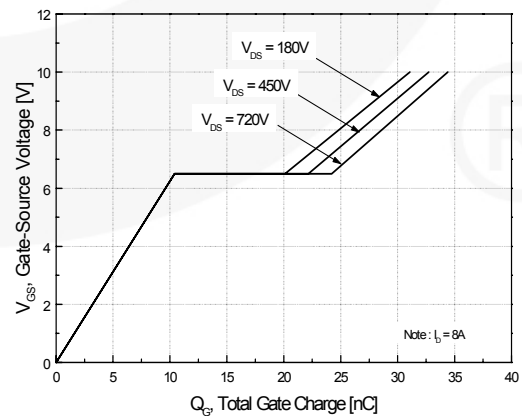


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

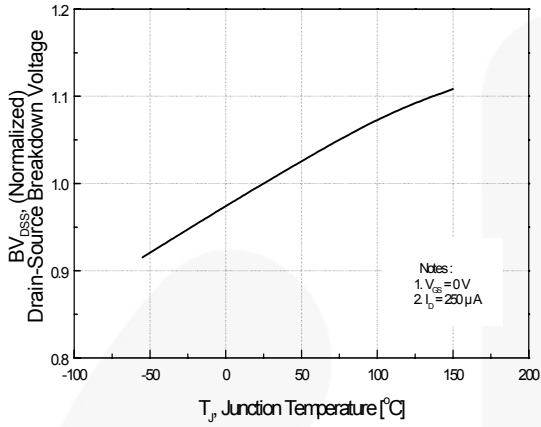


Figure 8. On-Resistance Variation vs. Temperature

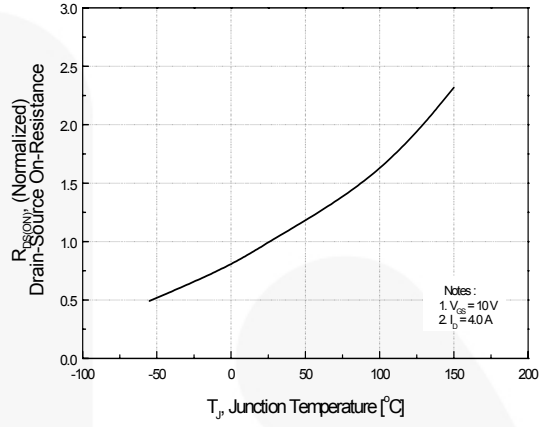


Figure 9. Maximum Safe Operating Area

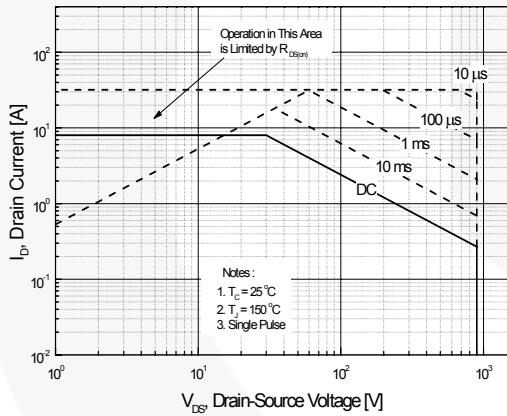


Figure 10. Maximum Drain Current vs. Case Temperature

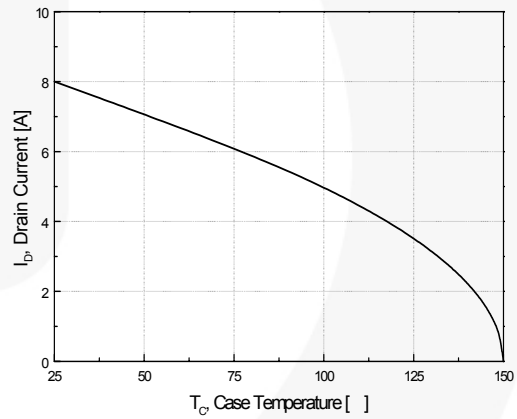
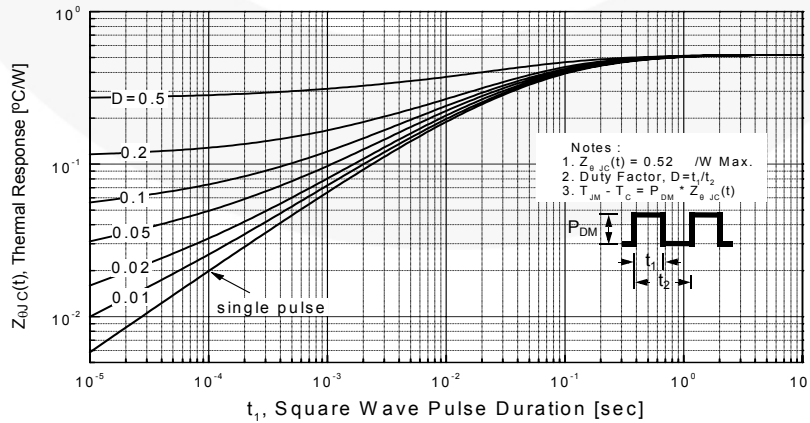


Figure 11. Transient Thermal Response Curve



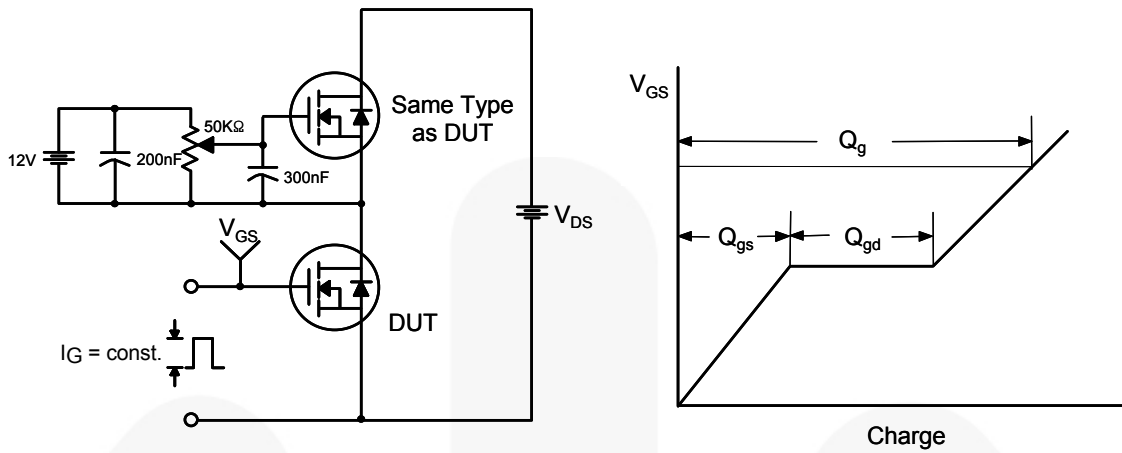


Figure 12. Gate Charge Test Circuit & Waveform

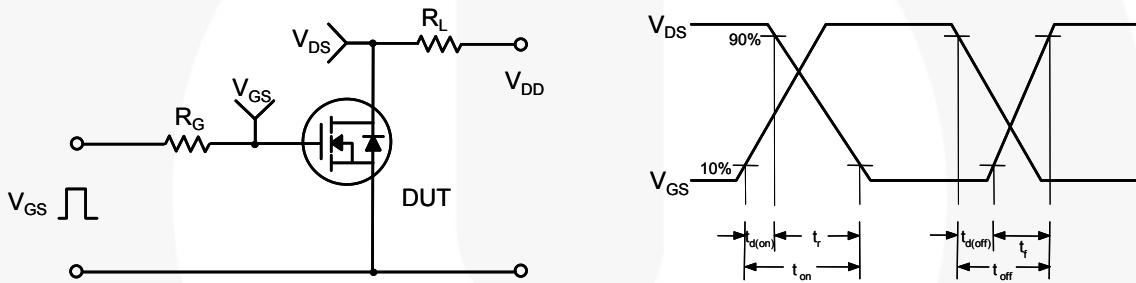


Figure 13. Resistive Switching Test Circuit & Waveforms

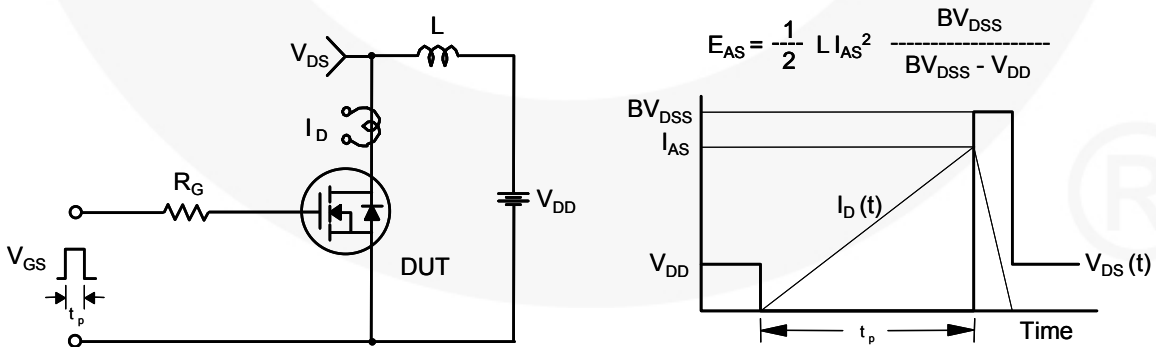


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

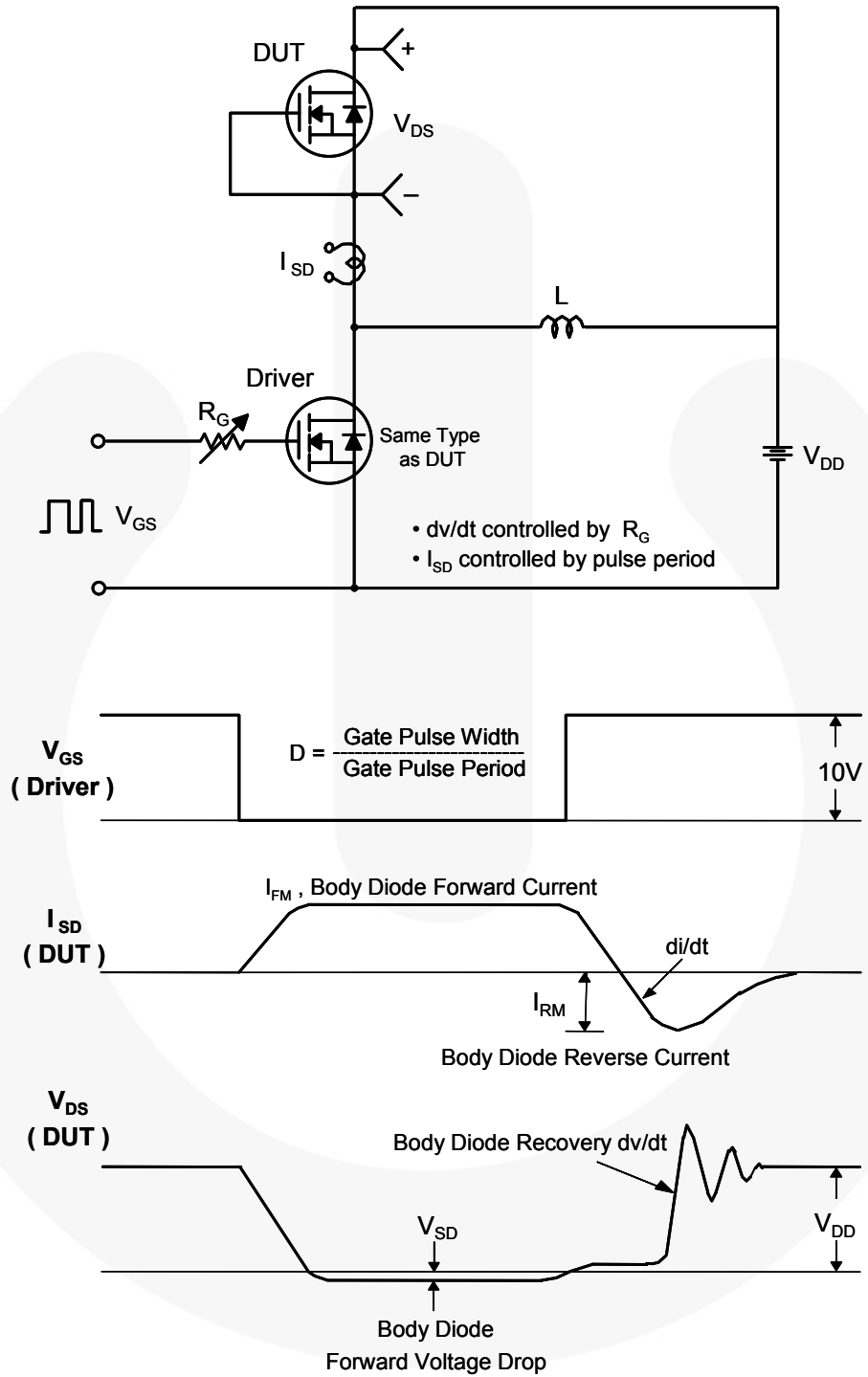
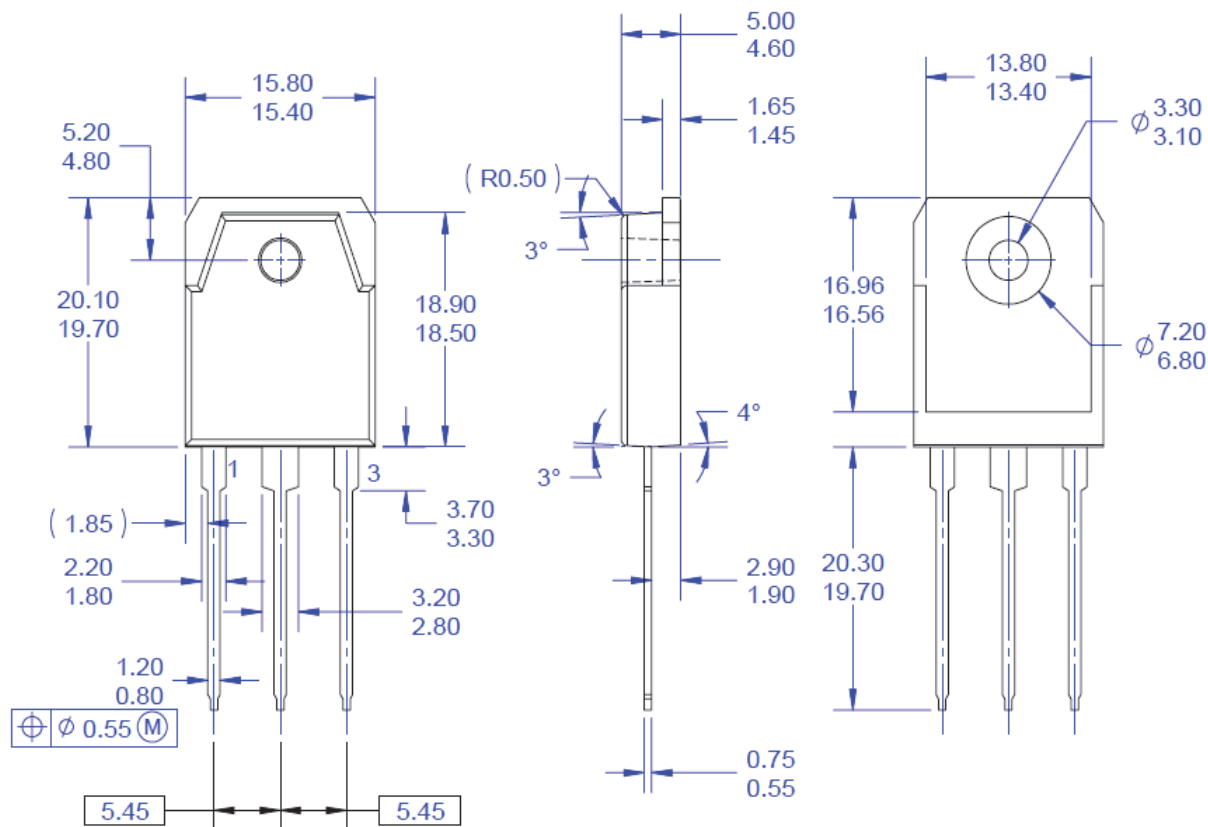


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- E) THIS PACKAGE IS INTENDED ONLY FOR TO3PN.
- F) DRAWING FILE NAME: TO3P03AREV4.

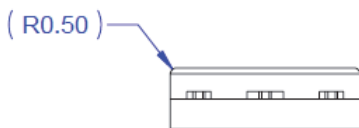


Figure 16. TO3, 3-Lead, Plastic, EIAJ SC-65

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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