

Features

- Advanced Process Technology
- New Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

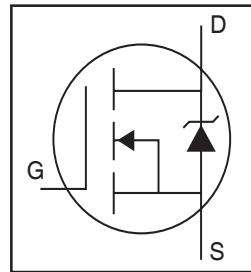
Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and wide variety of other applications.

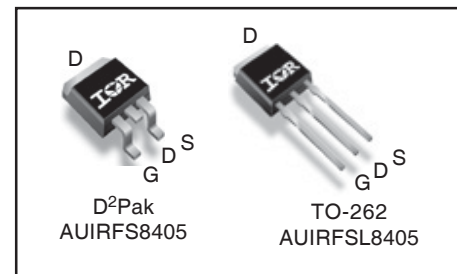
Applications

- Electric Power Steering (EPS)
- Battery Switch
- Start/Stop Micro Hybrid
- Heavy Loads
- DC-DC Applications

HEXFET® Power MOSFET



| | |
|-------------------------------|------------------------------|
| V_{DSS} | 40V |
| $R_{DS(on)}$ typ. max. | 1.9mΩ 2.3mΩ |
| I_D (Silicon Limited) | 193A Ⓞ |
| I_D (Package Limited) | 120A |



| | | |
|----------|----------|----------|
| G | D | S |
| Gate | Drain | Source |

| Base part number | Package Type | Standard Pack | | Complete Part Number |
|------------------|--------------|---------------------|----------|----------------------|
| | | Form | Quantity | |
| AUIRFSL8405 | TO-262 | Tube | 50 | AUIRFSL8405 |
| AUIRFS8405 | D2Pak | Tube | 50 | AUIRFS8405 |
| | | Tape and Reel Left | 800 | AUIRFS8405TRL |
| | | Tape and Reel Right | 800 | AUIRFS8405TRR |

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

| Symbol | Parameter | Max. | Units |
|---------------------------------|---|-------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited) | 193Ⓞ | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited) | 137Ⓞ | |
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited) | 120 | |
| I_{DM} | Pulsed Drain Current Ⓞ | 904 | |
| $P_D @ T_C = 25^\circ\text{C}$ | Maximum Power Dissipation | 163 | W |
| | Linear Derating Factor | 1.1 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |
| | Mounting torque, 6-32 or M3 screw | 10lbf·in (1.1N·m) | |

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Avalanche Characteristics

| | | | |
|------------------------------|--|---------------------------|----|
| E_{AS} (Thermally limited) | Single Pulse Avalanche Energy ③ | 181 | mJ |
| E_{AS} (tested) | Single Pulse Avalanche Energy Tested Value ④ | 247 | |
| I_{AR} | Avalanche Current ② | See Fig. 14, 15, 24a, 24b | A |
| E_{AR} | Repetitive Avalanche Energy ② | | mJ |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|-----------------|-----------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case ⑤⑥ | — | 0.92 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ⑤ | — | 40 | |

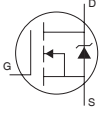
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|-------|------|-------|--|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.026 | — | V/°C | Reference to 25°C , $I_D = 1.0\text{mA}$ ② |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 1.9 | 2.3 | mΩ | $V_{GS} = 10V, I_D = 100A$ ⑤ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.2 | 3.0 | 3.9 | V | $V_{DS} = V_{GS}, I_D = 100\mu A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 1.0 | μA | $V_{DS} = 40V, V_{GS} = 0V$ |
| | | — | — | 150 | | $V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -20V$ |
| R_G | Internal Gate Resistance | — | 2.3 | — | Ω | |

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

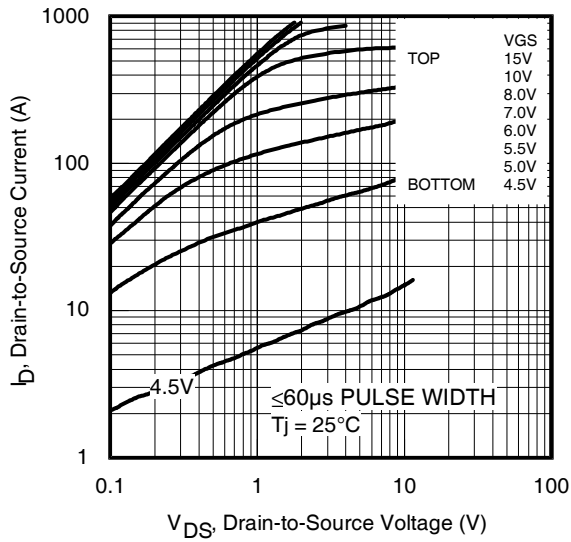
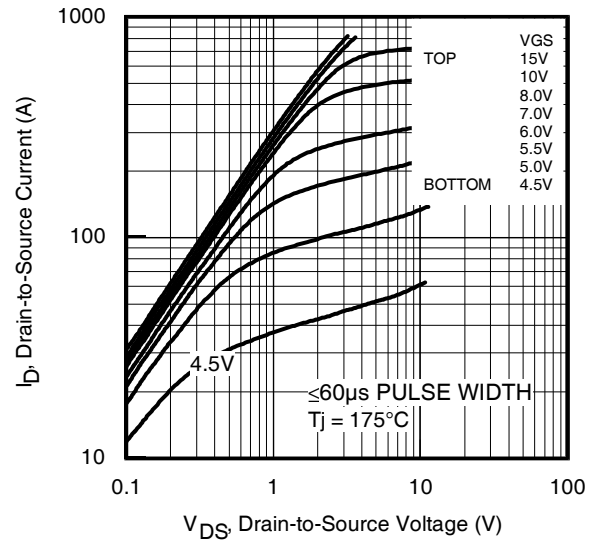
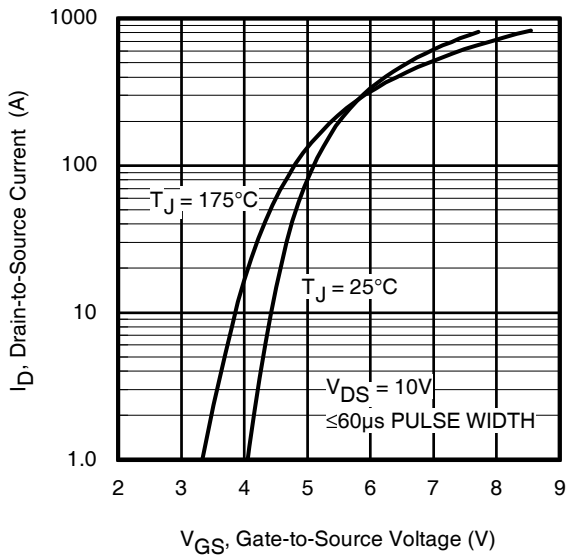
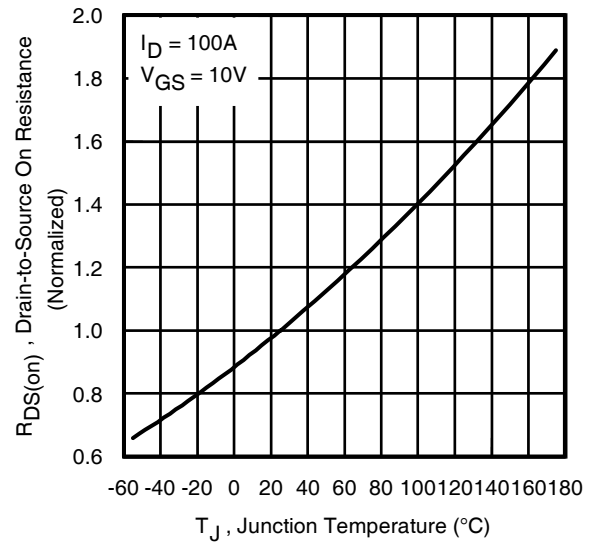
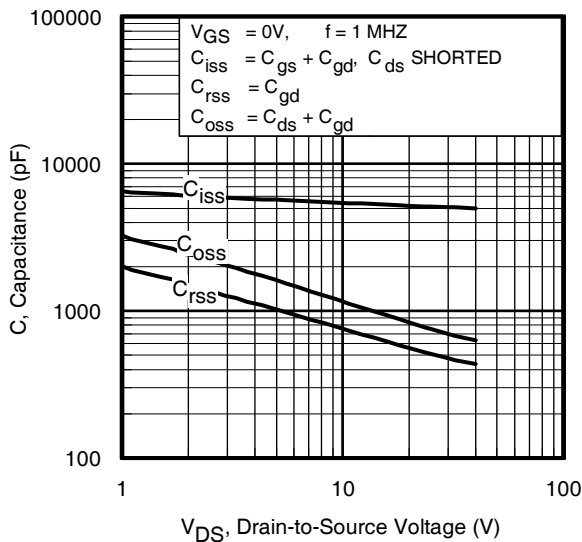
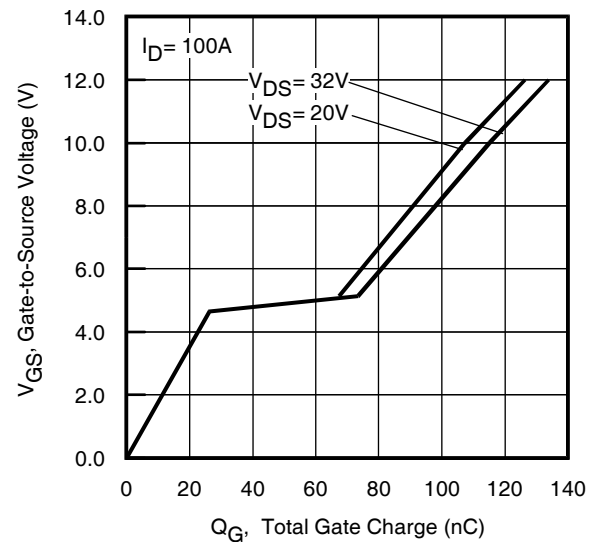
| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------|---|------|------|------|-------|--|
| g_{fs} | Forward Transconductance | 100 | — | — | S | $V_{DS} = 10V, I_D = 100A$ |
| Q_g | Total Gate Charge | — | 107 | 161 | nC | $I_D = 100A$ |
| Q_{gs} | Gate-to-Source Charge | — | 29 | — | | $V_{DS} = 20V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | 39 | — | | $V_{GS} = 10V$ ⑤ |
| Q_{sync} | Total Gate Charge Sync. ($Q_g - Q_{gd}$) | — | 68 | — | | $I_D = 100A, V_{DS} = 0V, V_{GS} = 10V$ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 14 | — | ns | $V_{DD} = 26V$ |
| t_r | Rise Time | — | 128 | — | | $I_D = 100A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 55 | — | | $R_G = 2.7\Omega$ |
| t_f | Fall Time | — | 77 | — | | $V_{GS} = 10V$ ⑤ |
| C_{iss} | Input Capacitance | — | 5193 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 754 | — | | $V_{DS} = 25V$ |
| C_{riss} | Reverse Transfer Capacitance | — | 519 | — | | $f = 1.0\text{MHz}$, See Fig. 5 |
| C_{oss} eff. (ER) | Effective Output Capacitance (Energy Related) | — | 878 | — | | $V_{GS} = 0V, V_{DS} = 0V$ to $32V$ ⑦, See Fig. 11 |
| C_{oss} eff. (TR) | Effective Output Capacitance (Time Related) | — | 1225 | — | | $V_{GS} = 0V, V_{DS} = 0V$ to $32V$ ⑧ |

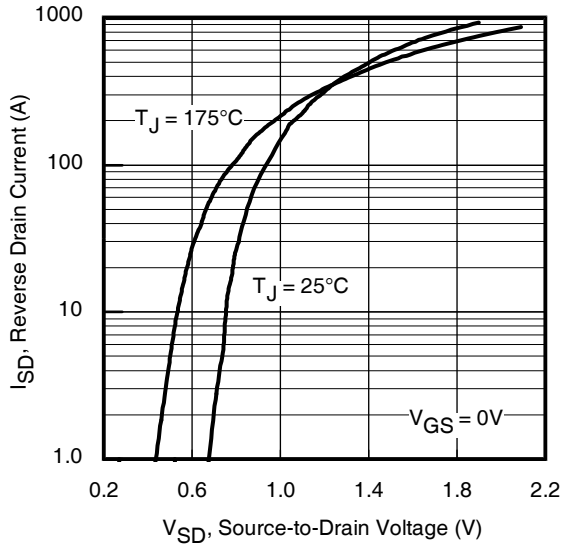
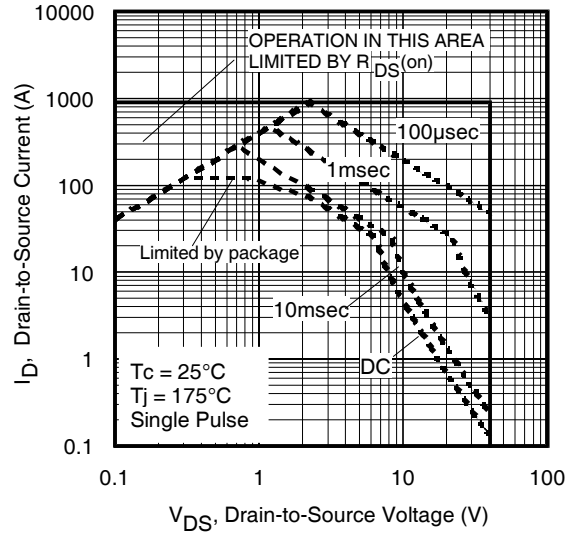
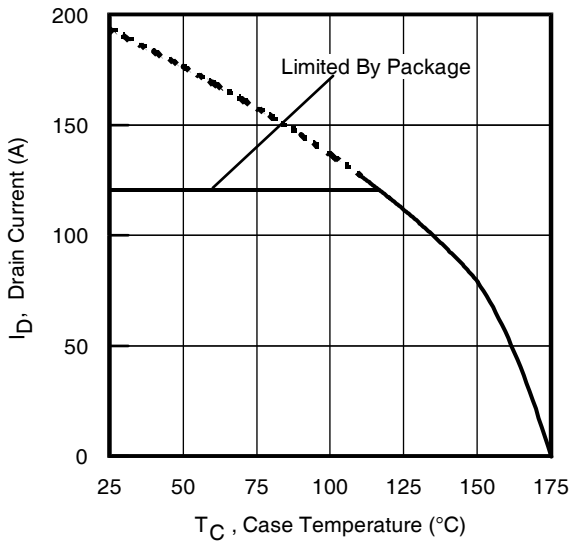
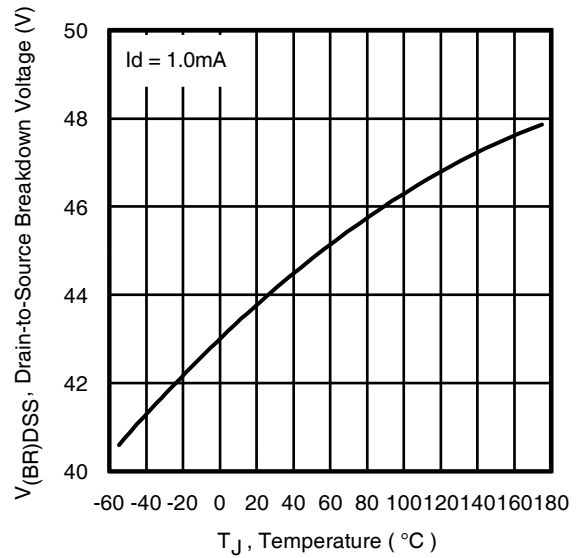
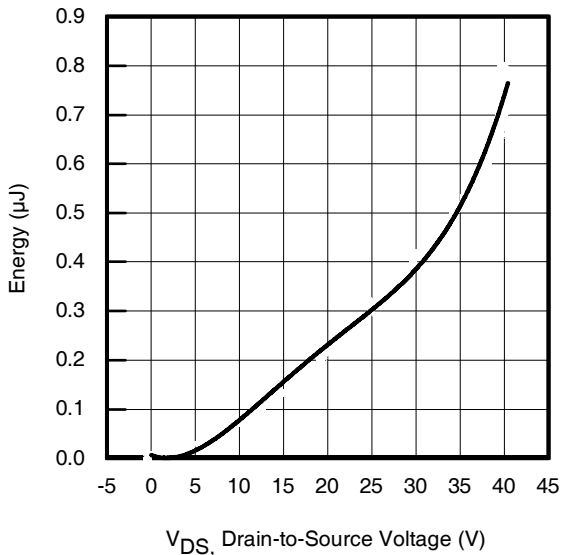
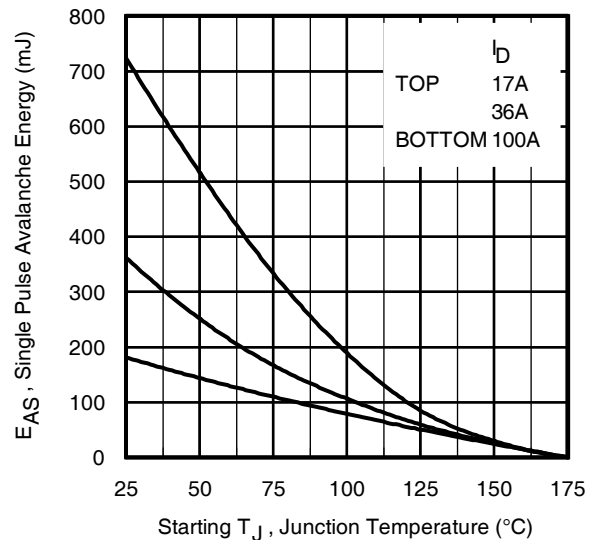
Diode Characteristics

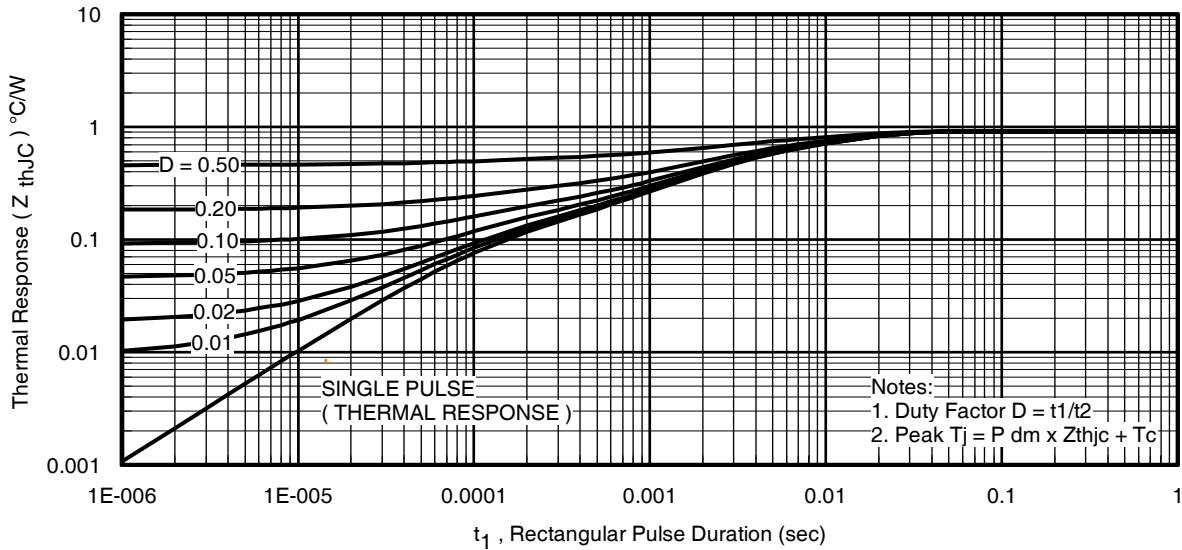
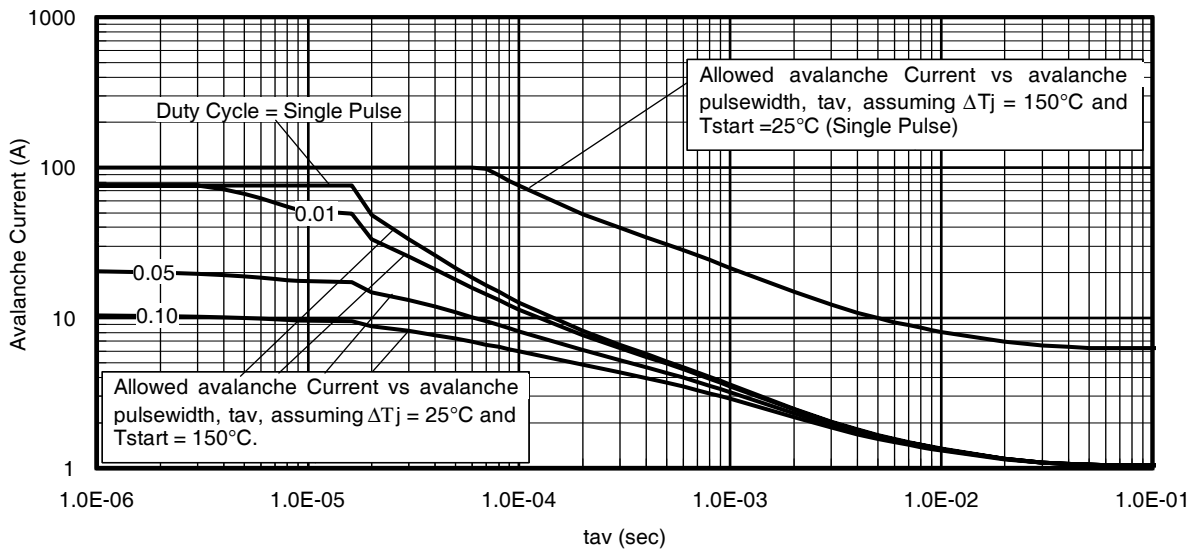
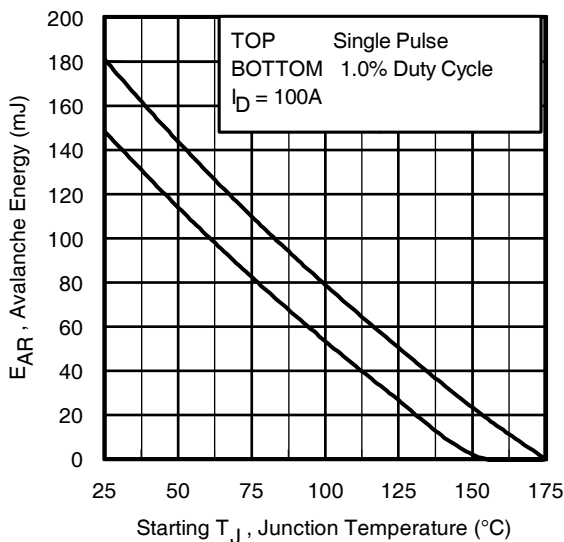
| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------|--|--|------|------------------|-------|--|
| I_S | Continuous Source Current (Body Diode) | — | — | 193 ^① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I_{SM} | Pulsed Source Current (Body Diode) ^② | — | — | 904 | | |
| V_{SD} | Diode Forward Voltage | — | 0.9 | 1.3 | V | $T_J = 25^\circ\text{C}$, $I_S = 100\text{A}$, $V_{GS} = 0\text{V}$ ^⑤ |
| dv/dt | Peak Diode Recovery ^③ | — | 1.7 | — | V/ns | $T_J = 175^\circ\text{C}$, $I_S = 100\text{A}$, $V_{DS} = 40\text{V}$ |
| t_{rr} | Reverse Recovery Time | — | 44 | — | ns | $T_J = 25^\circ\text{C}$ |
| | | — | 45 | — | | $T_J = 125^\circ\text{C}$ |
| Q_{rr} | Reverse Recovery Charge | — | 44 | — | nC | $T_J = 25^\circ\text{C}$ |
| | | — | 46 | — | | $T_J = 125^\circ\text{C}$ |
| I_{RRM} | Reverse Recovery Current | — | 1.9 | — | A | $T_J = 25^\circ\text{C}$ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.036\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 100\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 100\text{A}$, $di/dt \leq 1295\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{OSS} eff. (TR) is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{OSS} eff. (ER) is a fixed capacitance that gives the same energy as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_{θ} is measured at T_J approximately 90°C .
- ⑩ $R_{\theta JC}$ value shown is at time zero.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Typical C_{oss} Stored Energy

Fig 12. Maximum Avalanche Energy vs. Drain Current

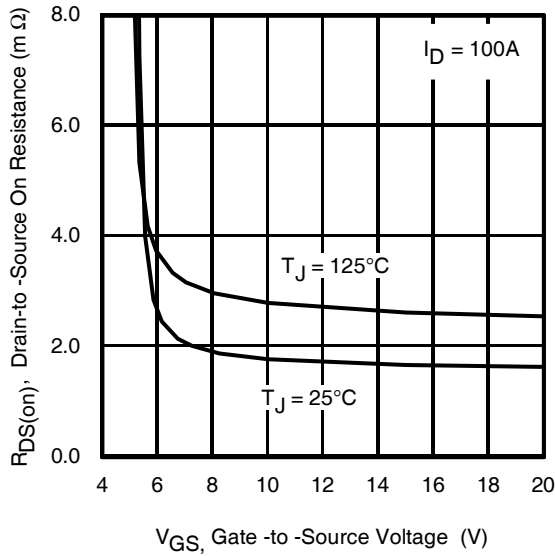
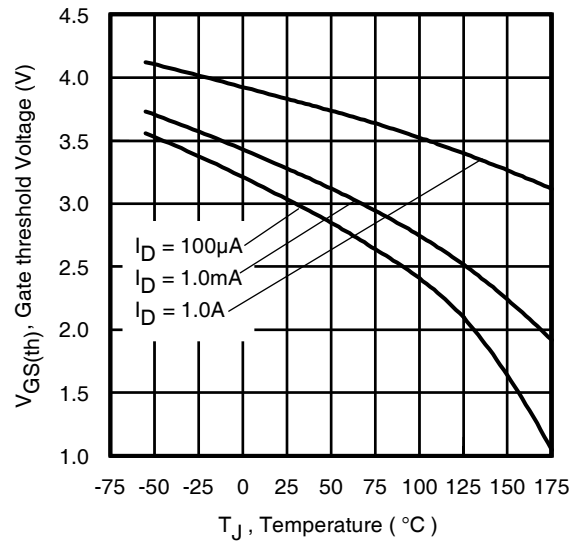
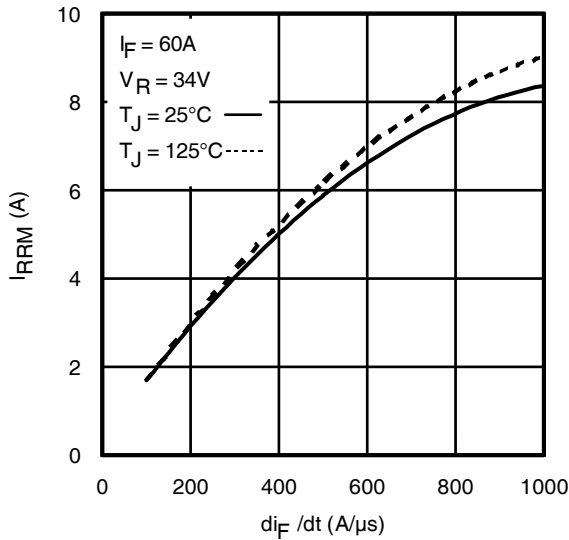
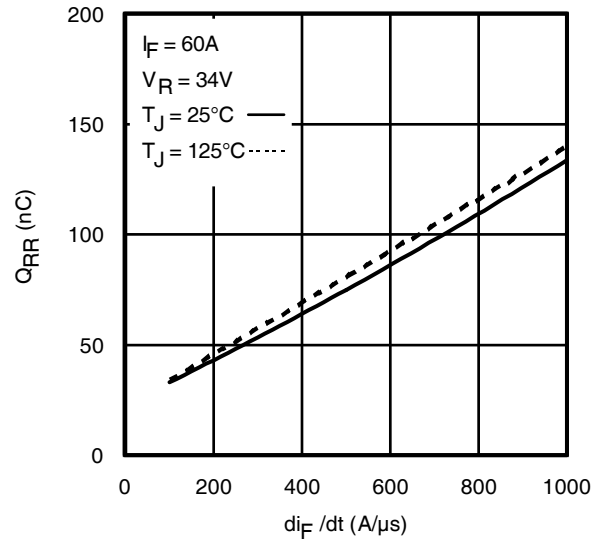
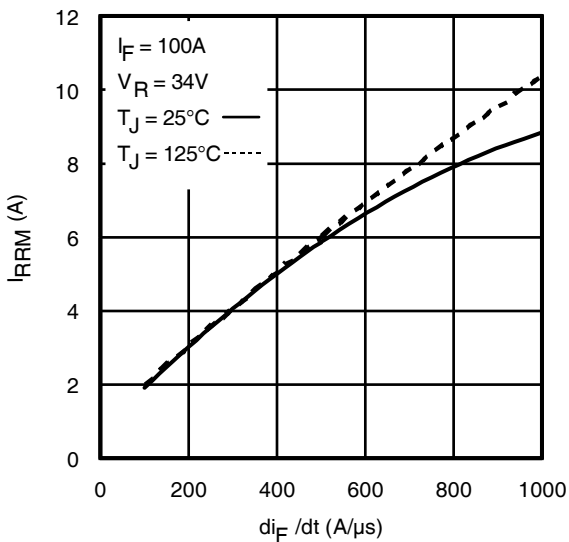
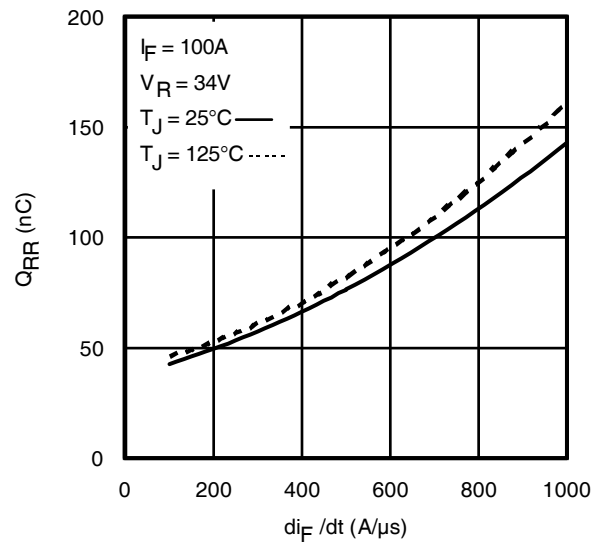

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature
Notes on Repetitive Avalanche Curves , Figures 14, 15
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 24a, 24b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig 16. On-Resistance vs. Gate Voltage

Fig 17. Threshold Voltage vs. Temperature

Fig. 18 - Typical Recovery Current vs. di_f/dt

Fig. 19 - Typical Stored Charge vs. di_f/dt

Fig. 20 - Typical Recovery Current vs. di_f/dt

Fig. 21 - Typical Stored Charge vs. di_f/dt

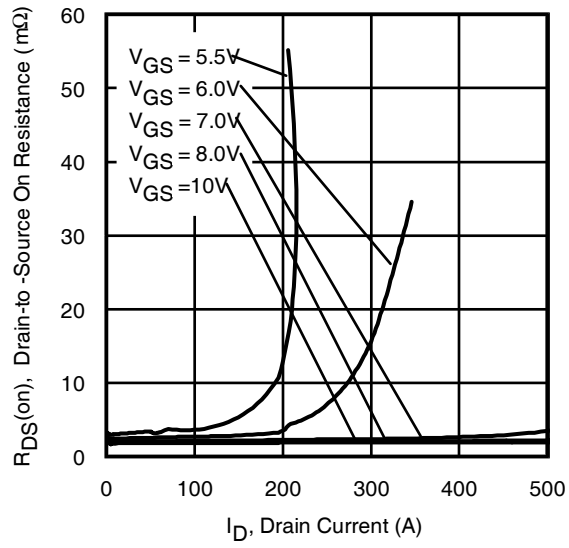
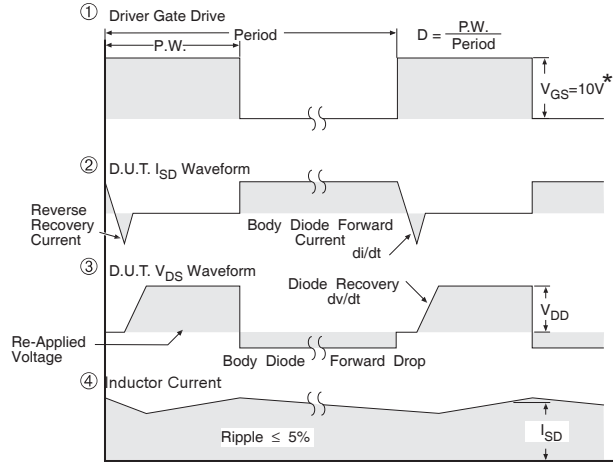
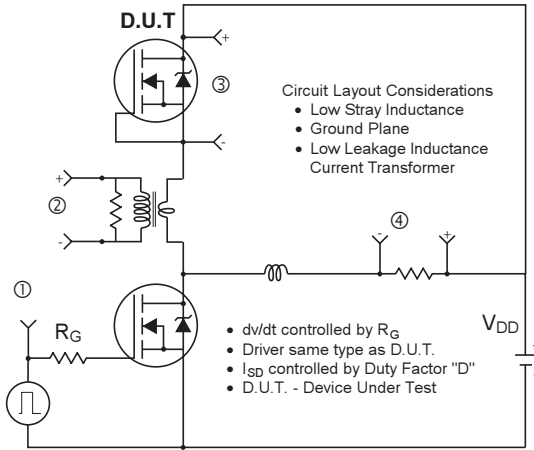


Fig 22. Typical On-Resistance vs. Drain Current



* $V_{GS} = 5V$ for Logic Level Devices

Fig 23. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

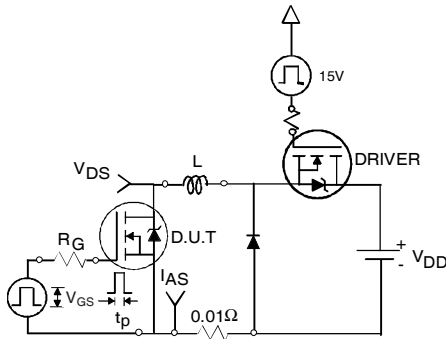


Fig 24a. Unclamped Inductive Test Circuit

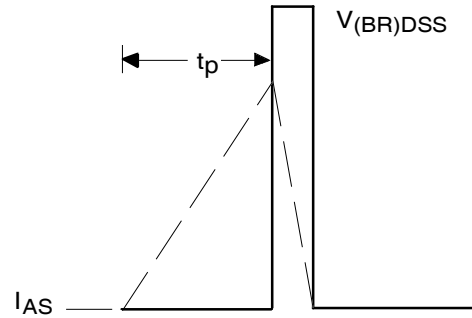


Fig 24b. Unclamped Inductive Waveforms

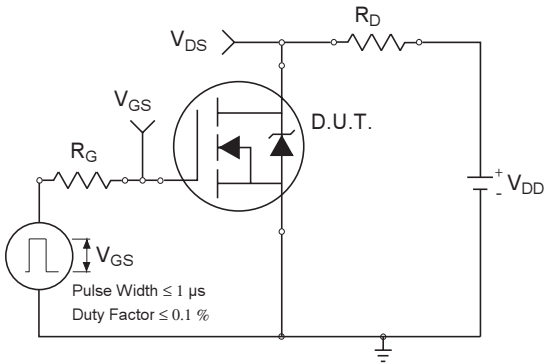


Fig 25a. Switching Time Test Circuit

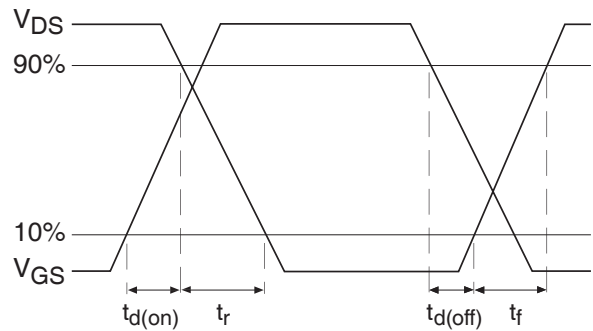


Fig 25b. Switching Time Waveforms

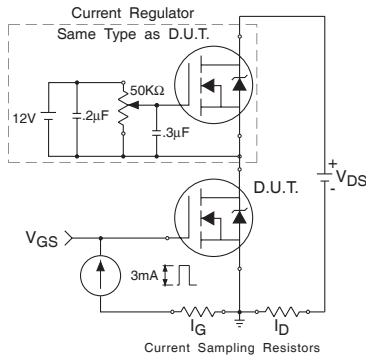


Fig 26a. Gate Charge Test Circuit

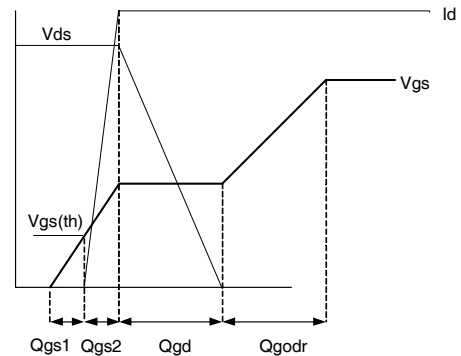
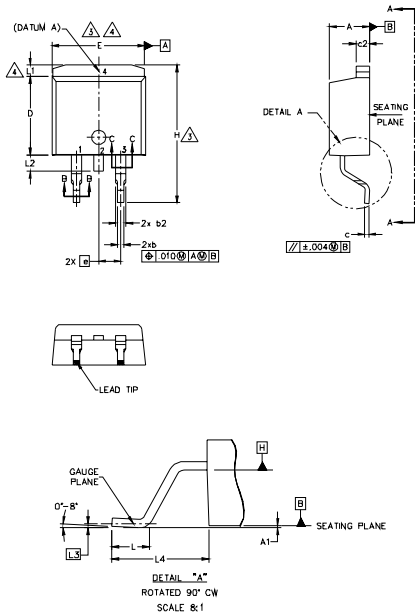


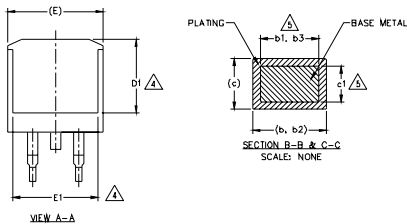
Fig 26b. Gate Charge Waveform

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | 5 |
| A1 | 0.00 | 0.254 | .000 | .010 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | 5 |
| c1 | 0.38 | 0.58 | .015 | .023 | |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | - | .270 | - | 4 |
| E | 9.65 | 10.67 | .380 | .420 | 3,4 |
| E1 | 6.22 | - | .245 | - | 4 |
| e | 2.54 BSC | | .100 BSC | | 4 |
| H | 14.61 | 15.88 | .575 | .625 | |
| L | 1.78 | 2.79 | .070 | .110 | |
| L1 | - | 1.65 | - | .066 | |
| L2 | - | 1.78 | - | .070 | |
| L3 | 0.25 BSC | | .010 BSC | | 4 |
| L4 | 4.78 | 5.28 | .188 | .208 | |



LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE

HEXFEET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

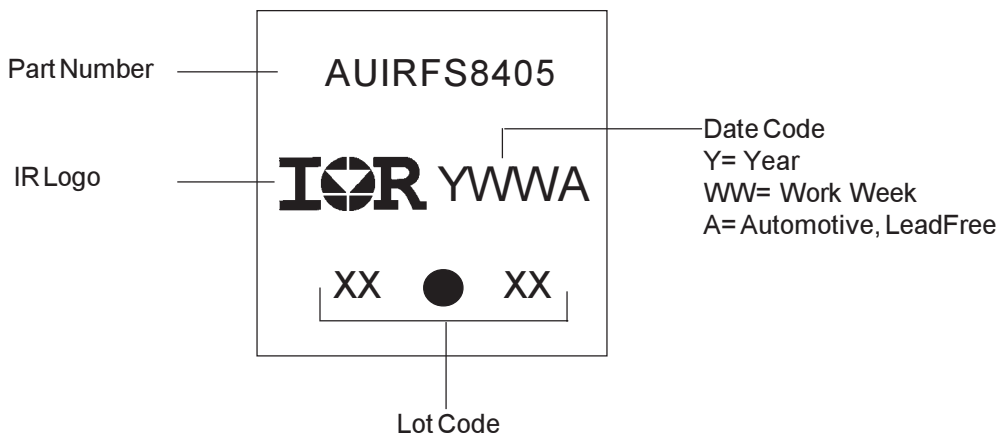
IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

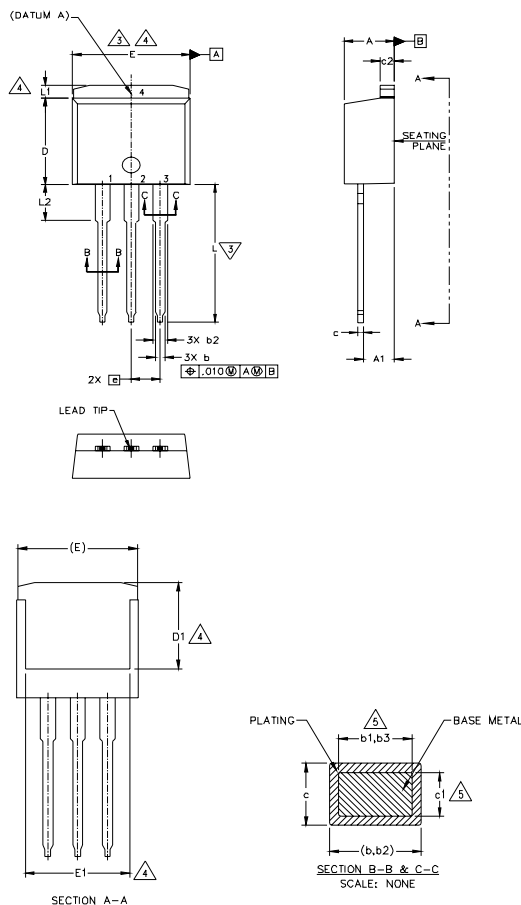
D²Pak (TO-263AB) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 2.03 | 3.02 | .080 | .119 | |
| b | 0.51 | 0.99 | .020 | .039 | 5 |
| b1 | 0.51 | 0.89 | .020 | .035 | |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | — | .270 | — | 4 |
| E | 9.65 | 10.67 | .380 | .420 | 3,4 |
| E1 | 6.22 | — | .245 | — | 4 |
| e | 2.54 BSC | | .100 BSC | | |
| L | 13.46 | 14.10 | .530 | .555 | |
| L1 | — | 1.65 | — | .065 | 4 |
| L2 | 3.56 | 3.71 | .140 | .146 | |

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION D1 AND c1 APPLY TO BASE METAL ONLY.
 6. CONTROLLING DIMENSION: INCH.
 7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

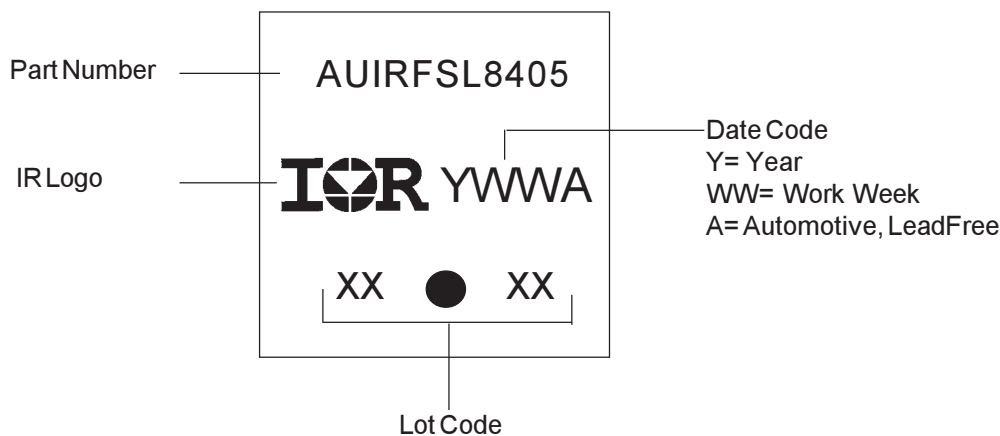
HEFFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

DIODES

- 1.- ANODE (NO DE) / OPEN (NO DE)
- 2.- CATHODE
- 3.- ANODE

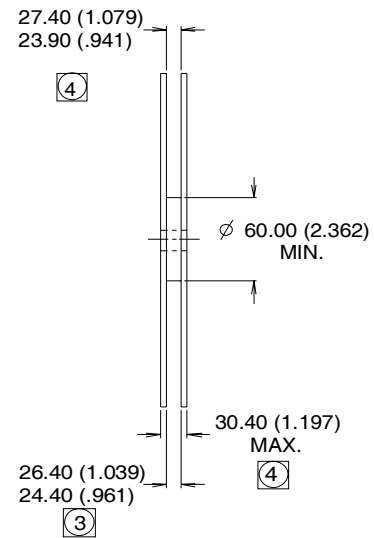
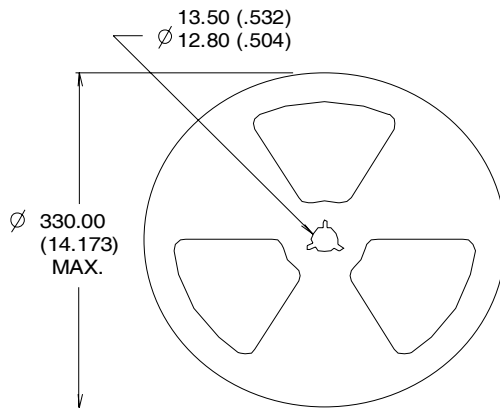
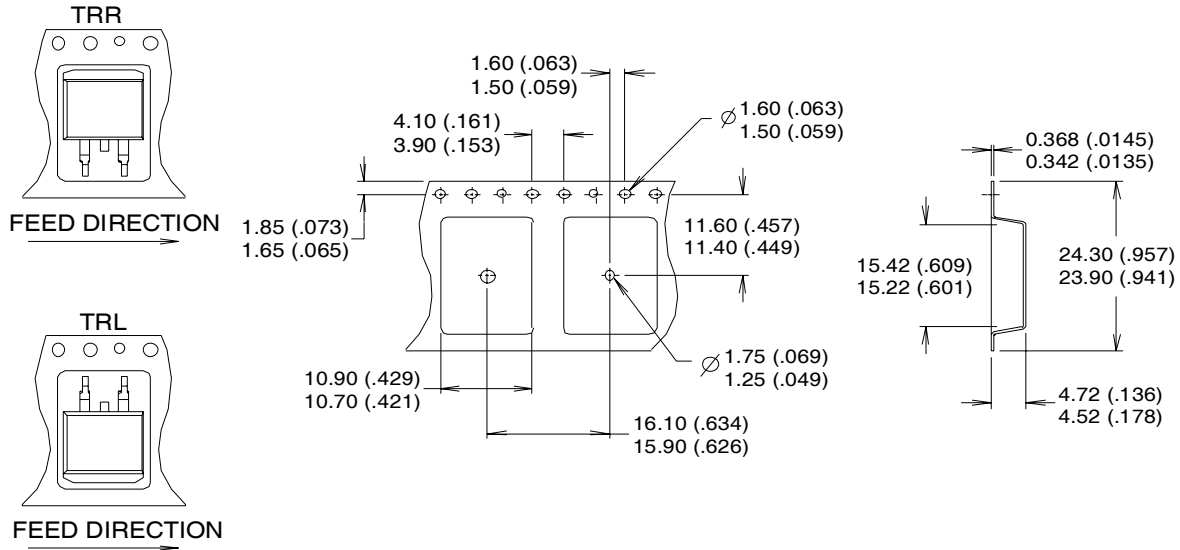
TO-262 Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Qualification Information[†]

| | | | |
|----------------------------|----------------------|---|------|
| Qualification Level | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| | | TO-262 | N/A |
| | | D ² PAK | MSL1 |
| ESD | Machine Model | Class M3 (+/- 400V) ^{††} AEC-Q101-002 | |
| | Human Body Model | Class H1C (+/- 2000V) ^{††} AEC-Q101-001 | |
| | Charged Device Model | Class C5 (+/- 2000V) ^{††} AEC-Q101-005 | |
| RoHS Compliant | | Yes | |

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>
^{††} Highest passing voltage.

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<http://www.irf.com/technical-info/>

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