W27C01

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Table of Contents-

W27C01

1. GENERAL DESCRIPTION

The W27C01 is a high speed, low power consumption Electrically Erasable and Programmable Read Only Memory organized as 131,072 x 8 bits. It requires only one supply in the range of 5.0V ±5% in normal read mode. The W27C01 provides an electrical chip erase function.
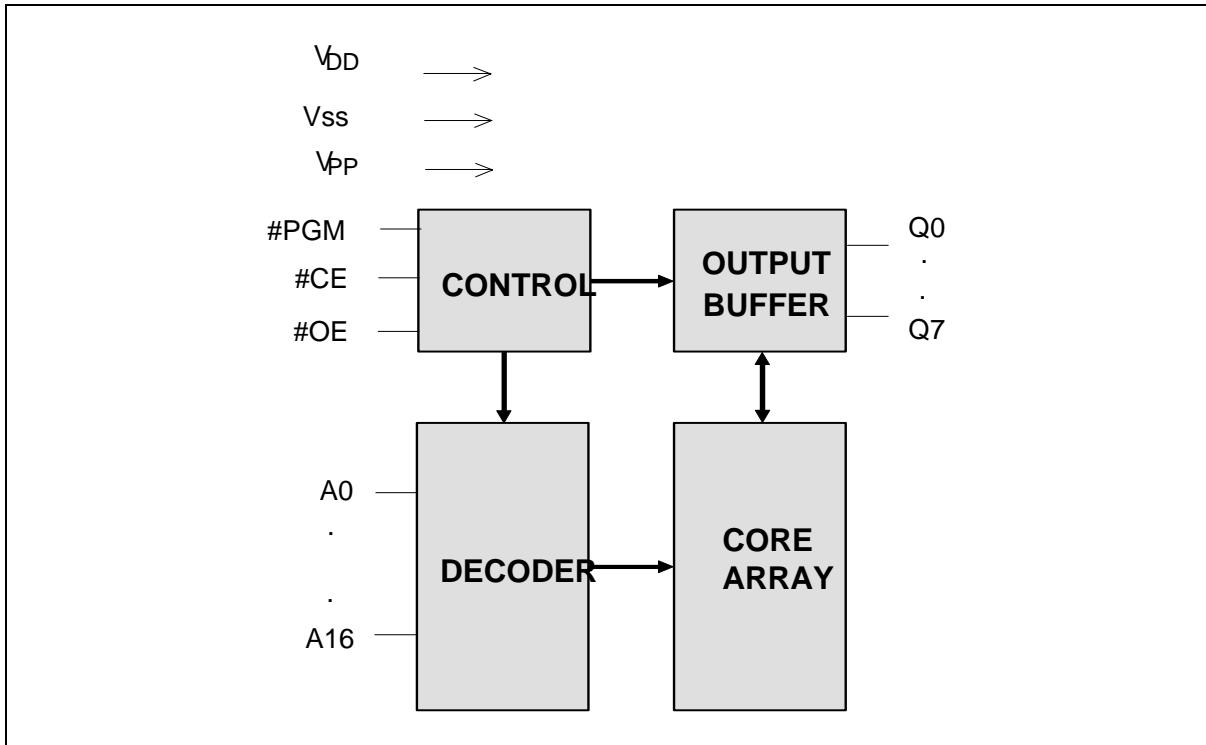
2. FEATURES

- Single power supply voltage: 5.0V ±5%

- High speed access time: 70 nS (max.)

- Read operating current: 30 mA (max.)

- Erase/Programming operating current: 30 mA (max.)

- Standby current: 20 μA (max.)

- +12V erase/programming voltage

- Fully static operation

- All inputs and outputs directly TTL/CMOS   compatible

- Three-state outputs

- Available packages: 32-pin 600 mil DIP, 32-lead PLCC and 32-lead STSOP

3. PIN CONFIGURATIONS

32-pin PDIP

Left	Pin		Pin	Right
Vpp	1		32	V DD
A16	2		31	#PGM
A15	3		30	NC
A12	4		29	A14
A7	5		28	A13
A6	6		27	A8
A5	7		26	A9
A4	8		25	A11
A3	9		24	#OE
A2	10		23	A10
A1	11		22	#CE
A0	12		21	Q7
Q0	13		20	Q6
Q1	14		19	Q5
Q2	15		18	Q4
Vss	16		17	Q3

32-lead PLCC

Top pins (left to right): A12 (4), A15 (3), A16 (2), Vpp (1), VDD (32), #PGM (31), NC (30)

Left pins (top to bottom): A7 (5), A6 (6), A5 (7), A4 (8), A3 (9), A2 (10), A1 (11), A0 (12), Q0 (13)

Bottom pins (left to right): Q1 (14), Q2 (15), Vss (16), Q3 (17), Q4 (18), Q5 (19), Q6 (20)

Right pins (top to bottom): A14 (29), A13 (28), A8 (27), A9 (26), A11 (25), #OE (24), A10 (23), #CE (22), Q7 (21)

32-lead STSOP

Left	Pin		Pin	Right
A11	1		32	#OE
A9	2		31	A10
A8	3		30	#CE
A13	4		29	Q7
A14	5		28	Q6
NC	6		27	Q5
#PGM	7		26	Q4
V DD	8		25	Q3
V PP	9		24	V SS
A16	10		23	Q2
A15	11		22	Q1
A12	12		21	Q0
A7	13		20	A0
A6	14		19	A1
A5	15		18	A2
A4	16		17	A3

4. BLOCK DIAGRAM

5. PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 − A16	Address Inputs
Q0 − Q7	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#PGM	Program Enable
VPP	Program/Erase Supply Voltage
VDD	Power Supply
Vss	Ground
NC	No Connection

6. FUNCTIONAL DESCRIPTION

Read Mode

Like conventional UVEPROMs, the W27C01 has two control functions and both of these produce data at the outputs.

#CE is for power control and chip select. #OE controls the output buffer to gate data to the output pins. When addresses are stable, the address access time (T_{ACC}) is equal to the delay from #CE to output (T_{CE}), and data are available at the outputs T_{OE} after the falling edge of #OE, if T_{ACC} and T_{CE} timings are met.

Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27C01 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

Erase mode is entered when V_{PP} is raised to V_{PE} (12V), $V_{DD} = V_{CE}$ (5V), #CE low, #OE high, A9 = V_{HH} (12V), A0 low, and all other address pins low and data input pins high. Pulsing #PGM low starts the erase operation.

Erase Verify Mode

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to "1" or not. The erase verify mode automatically ensures a substantial erase margin. This mode will be entered after the erase operation if $V_{DD} = V_{PE}$ (5V), #CE low, and #OE low, #PGM high.

Program Mode

Programming is performed exactly as it is in conventional UVEPROMs, and programming is the only way to change cell data from "1" to "0." The program mode is entered when V_{PP} is raised to V_{PP} (12V), $V_{DD} = V_{CP}$ (5V), #CE low, #OE high, the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing #PGM low starts the programming operation.

Program Verify Mode

All of the bytes in the chip must be verified to check whether they have been successfully programmed with the desired data or not. Hence, after each byte is programmed, a program verify operation should be performed. The program verify mode automatically ensures a substantial program margin. This mode will be entered after the program operation if $V_{PP} = V_{PP}$ (12V), #CE low, #OE low, and #PGM high.

Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When #CE high , erasing or programming of non-target chips is inhibited, so that except for the #CE, the W27C01 may have common inputs.

Standby Mode

The standby mode significantly reduces V_{DD} current. This mode is entered when #CE high. In standby mode, all outputs are in a high impedance state, independent of #OE and #PGM.

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Two-line Output Control

Since EPROMs are often used in large memory arrays, the W27C01 provides two control inputs for multiple memory connections. Two-line control provides for lowest possible memory power dissipation and ensures that data bus contention will not occur.

System Considerations

EPROM power switching characteristics require careful device decoupling. System designers are concerned with three supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by the falling and rising edges of #CE. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{DD} and Vss. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{DD} and Vss. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

7. TABLE OF OPERATING MODES

V_{DD} = 5.0V ±5%, Vpp = V_{PE} = V_{HH} = 12V, V_{CP} = V_{PE} = 5V, X = V_{IH} or V_{IL}

MODE	PINS							
	#CE	**#OE**	**#PGM**	**A0**	**A9**	**VDD**	**VPP**	**OUTPUTS**
Read	V_{IL}	V_{IL}	X	X	X	V_{DD}	V_{DD}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	X	V_{DD}	V_{DD}	High Z
Standby (TTL)	V_{IH}	X	X	X	X	V_{DD}	V_{DD}	High Z
Standby (CMOS)	V_{DD} ±0.3V	X	X	X	X	V_{DD}	V_{DD}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	X	X	V_{CP}	V_{PP}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{CP}	V_{PP}	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	V_{CP}	V_{PP}	High Z
Erase	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{PE}	V_{CP}	V_{PE}	FF (Hex)
Erase Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PE}	V_{PE}	D_{OUT}
Erase Inhibit	V_{IH}	X	X	X	X	V_{CP}	V_{PE}	High Z
Product Identifier-manufacturer	V_{IL}	V_{IL}	X	V_{IL}	V_{HH}	V_{DD}	V_{DD}	DA (Hex)
Product Identifier-device	V_{IL}	V_{IL}	X	V_{IH}	V_{HH}	V_{DD}	V_{DD}	01 (Hex)

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8. DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Operation Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
Voltage on all Pins with Respect to Ground Except V_{DD}, V_{PP} and A9 Pins	-0.5 to V_{DD} +0.5	V
Voltage on V_{DD} Pin with Respect to Ground	-0.5 to +7.0	V
Voltage on V_{PP} Pin with Respect to Ground	-0.5 to +14.5	V
Voltage on A9 Pin with Respect to Ground	-0.5 to +14.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9. CAPACITANCE

(V_{DD} = 5.0V ±5%, T_A = 25° C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	12	pF

10. READ OPERATION DC CHARACTERISTICS

(V_{DD} = 5.0V ±5%, T_A = 0 to 70° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = 0V to V_{DD}	-5	-	5	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0V to V_{DD}	-10	-	10	μA
Standby V_{DD} Current (TTL input)	I_{SB}	#CE = V_{IH}	-	-	1	mA
Standby V_{DD} Current (CMOS input)	I_{SB1}	#CE = V_{DD} ±0.2V	-	-	100	μA
V_{DD} Operating Current	I_{CC}	#CE=V_{IL}, I_{OUT} = 0 mA, f = 5 MHz	-	-	30	mA
V_{PP} Operating Current	I_{PP}	V_{PP} = V_{DD}	-	-	10	μA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.2	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.1 mA	2.4	-	-	V
V_{PP} Operating Voltage	V_{PP}	-	V_{DD} -0.7	-	V_{DD}	V

W27C01

Program/Erase DC Characteristics

(T_A = 25° C, V_{DD} = 5.0V ±5%, V_{HH} = 12V)

| PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = V_{IL} or V_{IH}	-10	-	10	μA
V_{DD} Program Current	I_{CP}	#CE = V_{IL}, #OE = V_{IH}, #PGM = V_{IL}	-	-	30	mA
V_{DD} Erase Current	I_{CE}	#CE = V_{IL}, #OE = V_{IH}, #PGM = V_{IL}, A9 = V_{HH}	-	-	30	mA
V_{PP} Program Current	I_{PP}	#CE = V_{IL}, #OE = V_{IH}, #PGM = V_{IL}	-	-	30	mA
V_{PP} Erase Current	I_{PE}	#CE = V_{IL}, #OE = V_{IH}, #PGM = V_{IL}, A9 = V_{HH}	-	-	30	mA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.4	-	5.5	V
Output Low Voltage (Verify)	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V
A9 Silicon I.D. Voltage	V_{ID}	-	11.5	12.0	12.5	V
A9 Erase Voltage	V_{ID}	-	11.75	12.0	14.25	V
V_{PP} Program Voltage	V_{PP}	-	11.75	12.0	12.25	V
V_{PP} Erase Voltage	V_{PE}	-	11.75	12.0	14.25	V
V_{DD} Supply Voltage (Program)	V_{CP}	-	4.5	5.0	5.5	V
V_{DD} Supply Voltage (Erase)	V_{CE}	-	4.5	5.0	5.5	V
V_{DD} Supply Voltage (Erase Verify)	V_{PE}	-	-	5.0	-	V
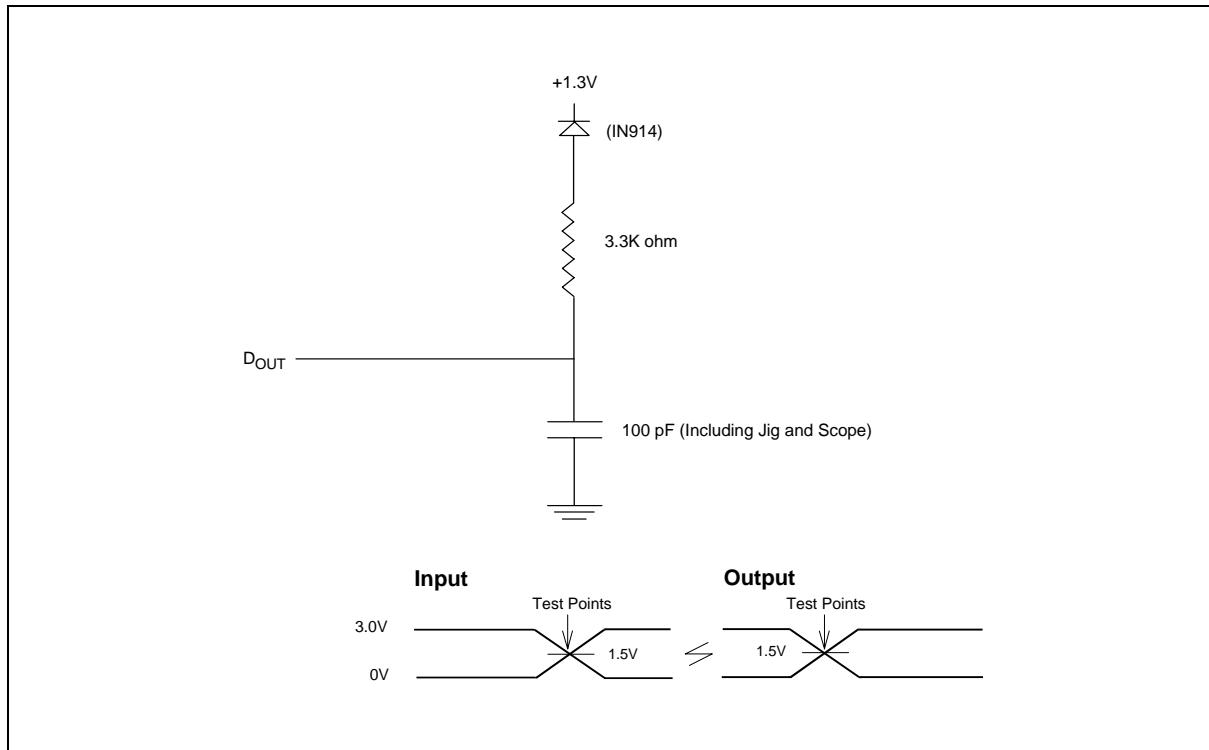
Note: V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

11. AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V/1.5V
Output Load	C_L = 100 pF, I_{OH}/I_{OL} = -0.1 mA/1.6 mA for Read
	I_{OH}/I_{OL} = -0.4 mA/2.1 mA for Program/Erase

AC Test Load and Waveforms

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12. READ OPERATION AC CHARACTERISTICS

(VDD = 5.0V ±5%, TA = 0 to 70° C)

PARAMETER	SYMBOL	W27C01-70		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	70	-	nS
Chip Enable Access Time	TCE	-	70	nS
Address Access Time	TACC	-	70	nS
Output Enable Access Time	TOE	-	30	nS
#OE High to High-Z Output	TDF	-	25	nS
Output Hold from Address Change	TOH	0	-	nS

Note: VDD must be applied simultaneously or before VPP and removed simultaneously or after VPP.

13. AC PROGRAMMING/ERASE CHARACTERISTICS
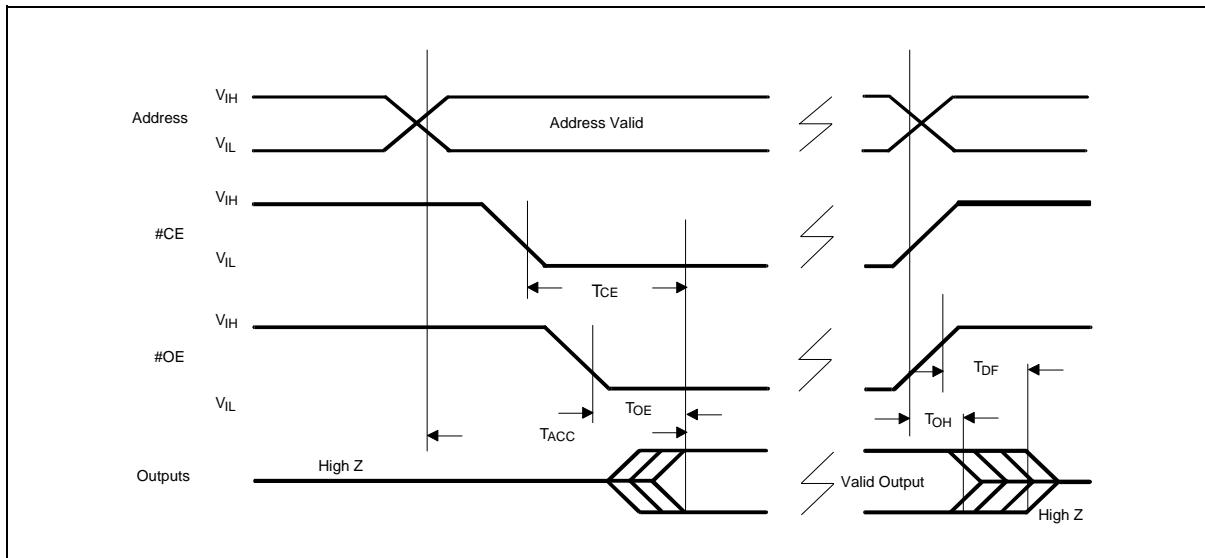
(VDD = 5.0V ±5%, TA = 25° C)

| PARAMETER	SYMBOL	LIMITS			UNIT
		MIN.	TYP.	MAX.	
VPP Setup Time	TVPS	2.0	-	-	μS
Address Setup Time	TAS	2.0	-	-	μS
Data Setup Time	TDS	2.0	-	-	μS
#PGM Program Pulse Width	TPWP	95	100	105	μS
#PGM Erase Pulse Width	TPWE	95	100	105	mS
Data Hold Time	TDH	2.0	-	-	μS
#OE Setup Time	TOES	2.0	-	-	μS
Data Valid from #OE	TOEV	-	-	150	nS
#OE High to Output High Z	TDFP	0	-	130	nS
Address Hold Time after #PGM High	TAH	0	-	-	μS
Address Hold Time (Erase)	TAHE	2.0	-	-	μS
#CE Setup Time	TCES	2.0	-	-	μS
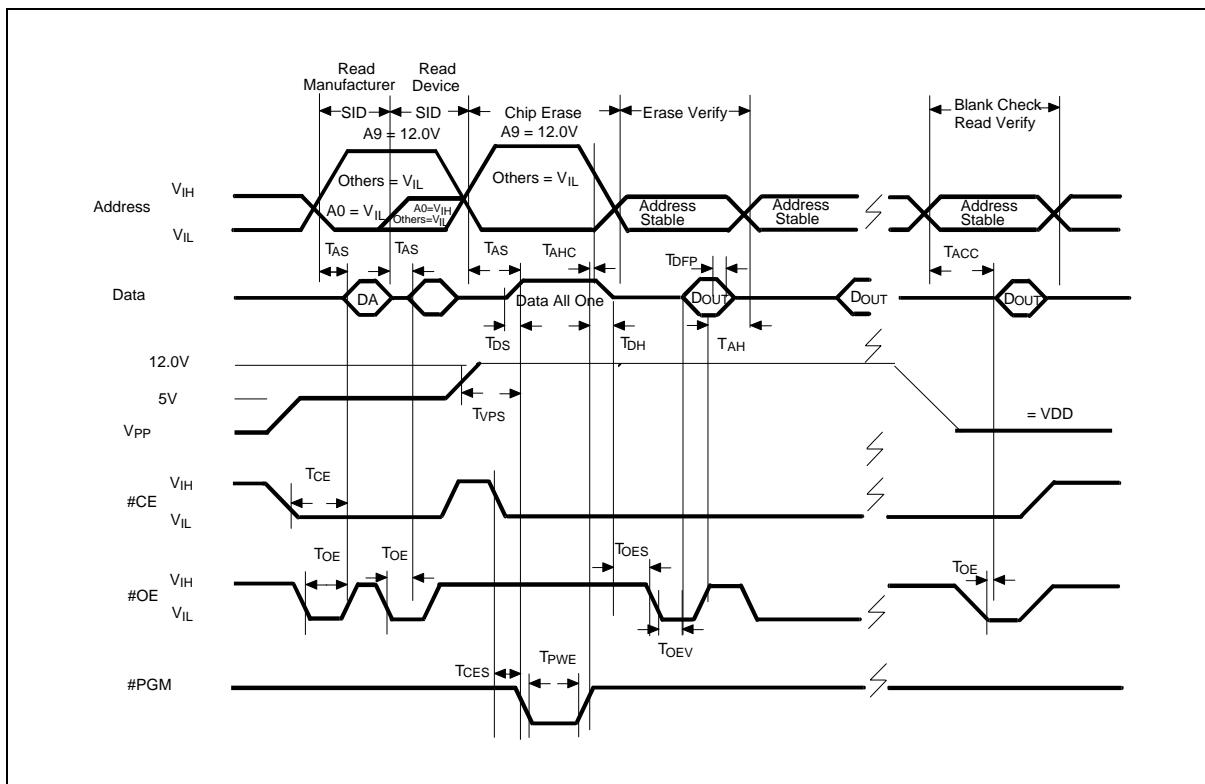
Note: VDD must be applied simultaneously or before VPP and removed simultaneously or after VPP.

## 14. TIMING WAVEFORMS

AC Read Waveform
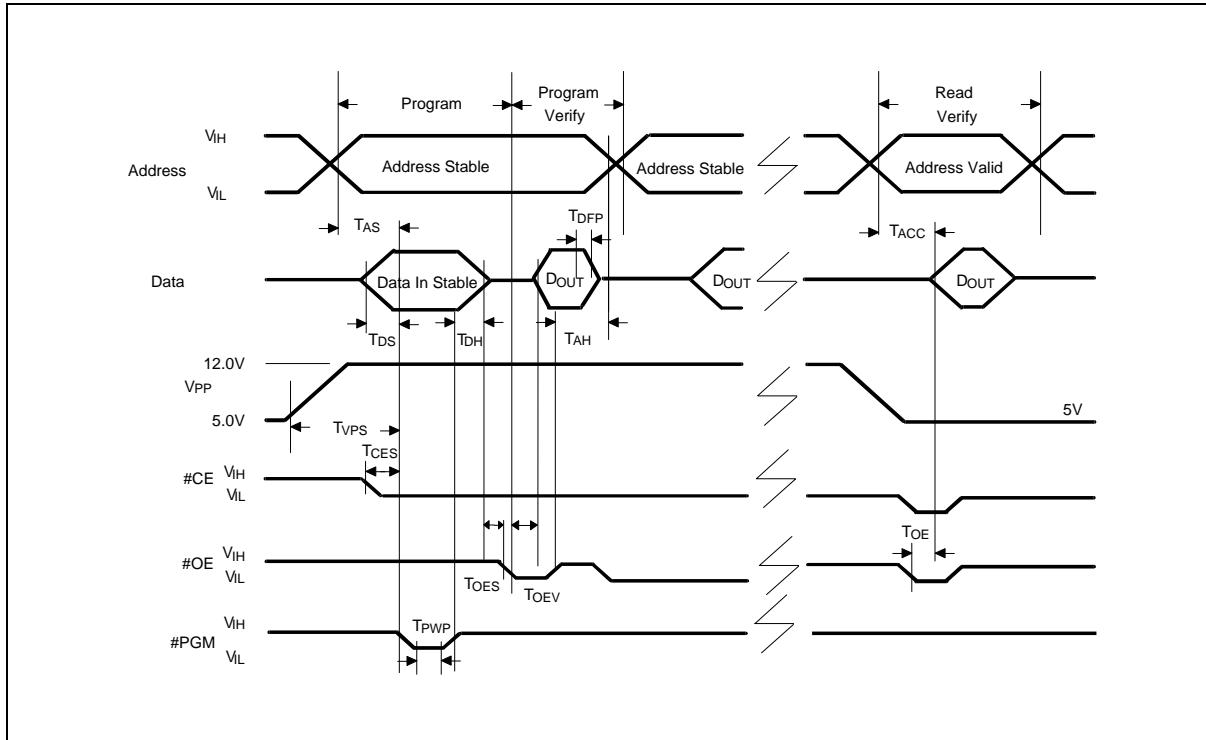
Erase Waveform
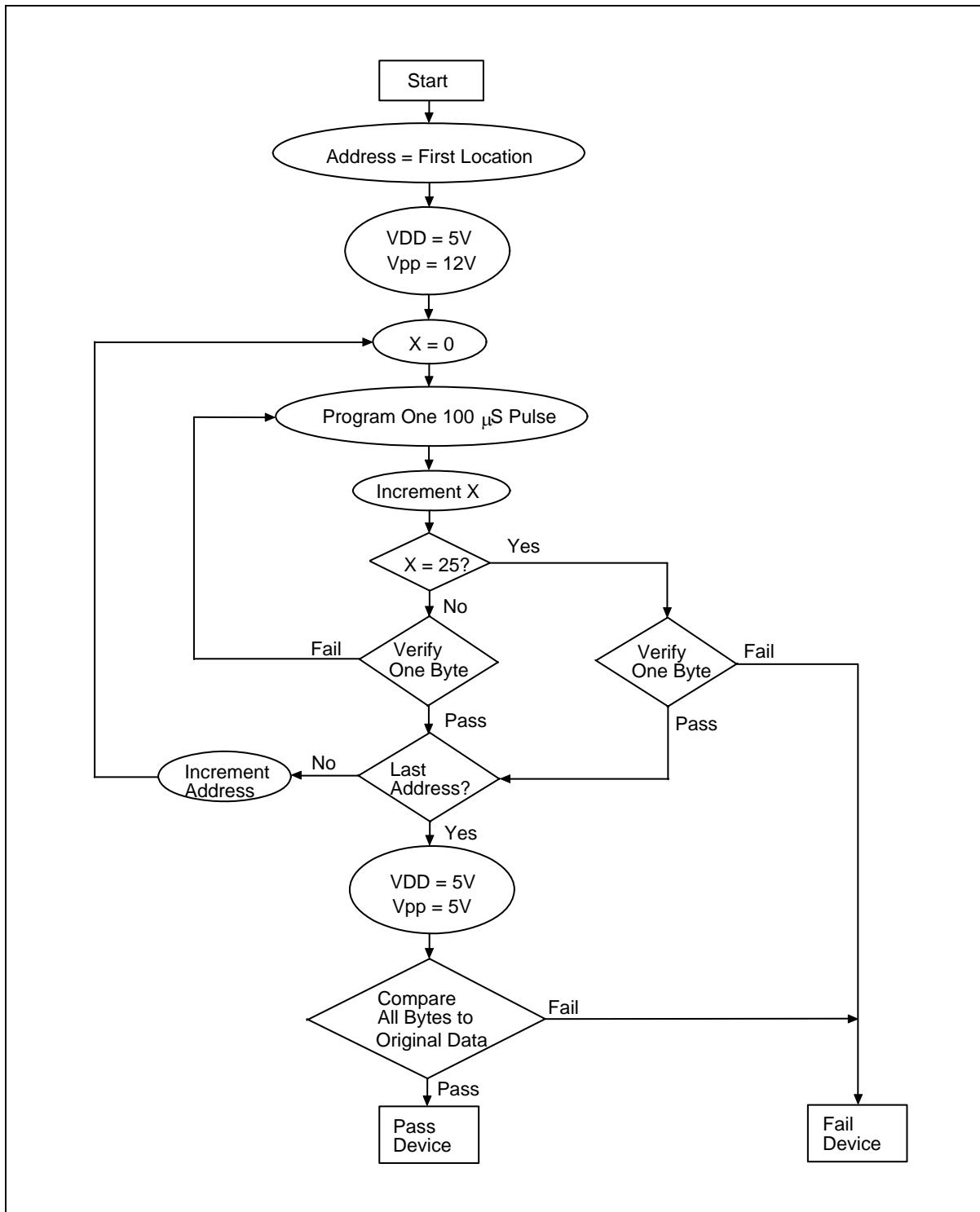
Timing Waveforms, Continued
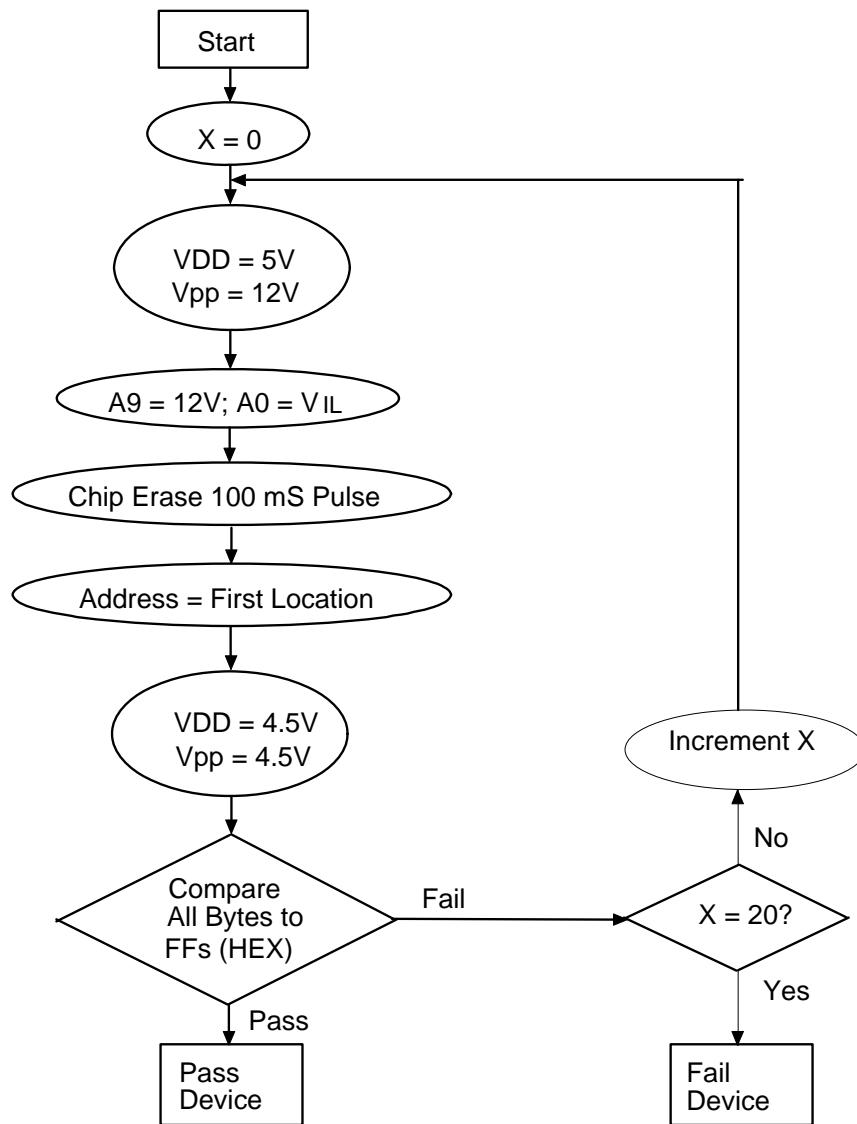
Programming Waveform

15. SMART PROGRAMMING ALGORITHM

```
                    ┌──────────┐
                    │  Start   │
                    └────┬─────┘
              ⬭ Address = First Location ⬭
              ⬭   VDD = 5V / Vpp = 12V   ⬭
                    ⬭   X = 0   ⬭
              ⬭ Program One 100 μS Pulse ⬭
                    ⬭ Increment X ⬭
                    ◇  X = 25?  ◇ — Yes
                       No
              ◇ Verify One Byte ◇ — Fail      ◇ Verify One Byte ◇ — Fail
                    Pass                              Pass
              ◇ Last Address? ◇ — No → ⬭ Increment Address ⬭
                    Yes
              ⬭   VDD = 5V / Vpp = 5V   ⬭
              ◇ Compare All Bytes to Original Data ◇ — Fail
                    Pass
              ┌──────────┐              ┌──────────┐
              │  Pass    │              │  Fail    │
              │  Device  │              │  Device  │
              └──────────┘              └──────────┘
```

16. SMART ERASE ALGORITHM

```
                    ┌──────────┐
                    │  Start   │
                    └────┬─────┘
                         ↓
                    ( X = 0 )
                         ↓
                  ( VDD = 5V
                    Vpp = 12V )
                         ↓
              ( A9 = 12V; A0 = V_IL )
                         ↓
          ( Chip Erase 100 mS Pulse )
                         ↓
          ( Address = First Location )
                         ↓
                  ( VDD = 4.5V
                    Vpp = 4.5V )
                         ↓
        ◇ Compare All Bytes to FFs (HEX) ◇ ──Fail──→ ◇ X = 20? ◇
                         │                              │No → ( Increment X )
                        Pass                           Yes
                         ↓                              ↓
                  ┌──────────┐                   ┌──────────┐
                  │  Pass    │                   │  Fail    │
                  │  Device  │                   │  Device  │
                  └──────────┘                   └──────────┘
```

17. ORDERING INFORMATION
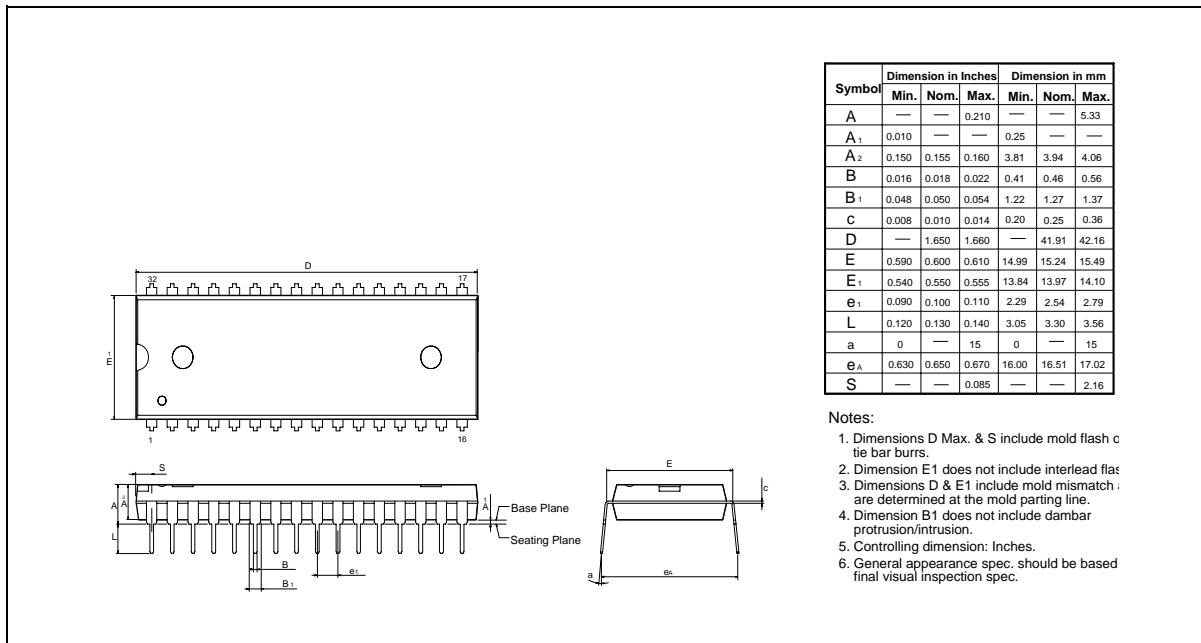
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (μA)	PACKAGE
W27C01-70	70	30	20	600 mil DIP
W27C01P-70	70	30	20	32-Lead PLCC
W27C01Q-70	70	30	20	32-Lead STSOP
W27C01-70Z	70	30	20	600 mil DIP lead free

Notes:
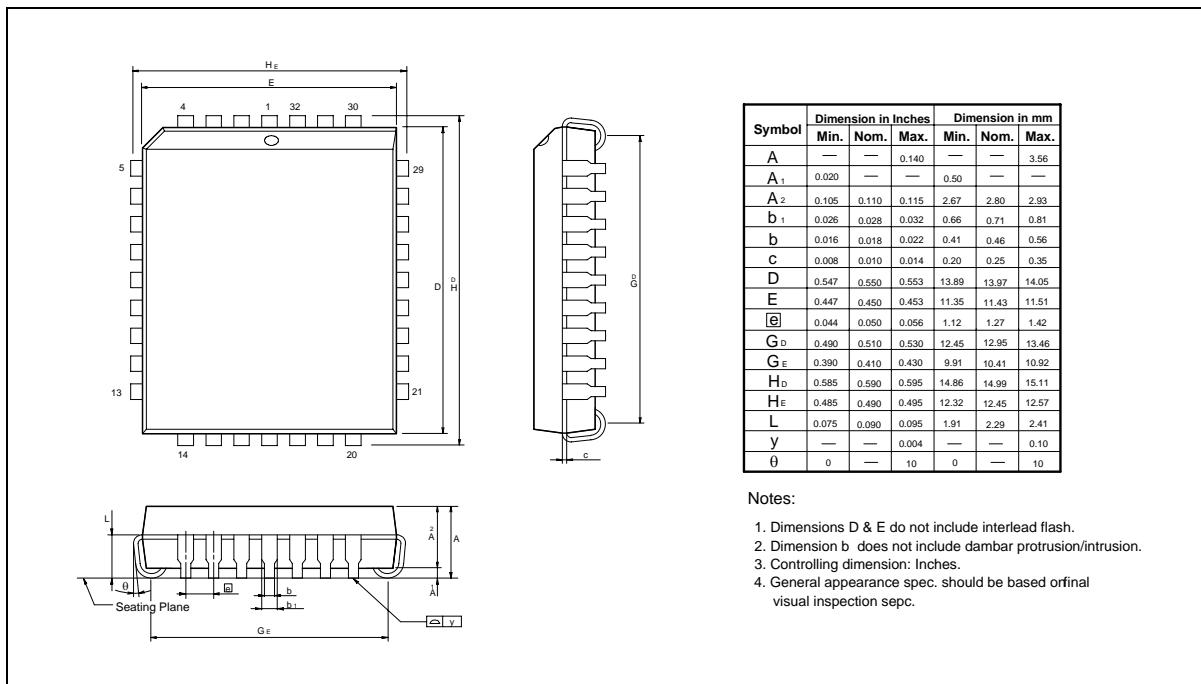
1. Winbond reserves the right to make changes to its products without prior notice.

2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

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18. PACKAGE DIMENSIONS

32-pin P-DIP

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based final visual inspection spec.

32-lead PLCC

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0	—	10	0	—	10

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based or final visual inspection sepc.

Package Dimensions, continued

32-lead STSOP (8 x 14 mm)

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A$_1$	0.002		0.006	0.05		0.15
A$_2$	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H$_D$		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L$_1$		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0	3	5	0	3	5

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19. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Apr. 2001	-	Initial Issued
A2	April 15, 2002	All	Modify by W27E01 except V_{DD} = 5.0V $\pm$5%
		5	Modify by W27E01 except V_{IH} = 2.2V (min.) for read operation.
A3	April 14, 2005	15	Adding important notice
A4	Oct. 31, 2006	17	Adding W27C01-70Z lead free package

Important Notice

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