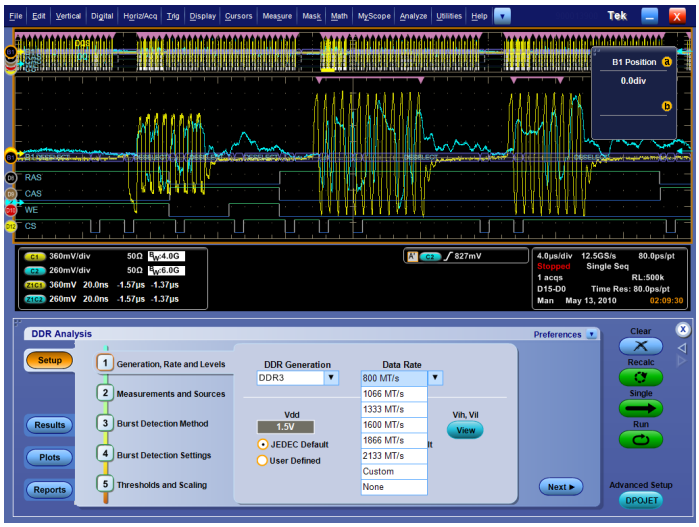
DDR Memory Bus Electrical Validation and Analysis Software



Features & Benefits

- Auto-configuration Wizard Guides Easy Setup and Test Configuration
- Analyze All Read/Write Bursts in the Entire Acquisition
- Plot DQS and DQ Eye Diagrams for Reads and Writes
- Perform JEDEC Conformance Tests with Pass/Fail Limits
- Use Chip Select to Qualify Multi-rank Measurements
- Navigate and Time Stamp Reads and Writes in an Acquired Record using Search and Mark
- Use Pinpoint Triggering, Visual Trigger, and DPX to Quickly Identify Infrequent Anomalies
- Easily Move between Conformance-test and Analysis/Debug Tools
- Automatically Produce Consolidated Reports with Pass/Fail Information, Statistical Measurement Results, and Test-setup Information
- On MSO70000, Use Address/Command Bus to Precisely Qualify Read and Write Bursts or Other Events
- On MSO70000, Perform Bus Timing Measurements on the Address/Command Bus

Applications

- DDR1
- DDR2
- DDR3
- LPDDR
- LPDDR2
- GDDR5

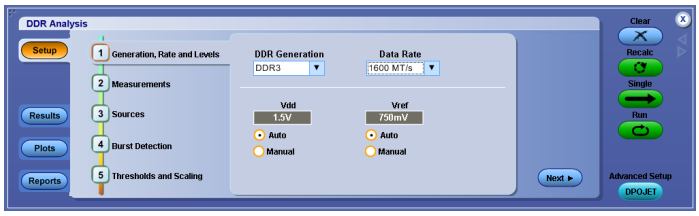
Option DDRA accelerates the analysis, validation, and conformance testing of memory systems based on JEDEC Test Recommendations.

A single license of DDRA provides support for multiple generations of the JEDEC DDR Standard; beginning with DDR1, DDR2, DDR3, while including DDR derivatives LPDDR, LPDDR2, and GDDR5. Option DDRA supports the common data rates in these standards alongside custom data rates up to and beyond 2133 MT/s. Whether you are doing intensive signal integrity analysis or debugging a specific memory transaction, DDRA will speed your ability to trigger on and identify read and write bursts in the acquired data record and then perform parametric measurements on the signals of interest.

DDRA Wizard for Easy Test Selection and Configuration

The wizard consolidates Tektronix experience and expertise in DDR testing into a simple, easy-to-follow test selection interface. The user selects which DDR technology, speed grade, and measurement group (reads, writes, clocks, address, and control lines) they are testing, using check boxes to select some or all measurements in a category. DDRA can then automate oscilloscope scale selection, DQ and DQS level selections, and threshold detection, then automate burst identification using search and mark. Search and mark (for read/write measurements) data is used to identify and separate all read vs. write bursts across the entire acquisition and qualify measurement zones for use by DPOJET Advanced Jitter and Eye Analysis. DPOJET will generate an eye diagram of the data and perform JEDEC standard measurements qualified on read or write bursts. Measurement configurations and JEDEC pass/fail limits are automatically applied for the selected measurements. Every edge in each identified burst is measured, then measurement results are included in statistics and plots for a complete analysis of the acquired waveform.

Tektronix®



DDR Analysis Menu

JEDEC-conforming Measurements and Conformance Testing

DDR Specification	Conformance
DDR	JESD79E (May 2005)
DDR2	JESD79-2F (November 2009)
DDR3	JESD79-3D (July 2010)
LPDDR	JESD209A (February 2009)
LPDDR2	JESD209-2E (April 2011)
GDDR5	JESD212 (December 2009)

Comprehensive Measurements for JEDEC Conformance Testing

Option DDRA adds a long list of JEDEC-specific measurements to the rich toolset of generic jitter, timing, and signal-quality measurements already present in DPOJET. In addition to the measurements shown below (for DDR3 in this example), Option DDRA also covers other application standards like DDR1, DDR2, LPDDR, LPDDR3, and GDDR5. DDRA also performs de-rating of Setup and Hold pass/fail limits based on the result of slew rate measurements, as stipulated by JEDEC in the test specs for DDR2 and DDR3 (JESD79-2F, JESD79-3D as of this writing).

Easily Switch between Conformance Testing and Advanced Debug Tools

DDRA gives you the option to easily switch between conformance testing and advanced analysis and debug modes. The power of the DPOJET analysis engine allows you flexibility to reconfigure existing measurements or add new measurements not specifically required by JEDEC and to create new user-specified test limits. You can also use features like logging, filters, histograms, and time trends in addition to the information produced by the DDRA wizard.

Fast Fault Identification using Pinpoint® Triggers and DPX Technology

In addition to all of the measurement and analysis tools that DDRA offers, you can use Pinpoint® triggering and DPX® to find infrequent signal events. Pinpoint® triggering allows you to trigger on reads or writes so that only relevant bursts can be shown. Once you have set the hardware triggering on a read or write condition, you can use DPX®, the industry's highest waveform acquisition rate for signal integrity testing and to determine specific DDR read/write signal characteristics. DPX® enables quick identification of infrequent events by using a color-graded display to see both frequent and infrequent waveform events, such as areas where there is bus contention, reflections, or system timing issues. New Visual Trigger feature now adds additional tools for setting precise trigger conditions to capture specific bit patterns or other waveform events, based on keep-in and keep-out areas.

JEDEC Measurements Supported for DDR3

Write Bursts	**Clock(Diff)**	Vix(ac)DQS
Data Eye Width	tCH(abs)	VSEH(AC)DQS#
Data Eye Height	tCH(avg)	VSEH(AC)DQS
Differential DQS	tCK(abs)	VSEH(DQS#)
InputSlew-Diff-Fall(DQS)	tCK(avg)	VSEH(DQS)
InputSlew-Diff-Rise(DQS)	tCL(abs)	VSEL(AC)DQS#
tDH-Diff(base)	tCL(avg)	VSEL(AC)DQS
tDH-Diff(derated)	tDVAC(CK)	VSEL(DQS#)
tDQSH	tERR	VSEL(DQS)
tDQSL	tJIT(cc)	**DQS (Single Ended, Read)**
tDQSS-Diff	tJIT(duty)	AC-OvershootArea(DQ)
tDS-Diff(base)	tJIT(per)	AC-UndershootArea(DQ)
tDS-Diff(derated)	**Clock(Single Ended)**	AC-Overshoot(DQ)
tDSH-Diff	AC-Overshoot(CK#)	AC-Undershoot(DQ)
tDSS-Diff	AC-Overshoot(CK)	AC-OvershootArea(DQS)
tDVAC(DQS)	AC-OvershootArea(CK#)	AC-UndershootArea(DQS)
Single Ended DQS	AC-OvershootArea(CK)	AC-Overshoot(DQS)
tDIPW-SE	AC-Undershoot(CK#)	AC-Undershoot(DQS)
tDQSS-SE	AC-Undershoot(CK)	AC-OvershootArea(DQS#)
tDSH-SE	AC-UndershootArea(CK#)	AC-UndershootArea(DQS#)
tDSS-SE	AC-UndershootArea(CK)	AC-Overshoot(DQS#)
Slew Rate DQ	Vix(ac)CK	AC-Undershoot(DQS#)
Slew Rate-Hold-Rise(DQ)	VSEH(AC)CK#	**Precharge**
Slew Rate-Hold-Fall(DQ)	VSEH(AC)CK	tRP(ACT)
Slew Rate-Setup-Rise(DQ)	VSEH(CK#)	tRP(MRS)
Slew Rate-Setup-Fall(DQ)	VSEH(CK)	**Address/Command Measurements**
tWPRE	VSEL(AC)CK#	AC-Overshoot
tWPST	VSEL(AC)CK	AC-OvershootArea
Read Bursts	VSEL(CK#)	AC-Undershoot
Data Eye Width	VSEL(CK)	AC-UndershootArea
Data Eye Height	**DQS(Single Ended)**	InputSlew-Diff-Fall(CK)
Differential DQS	AC-OvershootArea(DQ)	InputSlew-Diff-Rise(CK)
SRQdiff-Fall(DQS)	AC-UndershootArea(DQ)	Slew Rate-Hold-Fall(Addr/Cmd)
SRQdiff-Rise(DQS)	AC-Overshoot(DQ)	Slew Rate-Hold-Rise(Addr/Cmd)
tDQSCK-Diff	AC-Undershoot(DQ)tDSH	Slew Rate-Setup-Fall(Addr/Cmd)
tDQSQ-Diff	AC-Overshoot(DQS#)	Slew Rate-Setup-Rise(Addr/Cmd)
tQH	AC-Overshoot(DQS)	tIH(base)
tDVAC(DQS)	AC-OvershootArea(DQS#)	tIH(derated)
SRQdiff-Fall(CK)	AC-OvershootArea(DQS)	tIPW-High
SRQdiff-Rise(CK)	AC-Undershoot(DQS#)	tIPW-Low
tRPRE	AC-Undershoot(DQS)	tIS(base)
tPST	AC-UndershootArea(DQS#)	tIS(derated)
	AC-UndershootArea(DQS)	

Additional Capabilities using a Performance MSO (Mixed-Signal Oscilloscope)

The MSO70000 Series Performance MSOs allow you to probe more signals on the DDR bus and to trigger on and view specific bus events. Up to 16 digital channels can be used to view logic states of command and address signals such as RAS, CAS, WE, CE, CS, etc. Signal integrity of these 16 inputs can be analyzed using the iCapture™ multiplexing feature, which allows any of the digital input signals to be internally routed to one of the scope's four analog channels. Measurements involving command-bus cycle timing can also be analyzed using the bus-decode features of the MSO and DDRA software.

Full Bus Analysis using Logic Analyzer and Oscilloscope

When full protocol analysis or probing of the entire memory bus is required, a logic analyzer can provide this additional capability. The TLA7000 Series logic analyzers can also be linked with Tektronix oscilloscopes to provide an integrated test setup using tools such as iCapture mentioned above. This eliminates the need for double probing and allows full analog capture of any signals probed by the logic analyzer. In addition, the iView™ display interface allows transfer of the oscilloscope data to the logic analyzer display, so that data from both instruments are analyzed and time-aligned on one display screen.

Characteristics

Bandwidth Recommendations for Each DDR Standard

DDR Type	Maximum Data Rate (JEDEC)	Clock Rate	5th Harmonic of Clock	Max SE Slew Rate (JEDEC)	Typical Signal Swing	Oscilloscope Rise Time 10% - 90%*1	Recommended Oscilloscope BW*2
DDR	400 MT/s	200 MHz	1 GHz	5 V/ns	1.8 V	89 ps	4 GHz
DDR2	800 MT/s	400 MHz	2 GHz	5 V/ns	1.25 V	62 ps	6 GHz
DDR3	2133 MT/s	1066 MHz	5.3 GHz	5 V/ns	1.0 V	49 ps	8 GHz
GDDR5	5 GT/s	2.5 GHz	12.5 GHz	N/A	0.8 V	18 ps	20 GHz*3

*1 For 3% maximum error on rise-time measurement.

*2 For less stringent applications, a one-step reduction in scope bandwidth may be acceptable.

*3 Based on 5 GT/s system; lower BW scope may suffice for lower data rates.

Ordering Information

DDRA

DDR Memory Bus Electrical Validation and Analysis Oscilloscope Software.

To order on a new DPO5000, MSO5000, DPO7000, DPO70000, DSA70000*4, or MSO70000 Series:

Order	Description
Opt. DDRA	Preinstall on a new DPO5000*5, MSO5000*5, DPO7000*5, DPO70000*5, DSA70000, or MSO70000*5 Series oscilloscope
DPOFL-DDRA	DDR Memory Technology Analysis Package – Floating License

*4 Note: Opt. DJA and ASM are standard on the DSA70000 Series oscilloscopes.

*5 Note: Opt. ASM (Advanced Event Search and Mark) and Opt. DJA (DPOJET) are required.

To upgrade an existing DPO5000, MSO5000, DPO7000, DPO70000, DSA70000, or MSO70000 Series:

Order	Description
DPO-UP DDRA	Upgrade to Option DDRA (requires Opt. ASM and DJA)
DPO-UP DJAE	Upgrade MSO/DPO5000 Series with DPOJET Jitter and Eye Diagram Analysis (Opt. DJA)
DPO-UP DJAM	Upgrade DPO7000 with DPOJET Jitter and Eye Diagram Analysis (Opt. DJA)
DPO-UP DJAH	Upgrade DPO70404 - DPO70804 or MSO70404 - MSO70804 with DPOJET Jitter and Eye Diagram Analysis (Opt. DJA)
DPO-UP DJAU	Upgrade DPO71254 - DPO73304 or MSO71254 - MSO72004 with DPOJET Jitter and Eye Diagram Analysis (Opt. DJA)
DPO-UP DJUP	DJA DPOJET software for scopes with both TDSJIT3 and TDSRTE licenses

Note: Software is supplied on the internal hard drive of the DPO5000, MSO5000, DPO7000, DPO70000, DSA70000, and MSO70000 Series oscilloscopes. User documentation (online or user manual) is part of the oscilloscope documentation.

To order a floating license for an existing DPO5000, MSO5000, DPO7000, DPO70000, DSA70000, or MSO70000 Series:

Order	Description
DPOFL-DDRA	DDR Memory Technology Analysis Package – Floating License
DPOFL-DJA	DPOJET Jitter and Eye Diagram Analysis – Floating License

Recommended Accessories

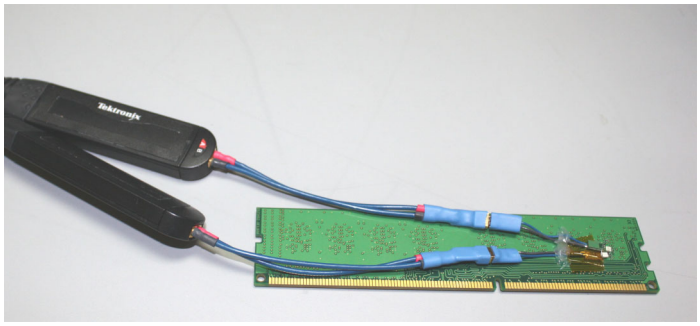
Order	Description
P7500 Series	TriMode™ Differential Probe
020-2955-xx	Micro-coax Tips (TriMode) for P7500 Probes
020-3022-xx	Micro-coax Tips (TriMode) for P7500 Probes*6
020-2954-xx	Socket Cable for P7500 Probes
P6780	Differential Logic Probe for MSO70000
TDP3500	Differential Probe for MSO/DPO5000 and DPO7000 Series Oscilloscopes
Recommended Nexus Technology Accessories	
NEX-DDR3MP78BSC	BGA Interposer for DDR3 x4/x8-solder Version
NEX-DDR3MP78BSCSK	BGA Interposer for DDR3 x4/x8-socket Version
NEX-DDR3MP96BSC	BGA Interposer for DDR3 x16-solder Version
NEX-DDR3MP96BSCSK	BGA Interposer for DDR3 x16-socket Version
NEX-DDR2MP60BSC	BGA Interposer for DDR2 x4/x8-solder Version
NEX-DDR2MP60BSCSK	BGA Interposer for DDR2 x4/x8-socket Version
NEX-DDR2MP84BSC	BGA Interposer for DDR2 x16-solder Version
NEX-DDR2MP84BSCSK	BGA Interposer for DDR2 x16-socket Version
Note: For more detailed information contact http://www.nexustechnology.com	

*6 For use with BGA Interposers only.

BGA Interposer probing solution for DDR2/DDR3

TLA7000 Series logic analyzer and Logic Probes Connection to the oscilloscope through Analog Mux. See www.tektronix.com/logic_analyzers

P7500 Series TriMode™ probe.



020-2955-xx Micro-Coax tips soldered to DIMM.

CE

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

Contact Tektronix:

ASEAN / Australasia (65) 6356 3900

Austria 00800 2255 4835*

Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777

Belgium 00800 2255 4835*

Brazil +55 (11) 3759 7627

Canada 1 800 833 9200

Central East Europe and the Baltics +41 52 675 3777

Central Europe & Greece +41 52 675 3777

Denmark +45 80 88 1401

Finland +41 52 675 3777

France 00800 2255 4835*

Germany 00800 2255 4835*

Hong Kong 400 820 5835

India 000 800 650 1835

Italy 00800 2255 4835*

Japan 81 (3) 6714 3010

Luxembourg +41 52 675 3777

Mexico, Central/South America & Caribbean 52 (55) 56 04 50 90

Middle East, Asia, and North Africa +41 52 675 3777

The Netherlands 00800 2255 4835*

Norway 800 16098

People's Republic of China 400 820 5835

Poland +41 52 675 3777

Portugal 80 08 12370

Republic of Korea 001 800 8255 2835

Russia & CIS +7 (495) 7484900

South Africa +41 52 675 3777

Spain 00800 2255 4835*

Sweden 00800 2255 4835*

Switzerland 00800 2255 4835*

Taiwan 886 (2) 2722 9622

United Kingdom & Ireland 00800 2255 4835*

USA 1 800 833 9200

* European toll-free number. If not accessible, call: +41 52 675 3777

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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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