OKI Semiconductor

PEDL86V7668-01
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ML86V7668 Preliminary

NTSC/PAL/SECAM Digital Video Decoder

GENERAL DESCRIPTION

The ML86V7668 is an LSI that converts NTSC, PAL and SECAM analog video signals into the YCbCr standard digital format defined by ITU-R recommendations BT.601/BT.656 and RGB digital data.
The device has two built-in 10-bit A/D converter channels and can accept composite video or S-video signal as input.
The composite video signal is separated into a luminance signal and chrominance signals by a 2-dimensional Y/C separation filter (2-line or 3-line adaptive comb filter) and are then converted to a general-purpose video data format.
In addition to the asynchronous sampling that is a special feature of Oki decoders, video signals can also be sampled using digital PLL for line lock clock sampling.
Further, due to the built-in pixel position correction circuit and the FIFO for correcting the pixel count, the video jitter that can be a problem with asynchronous sampling is eliminated and jitter-free output data is ensured.

USES AND APPLICATION EXAMPLES

The ML86V7668 is an IC that can be used as an interface for video signal input of any digital video processing system. The device can be operated with a digital PLL line lock clock for applications where image quality is of utmost importance. Further, for application where sync speed is important, such as switching between multiple input channels, an asynchronous clock allows high-speed synchronous operation.

Application Examples

- TVs and TV reception equipment
  Panel TVs such as TFT/PDP, PC TVs, digital TVs, set top boxes for receiving TV broadcasts
- Video recording equipment
  DVD-R/W, HDD recorders, digital VTRs, digital video cameras, and digital cameras
- Monitoring systems
  Multi-display equipment, long-playing video recording equipment, and transmission equipment for remote monitoring
- PC peripheral equipment
  Video capture boards, video editing equipment, and internet monitoring cameras

FEATURES

Input Section

- Accepts NTSC/PAL/SECAM composite video signals and S-video signals
- 4 composite inputs or 1 composite input + 3 S-video inputs can be connected
- Built-in clamp circuits and video amps
- Built-in 10-bit A/D converters (2 channels)
- Switchable between line lock clock sampling mode and asynchronous sampling mode
- Supported operating mode : Pixel frequency (system clock)
  NTSC/PAL/SECAM ITU-R BT.601 : 13.5 MHz (27 MHz)
  NTSC Square Pixel : 12.272727 MHz (24.545454 MHz)

Digital Processing Section

- 2-dimensional Y/C separation using an adaptive comb filter
  NTSC/PAL system: 2-line or 3-line adaptive comb filter
  For SECAM, the trap filter is used.
- Recognition of data in the VBI period (closed caption, CGMS, WSS) and function of reading from I^2C-bus (detection possible in all operating modes)
- Copy protection (e.g., macrovision AGC and color stripe) detection
- Capable of decoding specially standardized signals such as NTSC443, PAL-NC, M, and 60
  Automatic determinations can also be made partially by register settings.
- Built-in AGC/ACC circuits (automatic luminance level control/automatic color level control)
- Automatic NTSC/PAL/SECAM recognition (only in the ITU-R BT.601 mode)

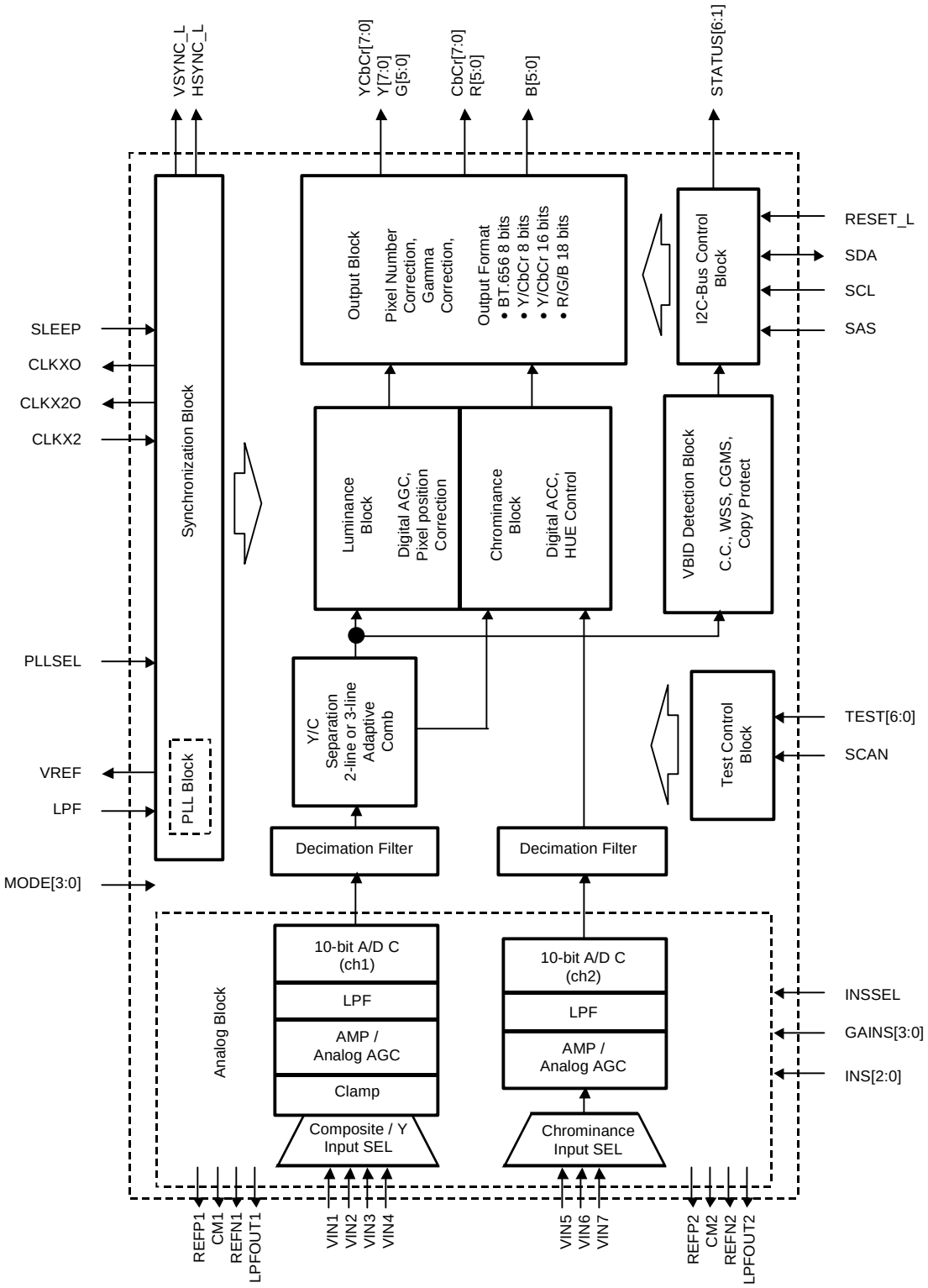
Output Section

- 5 selectable output interfaces
  ITU-R BT.656 : 8 bits (YCbCr)
  8-bit Y/CbCr : 8 bits (YCbCr) (4:2:2) + Sync.
  16-bit Y/CbCr : 8 bits (Y) + 8 bits (CbCr) (4:2:2)/(4:1:1) + Sync.
  18-bit RGB : 6 bits (R) + 6 bits (G) + 6 bits (B) + Sync.
- Output pixel count correction function via internal FIFO
- Screen scaling feature (QVGA)
- Gamma correction function (only RGB output mode)
- Sleep mode
- Output pin Hi-Z mode

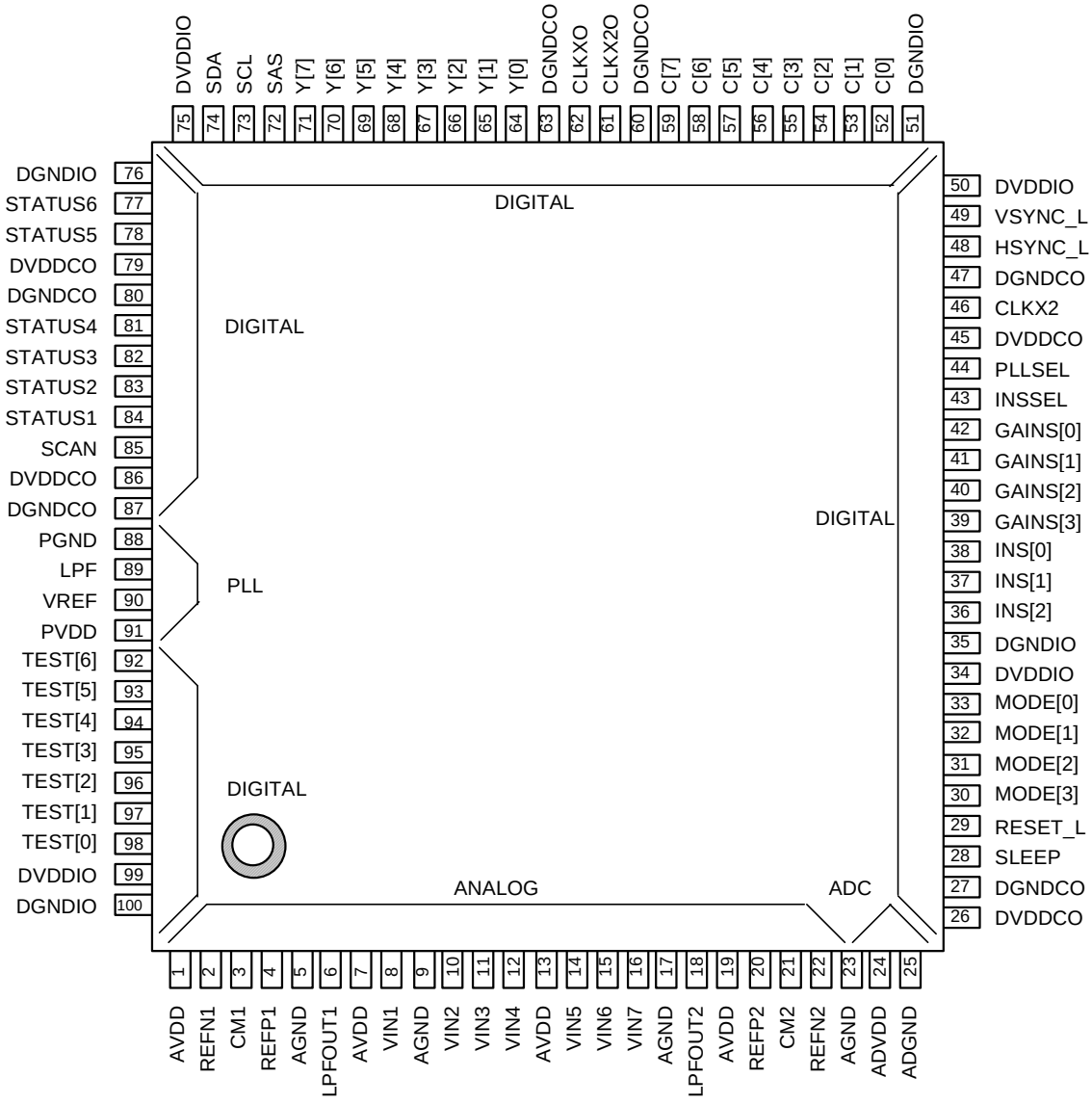
Other Sections

- I^2C-bus interface
- I/O: 3.3 V power supply, Core: 2.5 V power supply
- Package: 100-pin plastic TQFP (TQFP100-P-1414-0.50-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic TQFP (TQFP100-P-1414-0.50-K)

PIN DESCRIPTIONS

Note: The input pins are not pulled up or down.

Pin	Symbol	I/O	Description
1	AVDD	–	Analog power supply
2	REFN1	O	Ch1 ADC reference voltage (low) Open
3	CM1	O	Ch1 ADC reference voltage (middle) Open
4	REFP1	O	Ch1 ADC reference voltage (high) Open
5	AGND	–	Analog ground
6	LPFOUT1	O	Not used. Open
7	AVDD	–	Analog power supply
8	VIN1	I	Composite-1 input Connect this pin to AGND when not used.
9	AGND	–	Analog ground
10	VIN2	I	Composite-2 or S-video 1 luminance signal (Y-1) input Connect this pin to AGND when not used.
11	VIN3	I	Composite-3 or S-video 1 luminance signal (Y-2) input Connect this pin to AGND when not used.
12	VIN4	I	Composite-4 or S-video 1 luminance signal (Y-3) input Connect this pin to AGND when not used.
13	AVDD	–	Analog power supply
14	VIN5	I	S-Video1 macro signal (C-1) input Connect this pin to AGND when not used.
15	VIN6	I	S-Video 2 macro signal (C-2) input Connect this pin to AGND when not used.
16	VIN7	I	S-Video 3 macro signal (C-3) input Connect this pin to AGND when not used.
17	AGND	–	Analog ground
18	LPFOUT2	O	Not used. Open
19	AVDD	-	Analog power supply
20	REFP2	O	Ch2 ADC reference voltage (high) Open
21	CM2	O	Ch2 ADC reference voltage (middle) Open
22	REFN2	O	Ch2 ADC reference voltage (low) Open
23	AGND	–	Analog ground
24	ADVDD	–	ADC power supply
25	ADGND	–	ADC ground
26	DVDDCO	–	Digital core power supply
27	DGNDCO	–	Digital core ground
28	SLEEP	I	Sleep signal input. “0”: Normal operation, “1”: Sleep operation
29	RESET_L	I	Reset signal input. “0”: Reset, 1: Normal operation Reset after power is turned on.

Pin	Symbol	I/O	Description
30 | 31	MODE [3] MODE [2]	I	Output format external setting pins. Connect these pins to the “0” state when not used. Valid when register $01/IOC2[0] = “0” (default). MODE[3:2] “00” ITU-R BT.656: 8 bits (YCbCr) “01” 8-bit Y/CbCr: 8 bits (YCbCr) + Sync. “10” 16-bit Y/CbCr: 8 bits (Y) + 8 bits (CbCr) + Sync. “11” 18-bit RGB: 6 bits (R) + 6 bits (G) + 6 bits (B) + Sync.
32	MODE [1]	I	Operating mode determination setting pin. Connect this pin to the “0” state when not used. “0”: NTSC/PAL automatic determination “1”: NTSC/PAL/SECAM automatic determination
33	MODE [0]	I	“0”: ITU-R BT.601, “1”: Square Pixel The Square Pixel supports only NTSC.
34	DVDDIO	–	Digital IO power supply
35	DGNDIO	–	Digital IO ground
36 | 38	INS [2] | INS [0]	I	Amplifier gain external setting pins. Connect these pins to the "0" state when not used. Valid when external pin 43 INSSEL = 0. INS[2:0] Input pin [000] VIN1(pin 8) Composite-1 [001] VIN2(pin 10) Composite-2 [010] VIN3(pin 11) Composite-3 [011] VIN4(pin 12) Composite-4 [100] VIN2(pin 10) Y-1 VIN5(pin 14) C-1 [101] VIN3(pin 11) Y-2 VIN6(pin 15) C-2 [110] VIN4(pin 12) Y-3 VIN7(pin 16) C-3 [111] Prohibited setting (ADC enters sleep mode)
39 | 42	GAINS [3] | GAINS [0]	I	Amplifier gain external setting pins. Connect these pins to the “0” state when not used. Valid when external pin 43 INSSEL = 0. GAINS [2:0] Gain (X times)
43	INSSEL	I	Amplifier gain setting and input pin switch setting control select pin 0: External pin mode Amplifier gain setting: Pins 39 to 42 GAINS[3:0] are used Input pin setting: Pins 36 to 38 INS[2:0]) are used 1: Register mode Amplifier gain setting: Register $69/ADC2[5:0] Input pin setting: Register $68/ADC1[2:0] The internal register setting is invalid when the external pin mode is set.

Pin	Symbol	I/O	Description
44	PLLSEL	I	System clock select pin. “0”: Fixed clock, “1”: PLL reference clock
45	DVDDCO	–	Digital power supply
46	CLKX2	I	System clock input, or PLL reference clock input (Pin 44 = “0”) NTSC ITU-R BT.601 27 MHz NTSC Square Pixel 24.545454 MHz PAL ITU-R BT.601 27 MHz SECAM ITU-R BT.601 27 MHz PLL reference clock (Pin 44 = “1”) Register $70/PLLC1[6] “0”: 32 MHz*, “1”: 25 MHz
47	DGNDCO	–	Digital core ground
48	HSYNC_L	O	Horizontal sync signal output (H sync)
49	VSYNC_L	O	Vertical sync signal output (V sync)
50	DVDDIO	–	Digital IO power supply
51	DGNDIO	–	Digital IO ground
52 | 59	C [0] | C [7]	O	Data output C[7]:MSB - C[0] ITU-R BT.656 mode : Hi-Z 8-bit Y/CbCr mode : Hi-Z 16-bit Y/CbCr mode : 8-bit (CbCr)data output 18-bit RGB mode : C[7:6] = G[1:0] : C[5:0] = R[5:0] The output mode is set by pins 30 and 31, or register $01/IOC2[5:4].
60	DGNDCO	–	Digital core ground
61	CLKX2O	O	System clock output The system clock is output from this pin. The system clock in operation mode is output when PLL clock mode is used.
62	CLKXO	O	Pixel clock output The pixel frequency is output. (1/2 frequency of the system clock)
63	DGNDCO	–	Digital core ground
64 | 71	Y [0] | Y [7]	O	Data output Y[7]:MSB - Y[0] ITU-R BT.656 mode : YCbCr 8-bit data output 8-bit Y/CbCr mode : YCbCr 8-bit data output 16-bit Y/CbCr mode : 8-bit(Y) data output 18-bit RGB mode : Y[7:4]=B[3:0] : Y[3:0]=G[5:2] The output mode is set by pins 30 and 31, or register $01/IOC2[5:4].

Pin	Symbol	I/O	Description
72	SAS	I	I^2C bus slave address selection. Connect this pin to the “0” state when not used. “0” 1500 001X (X: 0 = Write, 1 = Read) “1” 1500 011X (X: 0 = Write, 1 = Read)
73	SCL	I	I^2C bus clock input. Connect this pin to the “0” state when not used.
74	SDA	I/O	I^2C bus data input/output pin. Externally connect a 4.7kΩ pull-up resistor. Connect this pin to the “0” state when not used.
75	DVDDIO	–	Digital IO power supply
76	DGNDIO	–	Digital IO ground
77	STATUS6	O	STATUS output pin 6. Selected by the internal register. Default VVALID RGB output mode: B[4]
78	STATUS5	O	STATU output pin 5. Selected by the internal register. Default HVALID RGB output mode: B[5]
79	DVDDCO	–	Digital core power supply
80	DGNDCO	–	Digital core ground
81	STATUS4	O	STATUS output pin 4. Selected by the internal register. Default ODD/EVEN
82	STATUS3	O	STATUS output pin 3. Selected by the internal register. Default NTSC/PAL identification
83	STATUS2	O	STATUS output pin 2. Selected by the internal register. Default VHVALID
84	STATUS1	O	STATUS output pin 1. Selected by the internal register. Default HLOCK sync detection
85	SCAN	I	Not used. Fixed to "0".
86	DVDDCO	–	Digital core power supply
87	DGNDCO	–	Digital core ground
88	PGND	–	PLL ground
89	LPF	I	Analog PLL loop filter connection pin. Connect this pin to the "1" state when not used. Refer to the sample circuits provided in the User's Manual.
90	VREF	O	PLL center frequency setting pin. Connect this pin to the "1" state when not used.
91	PVDD	–	PLL power supply
92 | 98	TEST [6] | TEST [0]	I	Not used. Fixed to "0".
99	DVDDIO	–	Digital IO power supply
100	DGNDIO	–	Digital IO ground

FUNCTIONAL DESCRIPTION

This section explains the basic functions of the IC in terms of the blocks shown in the block diagram.
Refer to the User's manual for detailed explanations of the internal registers and any functions that are not covered in this data sheet.

Analog Section

The analog section inputs video signals. The analog section uses the video signal channel selector, AMP and 10-bit ADC to select the desired channel from among several video signals and convert the input to digital video data.

- Analog input selector

  The analog input selector is compatible with composite signals and S-video signals. The maximum number of input connections is 4 channels of composite signals or 3 channels of S-video signals + 1 channels of composite signals. The selection of these input connections can be changed by external pins or by register controls using the I^2C-bus.

  # Related register: $68/ADC1[2:0]

- Clamp function

  The clamp fixes the video input signal in the ADC input range. Clamping is performed by sync chip clamp.

- AMP/analog AGC function

  This function converts video input signals to the optimum level for the ADC using the analog AMP of the AGC function. The AGC function has an output level adjust function in the luminance block of the digital section in addition to the AMP input level adjust function. Manual setting of the AMP gain is also possible.

  # Related register: $69/ADC2

- A/D converter

  This 10-bit A/D converter (ADC) converts analog video signals to digital video data. There are 2 channels built into the ADC. Sampling is performed at the pixel frequency or double-speed.

  # Related registers: $68/ADC1, $69/ADC2, $6A/ADC3

Digital Section

The digital section separates the video data digitized by the ADC into Y and C data, converts these data to various data formats and outputs them. The digital section also performs output level adjustment, image quality adjustment and various corrections.

- Decimation filter

  Since internal processing is performed at a single speed, this filter is needed to reduce the data that has been doubled by one-half. Using the decimation filter after double-speed sampling reduces high-frequency noise .

  # Related register: $08/FIFOBC[7]

2-dimensional Y/C Separation Block

This block separates composite data into Y (luminance) data and C (chrominance) data. For S pin input, Y/C separation circuit is bypassed. The Y/C separation function works only for lines which are active as image data and is bypassed for composite signals in the V blanking period.

- 2-Dimensional Y/C Separation Function

  With the Y/C separation filter, composite data is separated into Y (luminance) data and C (chrominance) data. There are various Y/C separation filters available, which can be selected in an internal register.
  Y/C separation of the SECAM signal is performed by the trap filter.

  # Related register: $10/YC1, $11/YC2

YC1[6:4]	NTSC Y/C separation	PAL Y/C separation
*000	2-line/3-line adaptive comb filter	2-line/3-line adaptive comb filter
001	3-line comb filter	2-line comb filter
010	Trap filter	Trap filter
011	3-line comb/trap adaptive filter	Undefined
100	Undefined	Undefined
101	2-line/3-line adaptive transition filter	Undefined
110	Undefined	Undefined
111	Undefined	2-line comb/trap adaptive transition filter

Luminance Block

The luminance block removes sync signals from the luminance data after Y/C separation, and performs adjustments such as luminance level adjustment and luminance image quality correction and adjustment. The digital decoded data that is output conforms with ITU-R BT.601.

- Pixel Position Correction Function

  This function corrects sampling error in asynchronous sampling and loss of PLL synchronization. Error correction is made in the horizontal direction, which improves vertical line jitter on the screen.

  # Related register: $22/SYNC3

- Digital AGC Function

  This function adjusts the output level of luminance signals. Adjustment is automatically performed by the digital AGC, but the adjustment can also be set manually by using an internal register to set digital MGC. In the digital AGC mode, the sync level is compared with a reference value to determine the amplification rate of the luminance level. The default is automatically adjusted to sync level 40IRE, but the level can also be adjusted in an internal register. In the digital MGC mode, the signal amplification rate and the black level are adjusted with register settings. The black level is adjusted by means of pedestal level adjustment.

  Regarding the AGC function, in addition to the output level adjust function in the digital section, the input level adjust function of the AMP in the analog section also operate separately.

  Note: AGC (Auto Gain Control), MGC (Manual Gain Control)

  # Related registers: $30/AGCC, $31/AGCRC, $32/SSEPL, $36/CLC

- Image Quality Adjustment

  The following image filters are provided for adjusting luminance image quality.
  Refer to the User's Manual for the characteristics of each filter.
  Aperture bandpass filter, coring filter for contour compensation, and luminance pre-filter

  # Related register: $35/LUMC4

Chrominance Block

This block decodes chroma data to Cb/Cr data and performs level adjustment and color adjustment. To eliminate unnecessary bands, this block first passes data through a bandpass filter (bypass is possible) and then through an ACC correction circuit to maintain a stable chroma level, before performing UV decoding. The result of the UV decoding is passed through a low-pass filter and output as a chrominance signal.

Related registers: $46/CHRSC1, $47/CHSC2

• Digital ACC Function

The digital ACC is the gain adjustment for the chrominance signal output level. Adjustment is automatically performed by the digital ACC (Auto Chrominance Control), but the adjustment can also be set manually by using an internal register to set digital MCC (Manual Chrominance Control). In the digital ACC mode, the burst level is compared with a reference value to determine the amplification rate of the chrominance level. The default is automatically adjusted to sync level 40IRE, but the level can also be adjusted in an internal register. Separate U/V level adjustment is also possible.

Related registers: $40/ACCC, $41/ACCRC

• Hue Adjust Function

The function for adjusting hue.

Hues can be adjusted by setting the HUE register.

Related register: $45/HUE

Output Block

The output block performs output timing adjustment, picture sizing, output format conversion and other types of output conversion.

• Pixel Count Correction Function

This function uses the internal FIFO to correct the total number of pixels in a line. It corrects the 1-line sampling error generated when in asynchronous sampling mode or PLL synchronization is lost, and fixes the pixel count for a line within the active screen. Refer to Active Pixel Timing for more on the pixel count for one line.

• Output Format Conversion Function

This function converts the output data to the desired output format.

The following output formats are possible.

Related registers: $00/IOC1, $01/IOC2

Output Formats

Output mode (i): interlace		Register IOC2[0] = 0	Register IOC2[0] = 1	Register
		Control pin (Pins 30, 31)	Register	
		MODE[3:2]	IOC2[5:4]	IOC2[1]
ITU-R BT.656	(i) 4:2:2	[00]	[00]	0
Y/CbCr 8 bits	(i) 4:2:2	[01]	[01]*	0
Y/CbCr 16 bits	(i) 4:2:2	[10]	[10]	0
Y/CbCr 16 bits	(i) 4:1:1	[10]	[10]	1
RGB 18 bits	(i) 4:4:4	[11]	[11]	0

Synchronization Block

This block controls the sync signals for internal operation, output sync signals, and the timing for each block. Synchronization detection levels, output timing, and various other functions can be adjusted by the registers listed below.

• PLL Function

The digital PLL circuit generates an operating clock synchronized with the horizontal sync signals of the video signals. With the input of a 25 MHz or 32 MHz standard clock, the double-speed sampling clock for each mode is provided as a line lock clock and used as the system clock.

The asynchronous sampling mode, which uses an asynchronous clock directly, can be used without using PLL.

Related registers: $70/PLLC1, $71/PLLC2, $72/PLLC3, $73/PLLC4

Input Clock Settings

Control pin Pin 44 PLLSEL	Input clock		Sampling
PLLSEL = "0" Fixed clock	Sampling clock input according to the operating mode (See the table below)		Asynchronous
PLLSEL = "1" PLL clock	\$70/PLLC1[6] = "0" * 32 MHz	\$70/PLLC1[6] = "1" * 25 MHz	\$70/PLLC1[7] = "0" * PLL ON/line lock
			\$70/PLLC1[7] = "1" PLL OFF/asynchronous

In the PLL mode, a double-speed line lock clock is generated by setting the operating mode.

Operating Modes/Sampling Clock Settings

Operating mode	\$01/IOC2[0] = "0" *	\$01/IOC2[0] = "1" *	Sampling clock (double-speed)
	Control pin (Pin 33)	Register	
	MODE[0]	\$00/IOC1[1]	Pin 46 CLKX2
ITU-R BT.601 13.5 MHz	0	0 *	27 MHz
NTSC Square pixel 12.272727 MHz	1	1	24.545454 MHz

—: Not used *: Default

VBID Detection Block

This block detects data information and copy protection information from the VBI (Vertical Blanking Interval) of the input luminance signals. The following four types of VBID data can be detected, and the detection line and detection level can be changed by altering register settings.

*Note: VBID detection may not provide accurate detection, if the signal status is bad.

- VBID Detection Function

(1) AGC copy protection

Detects whether specified lines include a macrovision AGC pulse (NTSC/PAL) and sets a flag.

Related registers: \$86/AGCD1, \$87/AGCD2, \$81/VBIDM, \$89/AIREG, \$92/VFLAG

(2) C. C. (Closed Caption)

Detects whether specified lines include closed caption data (NTSC/PAL), keeps separately the data of even and odd lines, and sets individual flags.

Related registers: \$82/CCD1, \$83/CCD2, \$81/VBIDM, \$89/AIREG, \$92/VFLAG, \$93/CCD00, \$94/CCD01, \$95/CCDE0, \$96/CCDE1

(3) WSS (Wide Screen Signaling)

Detects the WSS data in the lines specified by ETSI (European Telecommunications Standards Institute) and sets a flag (PAL only).

Related registers: \$88/WSSD, \$81/VBIDM, \$89/AIREG, \$92/VFLAG, \$9D/WSSD0, \$9E/WSSD1

(4) CGMS (Copy Generation Management System)

Detects the CGMS data in the lines specified by IEC61880 and sets a flag (NTSC only).

Related registers: \$84/CGMS1, \$85/CGMS2, \$81/VBIDM, \$89/AIREG, \$92/VFLAG, \$97/CGMS00, \$98/CGMS01, \$99/CGMS02, \$9A/CGMSE0, \$9B/CGMSE1, \$9C/CGMSE2

(5) Other copy protection detection functions
Detects the color stripes, false pulses, and MV protection and sets flags.
Related registers: $89/AIREG, $90/STATUS1, $91/STATUS2, $92/VFLAG

I^2C-bus Control Block
This serial interface block is based on the I^2C standard of the Phillips Corporation. The registers at up to subaddress 89h are write/read, while the registers from 90h on are read-only.

Normally, a license from the Phillips Corporation allowing the use of its I^2C patent is required to use an I^2C bus. However, the license to use this LSI chip as a slave is granted by the Phillips Corporation upon purchasing this LSI chip. There is no need for a license if the decoder is used alone, without I^2C control, but if this I^2C-bus is used to control this LSI, a license for use as a master is required.

As of 2001, the I^2C patent expired in Japan and the rest of the Asian region, so there have been no costs with regard to license fees. However, in the USA and Canada, there is still a requirement for the payment of license fees, so if this product is intended for overseas trade, it may be necessary to pay the Phillips Corporation license fees for the use of its patent. For more information, contact the Phillips Corporation.

Test Control Block
This block is used to test the LSI chip. It is not intended for user use.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	VDD1 *1	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage	VDD2 *2	Ta = 25°C	–0.3 to +3.6	V
Input voltage	Vi	Ta = 25°C	–0.3 to +3.9	V
Power consumption	Pw	Ta = 25°C	800	mW
Short output current	Ios	—	50	mA
Storage temperature	Tstg	—	–55 to +150	°C

Warning: Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.

*1 VDD1 (DVDD1,AVDD,ADVDD,PVDD)

*2 VDD2 (DVDD2)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	DVDD1	—	3	3.3	3.6	V
Power supply voltage	DVDD2	—	2.25	2.5	2.75	V
Power supply voltage	AVDD	—	3	3.3	3.6	V
Power supply voltage	ADVDD	—	3	3.3	3.6	V
Power supply voltage	PVDD	—	3	3.3	3.6	V
Power supply voltage	GND	—	—	0	—	V
Digital "H" level input voltage	Vih2	—	0.8 VDD	—	VDD+0.3	V
Digital "L" level input voltage	Vil	—	-0.3	—	0.6	V
Operating temperature	Ta	—	-40	—	85	°C

Note: Apply power to the device in order of DVDD1 → AVDD → DAVDD → PVDD → DVDD2. Follow the reverse sequence to power off the device.
Reset after all power supply voltages reach the specified values and check CLKX2 is input.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=-40～+85℃、VDD(DVDD1,ADVDD,AVDD,PVDD)=3.0V～3.6V,VDD2=2.25～2.75V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" level output voltage	Voh	Ioh=-4mA (*1)	0.7VDD	——	——	V
"L" level output voltage	Vol	Iol=4mA (*1)	——	——	0.6	V
Input leakage current	Ii	Vi=GND～VDD	-10	——	10	mA
Output leakage current	Io	Vi=GND～VDD	-10	——	10	mA
CM output voltage	Voclp	——	1.25	1.5	1.65	V
REFP output voltage	Vrt	——	1.75	2	2.15	V
REFN output voltage	Vrb	——	0.75	1	1.15	V
ADIN	Viadin	——	Vrb	——	Vrt	V
VIN	Vivin	C Coupling	0.4	—	1.3	Vp-p

*1: Y[7:0], C[7:0], HSYNC_L, VSYNC_L, VVALID, HVALID, CLKXO, STATUS1, STATUS2, STATUS3, STATUS4, CLKX2O

(Ta = –40 to +85°C, VDD (DVDD1, ADVDD, AVDD, PVDD) = 3.0 to 3.6 V, VDD2 = 2.25 to 2.75 V)

Parameter	Symbol	Condition	Operating clock	VDD	Typ. VDD = 3.3 V VDD2 = 2. 5 V	Max. VDD = 3.6 V VDD2 = 2.75 V	Unit
Digital power supply current (DVDD) 1 channel operating	IDD1	PLL Mode CLKX2= 32MHz AD1 on AD2 off	24.545454MHz	VDD	15	20	mA
				VDD2	35	55	
			27MHz	VDD	15	20	
				VDD2	40	60	
Analog power supply current (AVDD + ADVDD + PVDD)	IDA1		24.545454MHz		35	60	mA
			27MHz		35	60	
Digital power supply current (DVDD) 2 channels operating	IDD2	PLL Mode CLKX2= 32MHz AD1 on AD2 on	24.545454MHz	VDD	15	20	mA
				VDD2	35	50	
			27MHz	VDD	15	20	
				VDD2	40	55	
Analog power supply current (AVDD + ADVDD + PVDD)	IDA2		24.545454MHz		70	110	mA
			27MHz		70	120	
Digital power supply current (DVDD) 1 channel operating	IDD1	Fixed Clock Mode AD1 on AD2 off	24.545454MHz	VDD	15	20	mA
				VDD2	35	50	
			27MHz	VDD	15	20	
				VDD2	40	55	
Analog power supply current (AVDD + ADVDD + PVDD)	IDA1		24.545454MHz		30	50	mA
			27MHz		30	50	
Digital power supply current (DVDD) 2 channels operating	IDD2	Fixed Clock Mode AD1 on AD2 on	24.545454MHz	VDD	15	20	mA
				VDD2	35	50	
			27MHz	VDD	15	20	
				VDD2	40	55	
Analog power supply current (AVDD + ADVDD + PVDD)	IDA2		24.545454MHz		60	100	mA
			27MHz		60	110	
Power supply current (inactive)	IDDS	SLEEP			–	10	mA

AC Characteristics

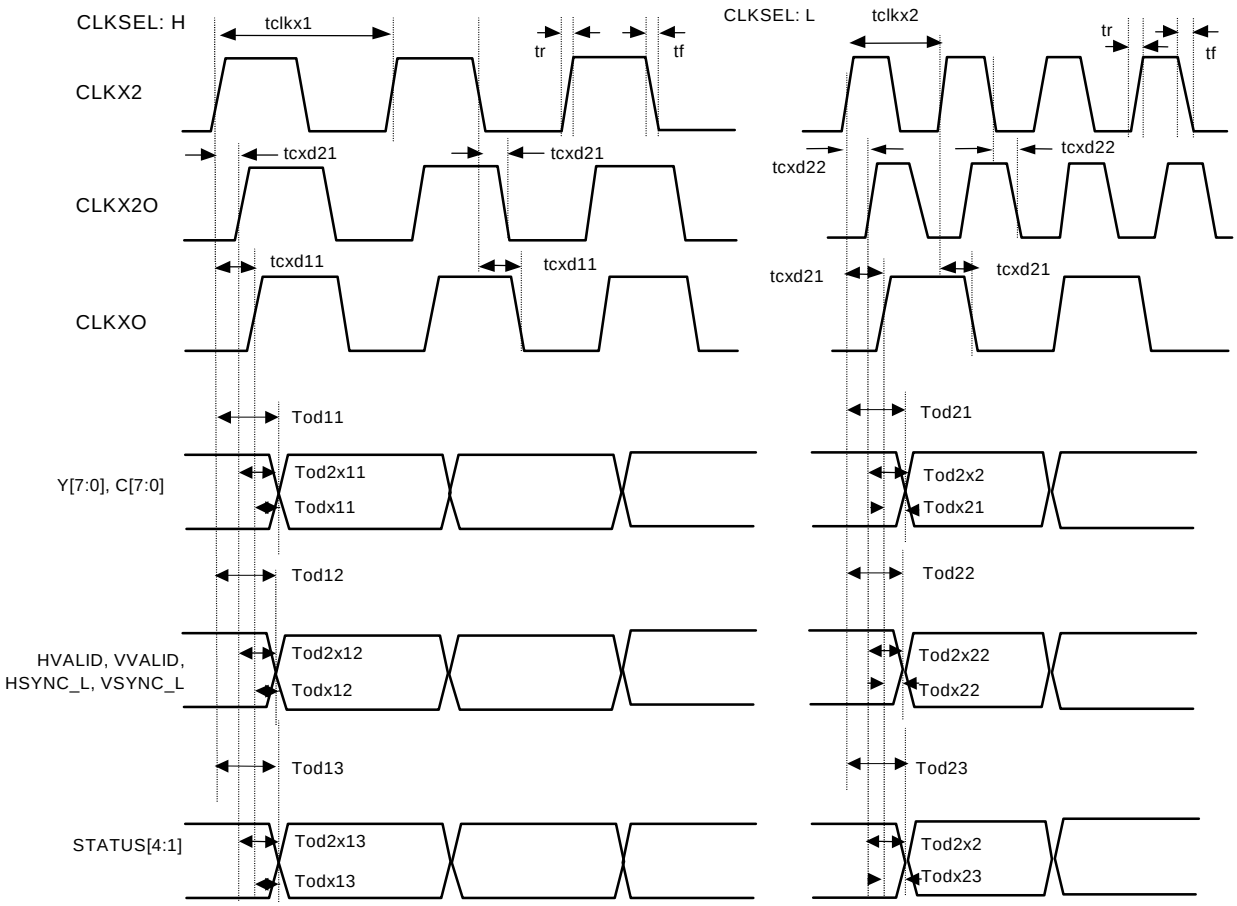
(Ta = –40 to +85°C, VDD (DVDD1, ADVDD, AVDD, PVDD) = 3.0 to 3.6 V, VDD2 = 2.25 to 2.75 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Cycle Frequency	1/tclkx2	ITU-R BT.601	—	27.0	—	MHz
		NTSC Square Pixel	—	24.545454	—	MHz
CLKX2 Duty	td_d2	—	45	—	55	%
Output Data Delay Time 1(*)	tod21	CLKSEL:L	——	——	16	ns
Output Data Delay Time 2(*)	tod22	CLKSEL:L	——	——	16	ns
Output Data Delay Time 3(*)	tod23	CLKSEL:L	——	——	16	ns
Output Data Delay Time 1x1(*)	todx21	CLKSEL:L	——	——	8	ns
Output Data Delay Time 1x2(*)	todx22	CLKSEL:L	——	——	8	ns
Output Data Delay Time 1x3(*)	todx23	CLKSEL:L	——	——	8	ns
Output Data Delay Time 2x1(*)	tod2x21	CLKSEL:L	——	——	10	ns
Output Data Delay Time 2x2(*)	tod2x22	CLKSEL:L	——	——	10	ns
Output Data Delay Time 2x3(*)	tod2x23	CLKSEL:L	——	——	10	ns
Output Clock Delay Time (*) (CLKX2-CLKX0)	tcxd21	CLKSEL:L	——	——	10	ns
Output Clock Delay Time (*) (CLKX2-CLKX20)	tcxd22	CLKSEL:L	——	——	8	ns
RESET_L width	rst_w		200	——	——	ns

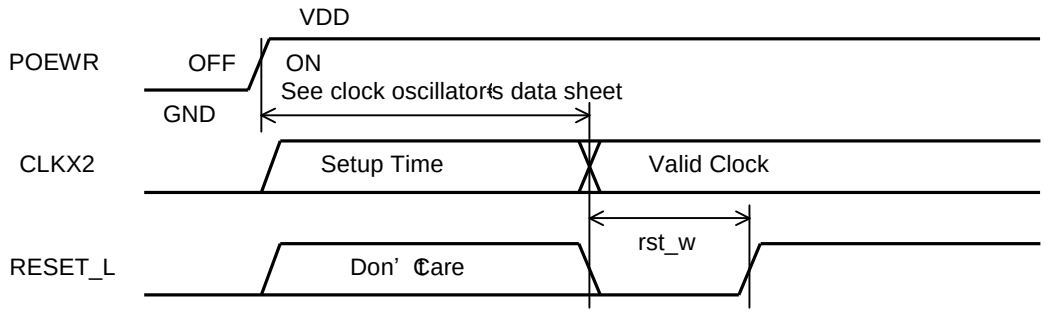
(*) Output load: 20 pF
Use a clock frequency accuracy of ± 100 ppm.

INPUT AND OUTPUT TIMING DIAGRAMS

Data Output Timing

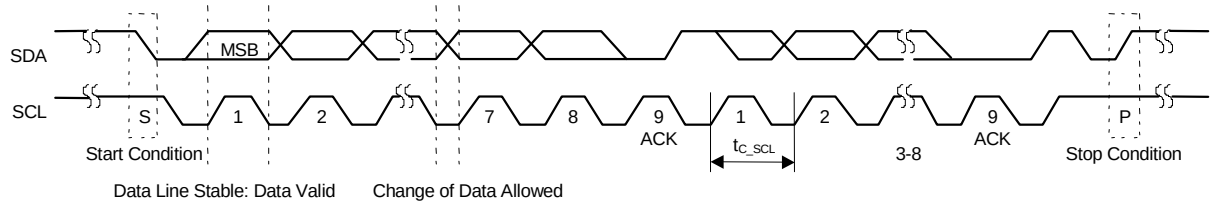


Reset Timing

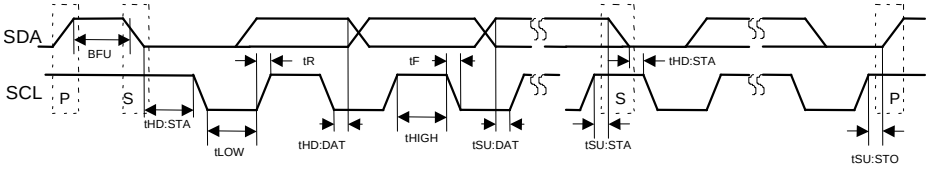


(*) Output data is "don't care" at reset.

I²C-bus Interface Timing



I²C-bus Timing

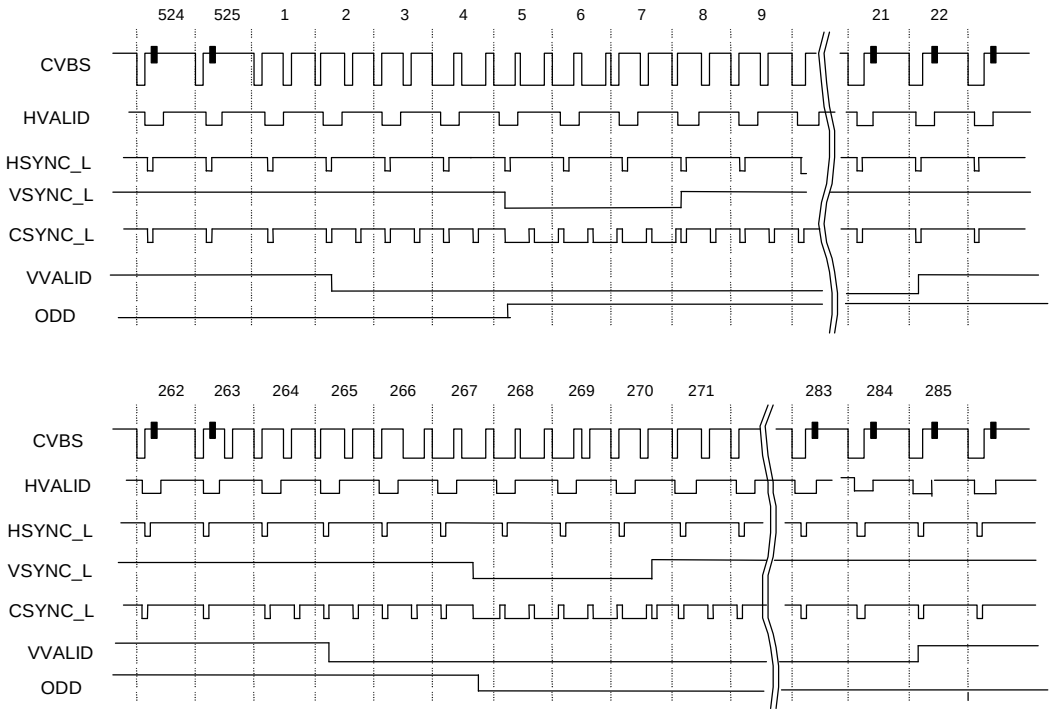


Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL frequency	0	100	400	KHz
tBUF	Bus open time	4.7			µs
tHD:STA	Start condition hold time	4.0			µs
tLOW	Clock LOW period	4.7			µs
tHIGH	Clock HIGH period	4.0			µs
tSU:STA	Start condition setup time	4.7			µs
tHD:DAT	Data hold time	300			ns
tSU:DAT	Data setup time	250			ns
tR	Line rise time			1	µs
tF	Line fall time			300	ns
tSU:STO	Stop condition setup time	4.7			µs

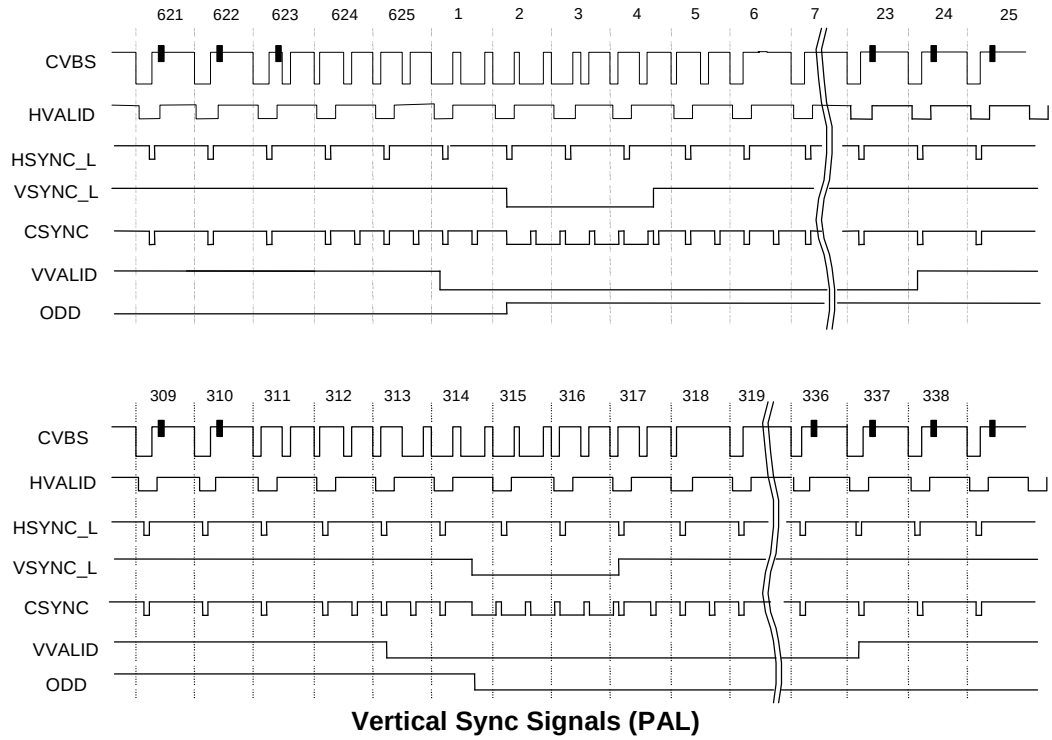
The I²C-bus timing is based on the table above.

Sync Signal Input and Output Timings (Default)

The following illustrations show the timing of vertical sync signals. The internal processing of the sync signal is performed before 1H.



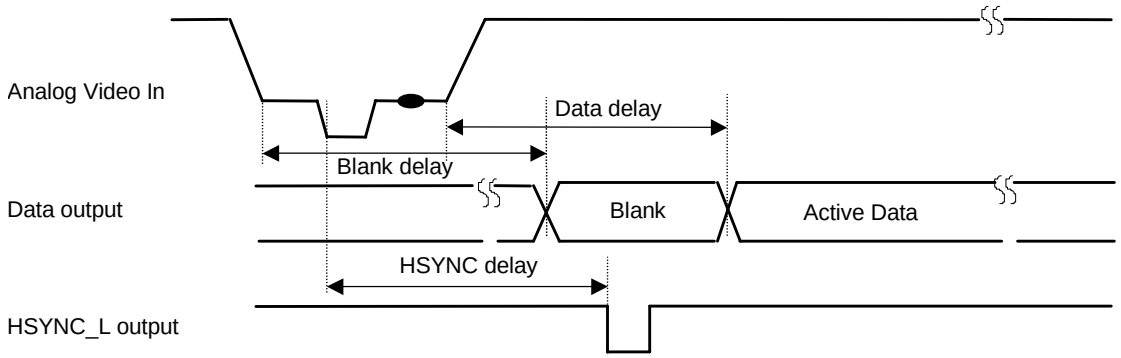
Vertical Sync Signals (NTSC)



Vertical Sync Signals (PAL)

Input/Output Delays (at Standard Signal Input)

The illustration below shows the time delay between the input of a video signal and the output of digital data.

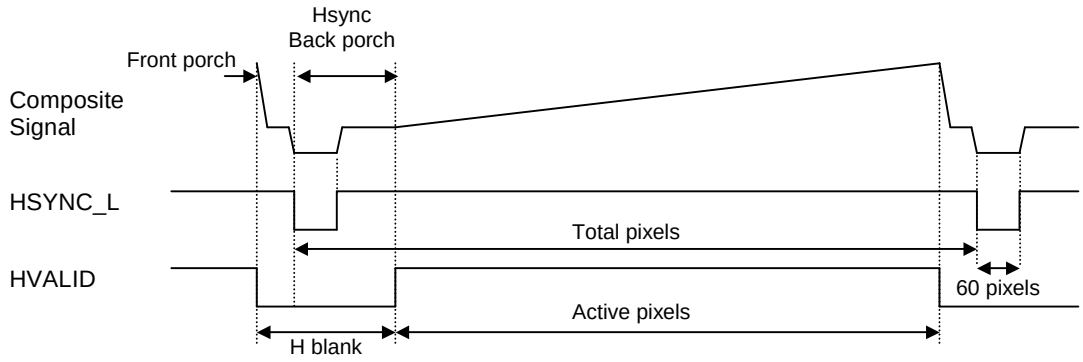


Absorption difference by T = 1 Pixel rate, α = FIFO

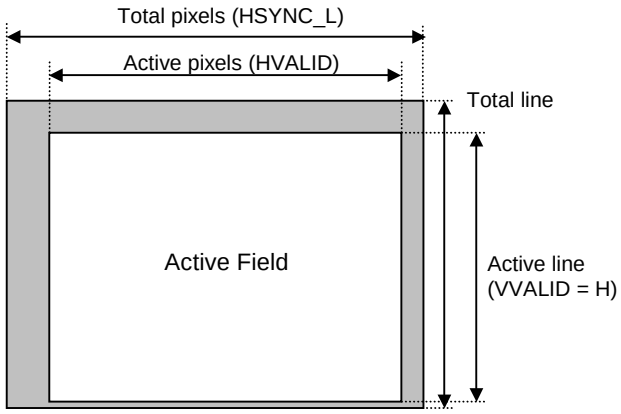
Video mode	Input signal	FIFO/FM mode	Delay
NTSC	Composite	FIFO-1	1.5H
NTSC	Composite	FM	1.5H
PAL/SECAM	Composite	FIFO-1	1.5H
PAL/SECAM	Composite	FM	1.5H

The data delay, blank delay, and sync signal delay are the same length.
1H varies with the sampling mode.
Depending on the signal status, the numeric value (T value) may vary.
In the FIFO mode, the output cycle is fixed, so the delay varies.
In the PAL mode, where Y/C separation is performed by trap filter, 1H is not added.

Active Pixel Timing



Note: Actually, there is an output delay of about 1H after video signal input.



Video Modes and Pixel/Line Counts (at Standard Signal Input)

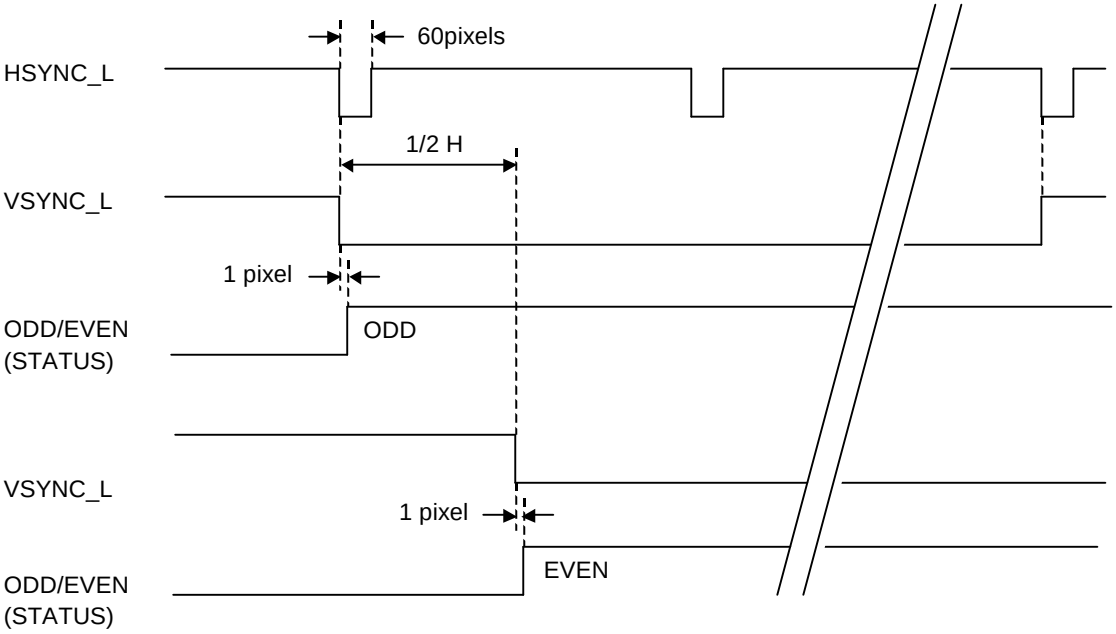
Video mode	Sampling pixel mode	Output pixel rate (MHz)	H					V			
			Front porch	Hsync Back porch	H blank	Active pixels	Total pixels	V blank	Active line	Total line	VSYNC_L
NTSC	ITUR.601	13.5	16	122	138	720	858	Odd/20 Even/20	Odd/242 Even/243	Odd/262 Even/263	Odd/262 Even/263
	Square pixel	12.272727	22	118	140	640	780				
PAL/ SECAM	ITUR.601	13.5	12	132	144	720	864	Odd/24 Even/25	Odd/288 Even/288	Odd/312 Even/313	Odd/312 Even/313

Note: Where the FIFO mode is used in asynchronous sampling operations with fixed clock, the 1-field sampling error accumulated in the line immediately following the fall of VVALID is reset. Therefore, the pixel count for the line that was reset will change. In addition, where the condition of VTR and other signals is poor in the FIFO-2 mode, the FIFO reset line might break in before the fall of VVALID.

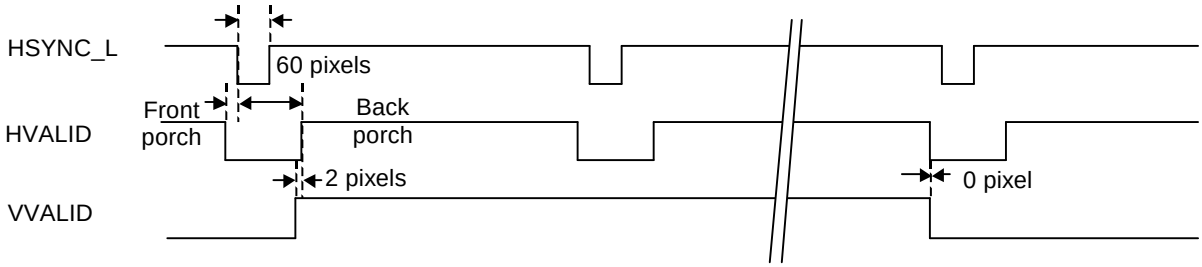
Sync Signals Output Timing (at Default/Standard Signal Input)

Each VALID signal and the ODD/EVEN signal are selected by the STATUS signal.

VSYNC_L, ODD/EVEN

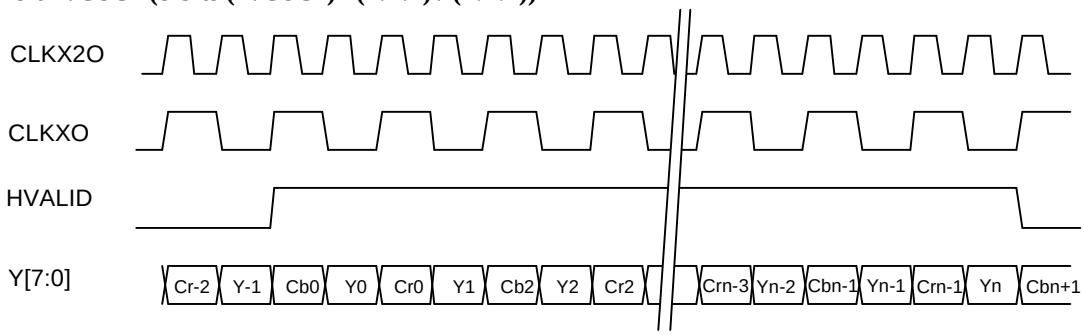


VALID Signal

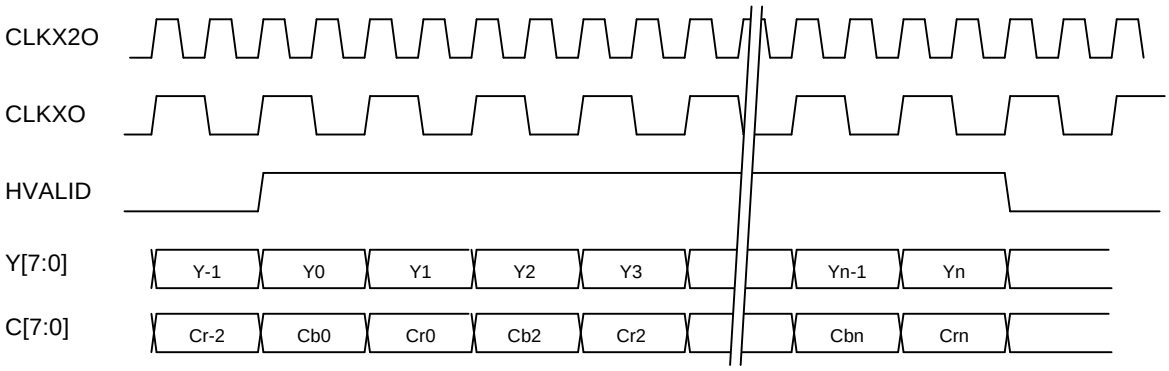


Output Timing by Mode

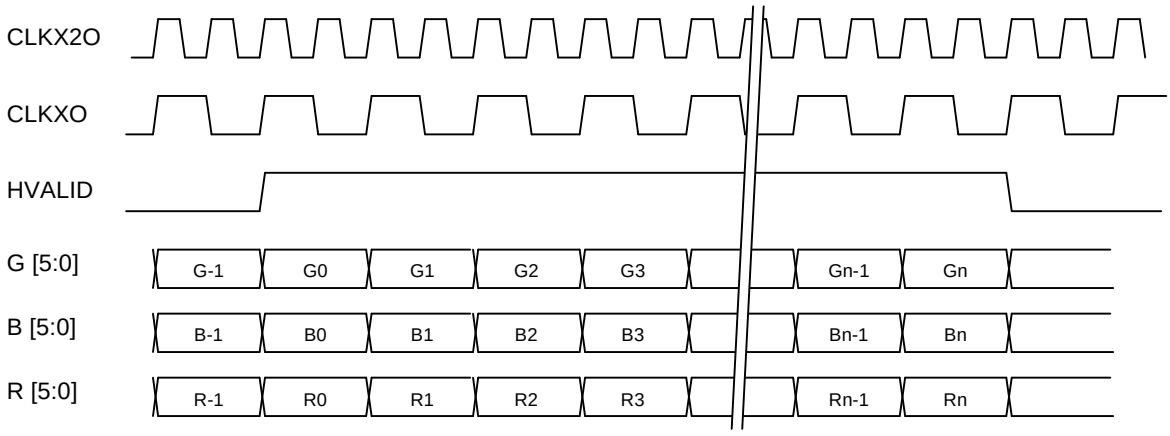
8-bit Y/CbCr (8 bits (Y/CbCr) (4:2:2) / (4:1:1))



16-bit Y/CbCr (8 bits (Y) + 8 bits (CbCr) (4:2:2) / (4:1:1))

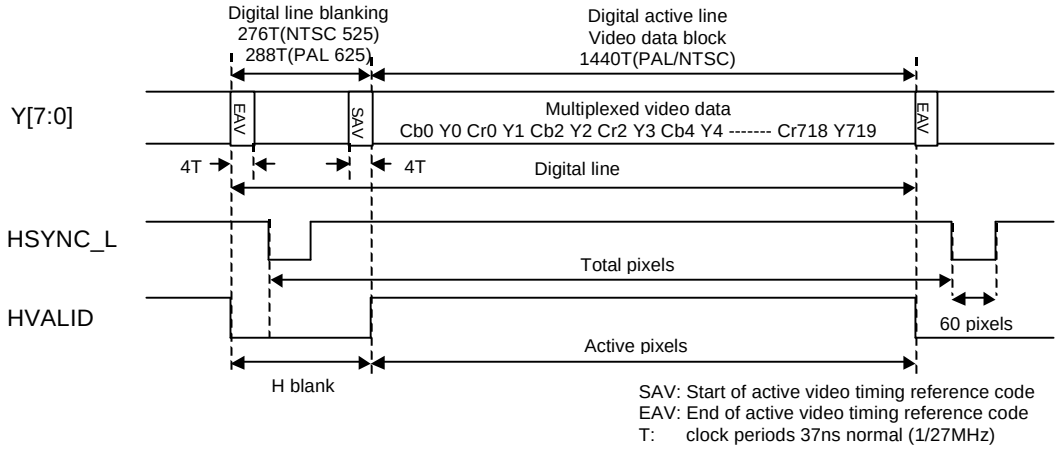


18-bit RGB (6 bits (R) + 6 bits (G) + 6 bits (B))



ITU-R BT.656-4 output:

Output is performed based on BT.656 of the ITU standards. Since sync signal information (SAV, EAV) is multiplexed with video data, for the interface that complies with BT.656, data can be transferred by connecting to 8-bit data lines, without connecting to the sync signal.



The data in the blanking period is masked, but the Y data can be output.

Note: When operating in the asynchronous sampling mode, digital lines 1716T (NTSC,525) and 1728T (PAL, 625) will change due to the sampling error.
In the FIFO mode, the pixels count correction function ensures that there is no fluctuation in the pixel count between active lines, but the line immediately following the fall of VVALID will change due to the FIFO reset.
In particular, when non-standard signals such as VTR signals are input, the line immediately following the fall of VVALID will vary greatly in accordance with the degree of the instability of the input signal. Where the sampling error is large, the line will change immediately before the fall of VVALID.
In some cases where the line count increases or decreases with respect to the reference, such as non-standard signals, EAV and SAV may not be guaranteed.

INTERNAL REGISTERS

The following is a list of registers. Be sure to use only the subaddresses specified in the table below. Refer to the User's Manual for details of each register.

	W/R	Sub ADD	Number of Register Bit's								HEX
			MSB	Default Value						LSB	
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
IOC1	W/R	00	0	0	0	1	0	0	0	1	11
IOC2	W/R	01	0	0	0	0	0	0	0	0	00
IOC3	W/R	02	0	0	0	0	1	0	1	1	0b
IOC4	W/R	04	0	0	0	0	0	0	1	0	02
IOC5	W/R	05	0	0	0	0	0	0	0	0	00
FIFOBC	W/R	08	0	0	0	1	0	0	0	0	10
RR1	W/R	09	0	0	0	0	0	0	0	0	00
RR2	W/R	0A	0	0	0	0	0	0	0	0	00
YC1	W/R	10	0	0	0	0	0	0	0	0	00
YC2	W/R	11	0	0	0	1	0	0	0	0	10
RR3	W/R	12	0	0	0	0	0	0	0	0	00
SYNC1	W/R	20	0	0	0	1	0	0	0	0	10
SYNC2	W/R	21	0	0	0	0	0	0	1	0	02
SYNC3	W/R	22	1	0	0	0	0	0	1	0	82
HSTHR	W/R	23	1	0	0	1	1	1	1	1	9f
VSTHR	W/R	24	0	0	0	0	0	0	0	0	00
HSDL	W/R	25	0	0	0	0	0	0	0	0	00
HVALT	W/R	26	0	0	0	0	0	0	0	0	00
VVALT1	W/R	27	0	0	0	0	0	0	0	0	00
VVALT2	W/R	28	0	0	0	0	0	0	0	0	00
AGCC	W/R	30	0	1	0	0	0	0	0	1	41
AGCRC	W/R	31	0	0	0	0	0	0	0	0	00
LUMC1	W/R	32	0	0	0	0	0	0	0	0	00
LUMC2	W/R	33	1	0	0	0	0	1	0	0	84
LUMC3	W/R	34	0	0	0	0	0	0	0	0	00
LUMC4	W/R	35	0	0	0	0	0	0	0	0	00
CLC	W/R	36	0	0	0	0	0	0	0	0	00
LOFLC	W/R	37	0	0	0	0	0	0	0	0	00
ACCC	W/R	40	0	1	0	0	0	0	0	0	40
ACCRC	W/R	41	0	0	0	0	0	0	0	0	00
CHRC	W/R	42	0	0	0	0	0	0	0	0	00
CKILL1	W/R	43	0	1	0	1	1	1	1	1	5f
CKILL2	W/R	44	0	0	0	1	0	0	0	1	11
HUE	W/R	45	0	0	0	0	0	0	0	0	00
CHRSC1	W/R	46	0	0	0	0	0	0	0	0	00
CHRSC2	W/R	47	0	0	0	0	0	0	0	0	00
BBHC1	W/R	50	1	0	0	0	1	0	0	1	89
BBHC2	W/R	51	0	0	0	0	0	0	0	0	00

	W/R	Sub ADD	Number of Register Bit's								HEX
			MSB	Default Value						LSB	
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
RGBC	W/R	54	0	0	0	0	0	0	0	0	00
QVGAC	W/R	58	0	0	0	0	0	0	0	0	00
ADC1	W/R	68	1	1	1	0	0	0	0	0	e0
ADC2	W/R	69	0	0	1	1	1	1	1	1	3f
ADC3	W/R	6A	0	0	1	1	0	0	0	0	30
RR4	W/R	6B	0	0	0	0	0	0	0	0	00
RR5	W/R	6C	1	1	1	1	0	0	1	1	f3
PLLC1	W/R	70	0	0	0	0	0	0	0	0	00
PLLC2	W/R	71	0	0	0	0	0	0	0	0	00
PLLC3	W/R	72	0	0	0	0	0	0	0	0	00
PLLC4	W/R	73	0	0	0	0	0	0	0	0	00
STA1	W/R	78	0	1	1	0	0	1	0	0	64
STA2	W/R	79	0	0	1	1	0	0	1	0	32
STA3	W/R	7A	0	0	0	1	0	0	0	0	10
VBIDC	W/R	80	0	0	0	0	0	0	0	0	00
VBIDM	W/R	81	1	0	0	0	0	1	1	0	86
CCD1	W/R	82	0	0	0	0	0	0	0	0	00
CCD2	W/R	83	0	0	0	0	0	0	0	0	00
CGMS1	W/R	84	0	0	0	0	0	0	0	0	00
CGMS2	W/R	85	0	0	0	0	0	0	0	0	00
AGCD1	W/R	86	0	0	0	0	0	0	0	0	00
AGCD2	W/R	87	0	0	0	0	0	0	0	0	00
WSSD	W/R	88	0	0	0	0	0	0	0	0	00
AIREG	W/R	89	0	0	0	0	0	0	0	0	00
STATUS1	R	90	–	–	–	–	–	–	–	–	–
STATUS2	R	91	–	–	–	–	–	–	–	–	–
VFLAG	R	92	–	–	–	–	–	–	–	–	–
CCDO0	R	93	–	–	–	–	–	–	–	–	–
CCDO1	R	94	–	–	–	–	–	–	–	–	–
CCDE0	R	95	–	–	–	–	–	–	–	–	–
CCDE1	R	96	–	–	–	–	–	–	–	–	–
CGMSO0	R	97	–	–	–	–	–	–	–	–	–
CGMSO1	R	98	–	–	–	–	–	–	–	–	–
CGMSO2	R	99	–	–	–	–	–	–	–	–	–
CGMSE0	R	9A	–	–	–	–	–	–	–	–	–
CGMSE1	R	9B	–	–	–	–	–	–	–	–	–
CGMSE2	R	9C	–	–	–	–	–	–	–	–	–
WSS0	R	9D	–	–	–	–	–	–	–	–	–
WSS1	R	9E	–	–	–	–	–	–	–	–	–

NOTES ON USE

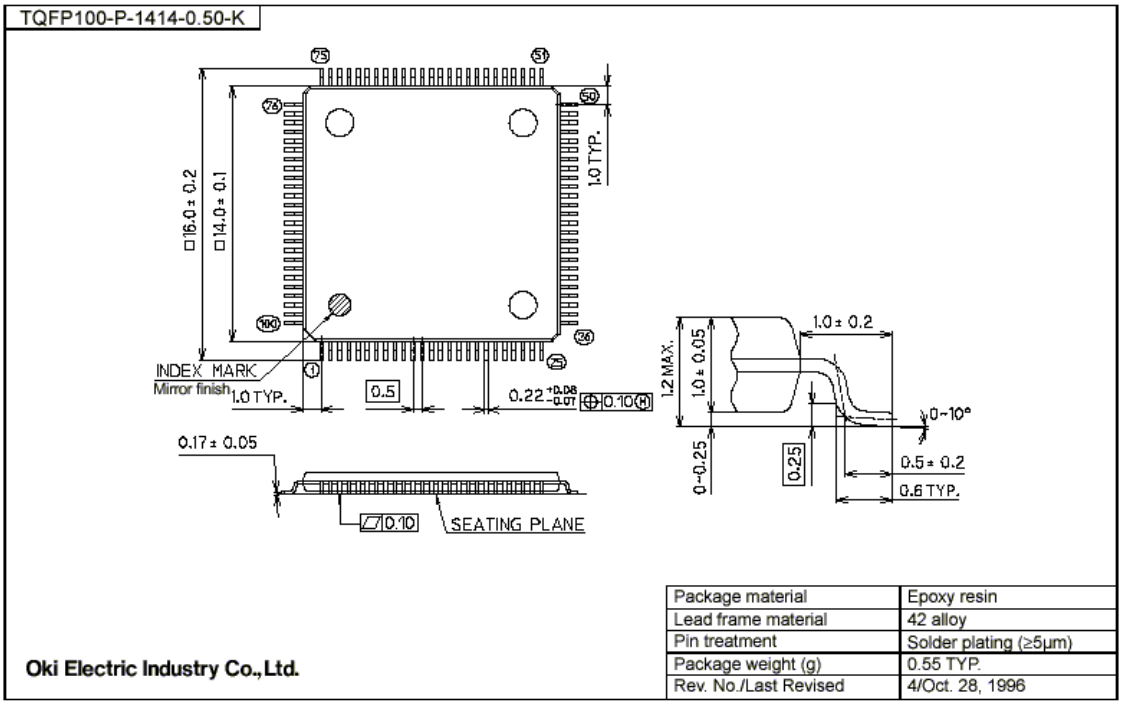
The ML86V7668 Video Decoder is being developed based on standard signals. Improvements are being made to ensure stable operation even with non-standard signals. However, the signal conditions and usage environments differ widely for signals such as those having a weak electromagnetic field, VTR playback signals, signals with numerous signal switching or a large amount of noise, and simple video signals from various cameras. As a result, stable operation for all signals has not yet been confirmed. Before using the decoder, please carefully evaluate and consider the signal conditions and usage environment of the intended use.

In addition to this Data Sheet, a ML86V7668 User's Manual is also available. The User's Manual explains each register and provides examples of adapted circuits as well as other information helpful in the design phase. Please read the User's Manual before embarking on design work.

Users are also requested to regularly download the most recent versions of this Data Sheet and the User's Manual from the Oki web site. As the newest information, not included in printed materials, and the answers to frequently asked questions are published on the web site, users are recommended to check the site regularly for updates.

PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL86V7668-01	Aug. 28, 2004	–	–	Preliminary edition 1

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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