



Integrated Device Technology, Inc.

# 64K x 16 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4027

## FEATURES:

- High density 1 megabit static RAM module
- Low profile 40 pin DSIP (Dual Single In-line vertical Package)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ( $\pm 10\%$ ) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

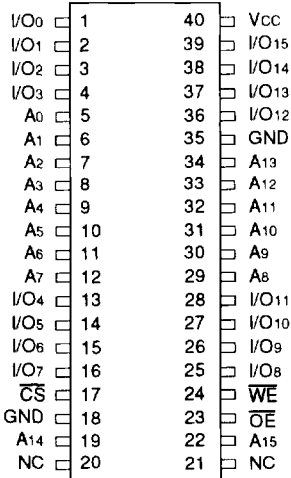
## DESCRIPTION:

The IDT7MP4027 is a 64K x 16 static RAM module constructed on an epoxy laminate (FR-4) substrate using 4 64K x 4 static RAMs in plastic SOJ packages. The IDT7MP4027 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MP4027 is packaged in a 40 pin DSIP (Dual Single In-line vertical Package). This configuration allows 40 pins to be placed on a package 2 inches long, 0.35 inches thick and 0.5 inches tall.

All inputs and outputs of the IDT7MP4027 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

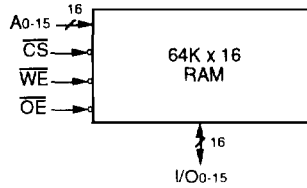
## PIN CONFIGURATION



DSIP  
TOP VIEW

2843 drw 01

## FUNCTIONAL BLOCK DIAGRAM



2843 drw 02

## PIN NAMES

A0-15	Addresses
I/O0-15	Data Inputs/Outputs
CS	Chip Select
WE	Write Enable
OE	Output Enable
NC	No Connect
VCC	Power
GND	Ground

2843 tbl 01

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COMMERCIAL TEMPERATURE RANGE

APRIL 1992

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**CAPACITANCE** (TA = +25°C, F = 1.0MHZ)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>I/O</sub>	Data I/O Capacitance	V <sub>(IN)</sub> = 0V	15	pF
C <sub>IN</sub>	Input Capacitance (Address and Control)	V <sub>(IN)</sub> = 0V	40	pF

**NOTE:** 2843 tbl 02  
1. This parameter is guaranteed by design but not tested.

**TRUTH TABLE**

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATA <sub>OUT</sub>	Active
Write	L	X	L	DATA <sub>IN</sub>	Active
Read	L	H	H	High-Z	Active

2843 tbl 05

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:** 2843 tbl 03  
1. V<sub>IL</sub> (min) = -1.5V for pulse width less than 10ns.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-10 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	50	mA

**NOTE:** 2843 tbl 06  
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V ± 10%

2843 tbl 04

**DC ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V ± 10%, T<sub>A</sub> = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage	V <sub>CC</sub> = Max.; V <sub>IN</sub> = GND to V <sub>CC</sub> (Address and Control)	—	40	μA
I <sub>LI</sub>	Input Leakage (Data)	V <sub>CC</sub> = Max.; V <sub>IN</sub> = GND to V <sub>CC</sub>	—	10	μA
I <sub>LO</sub>	Output Leakage	V <sub>CC</sub> = Max.; $\overline{CS}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	10	μA
V <sub>OL</sub>	Output Low	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8mA	—	0.4	V
V <sub>OH</sub>	Output High	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4mA	2.4	—	V

2843 tbl 07

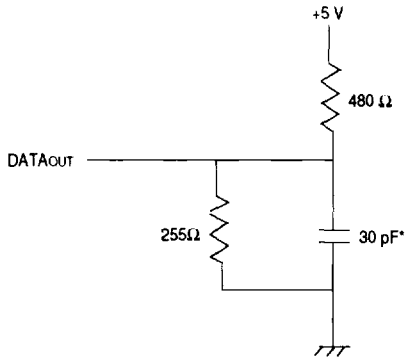
Symbol	Parameter	Test Conditions	7MP4027B Max.	7MP4027S Max.	Unit
I <sub>CC</sub>	Dymanic Operating Current	f = f <sub>MAX</sub> ; $\overline{CS}$ = V <sub>IL</sub> V <sub>CC</sub> = Max.; Output Open	720	640	mA
I <sub>SB</sub>	Standby Supply Current	$\overline{CS}$ ≥ V <sub>IH</sub> , V <sub>CC</sub> = Max. Outputs Open, f = f <sub>MAX</sub>	—	160	mA
I <sub>SB1</sub>	Full Standby Supply Current	$\overline{CS}$ ≥ V <sub>CC</sub> - 0.2V; f = 0 V <sub>IN</sub> > V <sub>CC</sub> - 0.2V or < 0.2V	—	120	mA

2843 tbl 08

**AC TEST CONDITIONS**

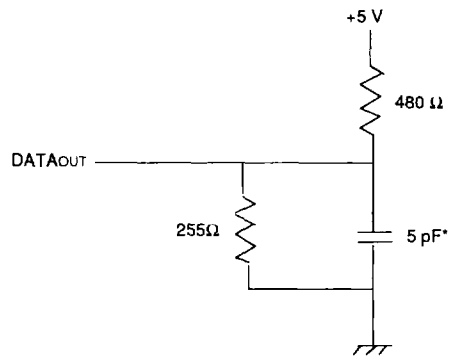
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2843 tbi 09



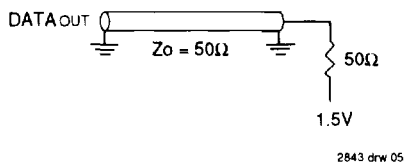
2843 drw 03

Figure 1. Output Load.



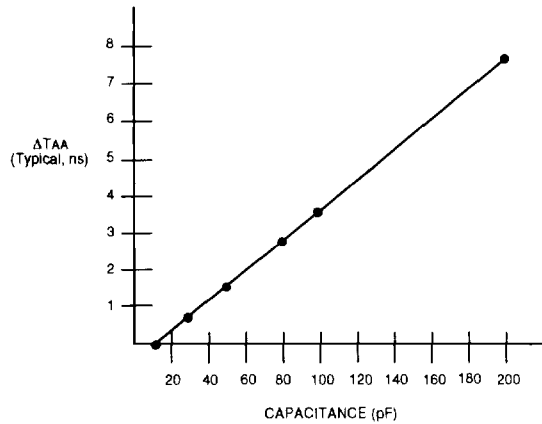
2843 drw 04

Figure 2. Output Load  
(for tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, and tOW)



2843 drw 05

Figure 3. Alternate Output Load.



2843 drw 06

Figure 4. Alternate Lumped Capacitive Load,  
Typical Derating.

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**AC ELECTRICAL CHARACTERISTICS**

(VCC = 5V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP4027BxxV								Unit
		-10 <sup>(2)</sup>		-12 <sup>(2)</sup>		-15		-17		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
tRC	Read Cycle Time	10	—	12	—	15	—	17	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	17	ns
tACS	Chip Select Access Time	—	4	—	5	—	6	—	8	ns
tCLZ <sup>(1)</sup>	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
tOE	Output Enable to Output Valid	—	4	—	5	—	6	—	8	ns
tOLZ <sup>(1)</sup>	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
tCHZ <sup>(1)</sup>	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	10	ns
tOHZ <sup>(1)</sup>	Output Disable to Output in High Z	—	3	—	4	—	5	—	6	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
<b>Write Cycle</b>										
tWC	Write Cycle Time	10	—	12	—	15	—	17	—	ns
tCW	Chip Select to End of Write	7	—	8	—	9	—	10	—	ns
tAW	Address Valid to End of Write	8	—	9	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	9	—	10	—	12	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ <sup>(1)</sup>	Write Enable to Output in High Z	—	4	—	5	—	6	—	7	ns
tDW	Data to Write Time Overlap	4	—	5	—	6	—	8	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW <sup>(1)</sup>	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

**NOTES:**

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2843 tbr 10

**AC ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = 5V ±10%, T<sub>A</sub> = 0°C to +70°C)

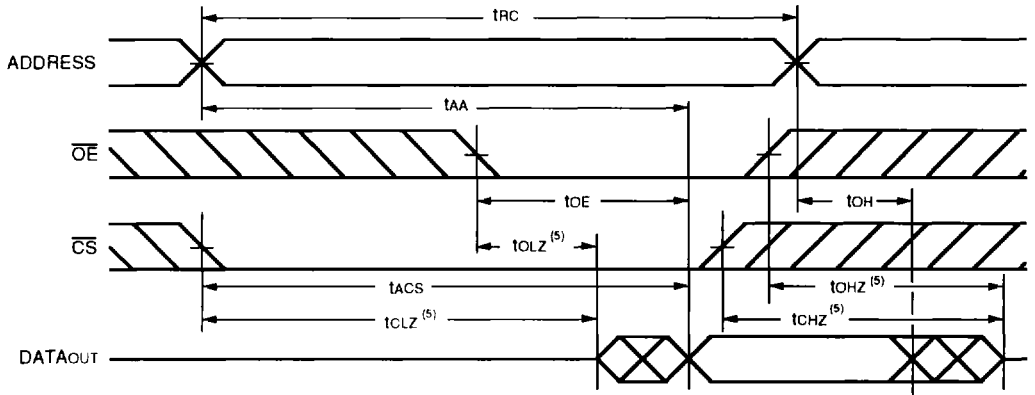
Symbol	Parameter	7MP4027SxxV								Unit
		-20		-25		-30		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	20	—	25	—	30	—	35	—	ns
t <sub>AA</sub>	Address Access Time	—	20	—	25	—	30	—	35	ns
t <sub>ACS</sub>	Chip Select Access Time	—	20	—	25	—	30	—	35	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select to Output in Low Z	4	—	4	—	4	—	4	—	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	12	—	12	—	15	—	20	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Deselect to Output in High Z	—	10	—	15	—	20	—	20	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Disable to Output in High Z	—	10	—	15	—	20	—	20	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t <sub>PU</sub> <sup>(1)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(1)</sup>	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	ns
<b>Write Cycle</b>										
t <sub>WC</sub>	Write Cycle Time	20	—	25	—	30	—	35	—	ns
t <sub>CW</sub>	Chip Select to End of Write	15	—	20	—	25	—	30	—	ns
t <sub>AW</sub>	Address Valid to End of Write	15	—	20	—	25	—	30	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	15	—	20	—	25	—	30	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable to Output in High Z	—	10	—	15	—	20	—	20	ns
t <sub>DW</sub>	Data to Write Time Overlap	12	—	15	—	17	—	20	—	ns
t <sub>DH</sub>	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(1)</sup>	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

**NOTE:**

1. This parameter is guaranteed by design, but not tested.

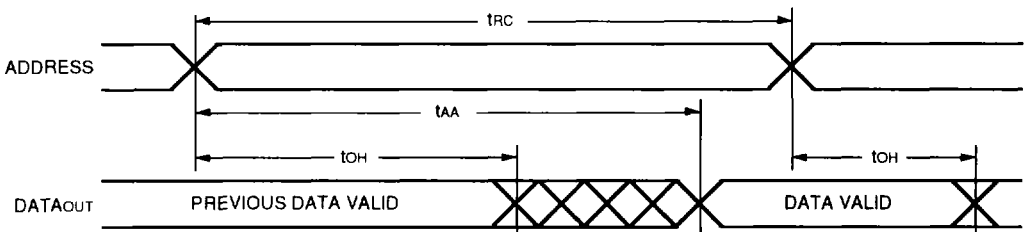
2843 tbl 11

**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**



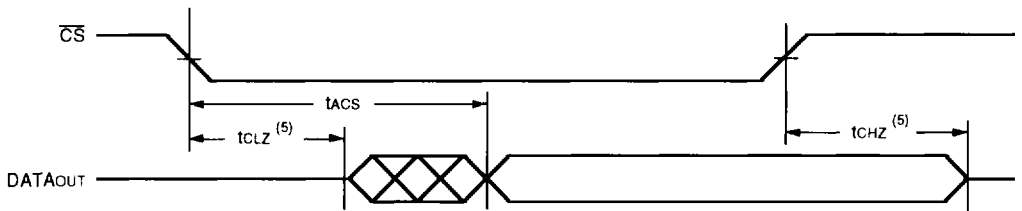
2843 drw 07

**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1,2,4)</sup>**



2843 drw 08

**TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1,3,4)</sup>**

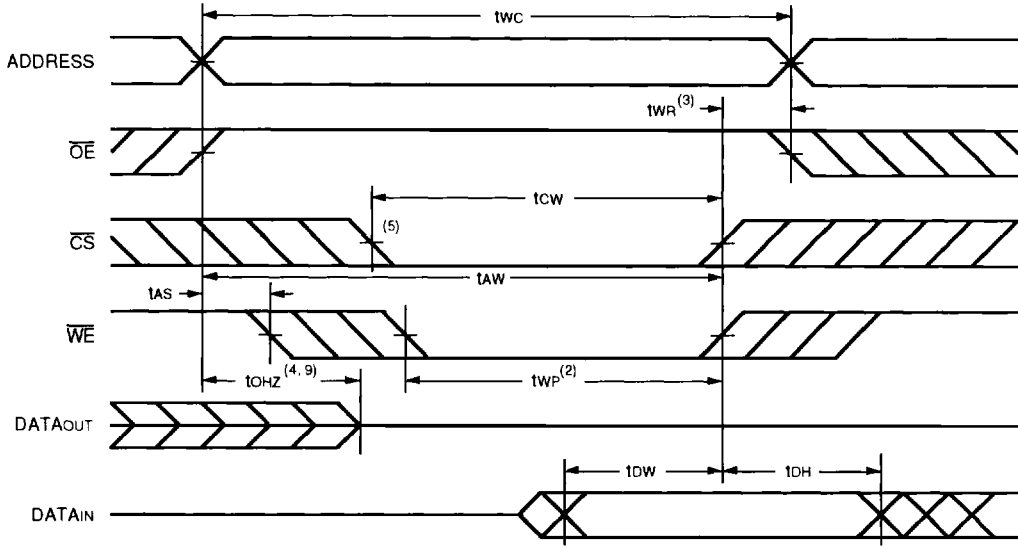


2843 drw 09

**NOTES:**

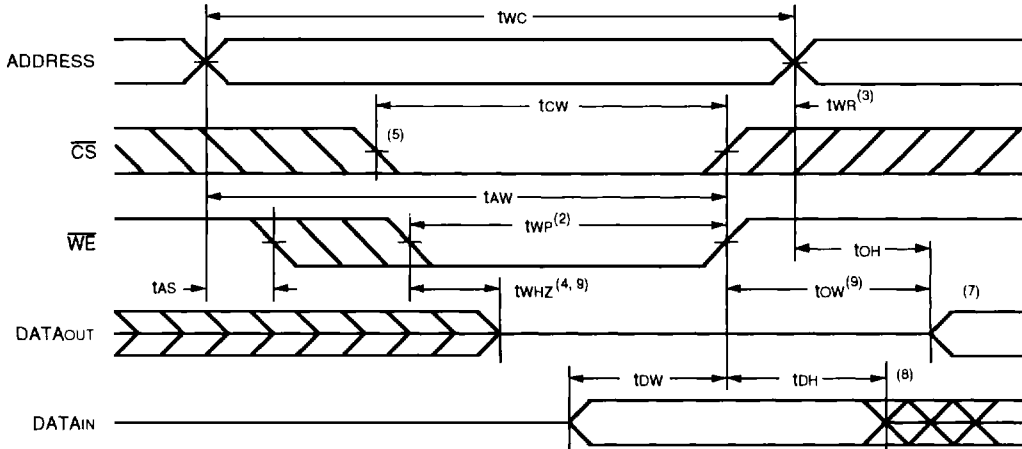
1. WE is High for Read Cycle.
2. Device is continuously selected. CS = V<sub>IL</sub>.
3. Address valid prior to or coincident with CS transition low.
4. OE = V<sub>IL</sub>.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1, 2, 3, 7)</sup>**



2843 drw 10

**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1, 2, 3, 5)</sup>**



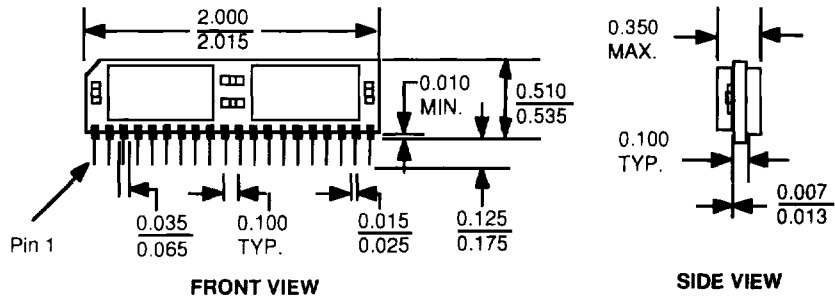
2843 drw 11

**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be high during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS}$  low transition occurs simultaneously with or after the  $\overline{WE}$  low transition, the outputs remain in a high impedance state.
6. Transition is measured  $\pm 200mV$  from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a  $\overline{WE}$  controlled write cycle, write pulse ( $t_{WP}$ ) >  $t_{WHZ} + t_{OW}$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is high during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

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PACKAGE DIMENSIONS



2843 drw 12