STB80NE06-10

N-CHANNEL 60V - 0.085 Ω - 80A D²PAK "SINGLE FEATURE SIZE™" POWER MOSFET

Table 1. General Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB80NE06-10	60 V	< 0.01 Ω	80 A

FEATURES SUMMARY

- TYPICAL $R_{DS(on)}$ = 0.085 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE

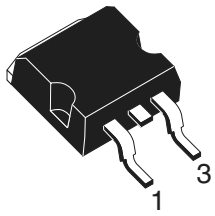
DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC CONVERTERS
- AUTOMOTIVE ENVIRONMENT

Figure 1. Package



TO-263
D²PAK
(suffix "T4")

Figure 2. Internal Schematic Diagram

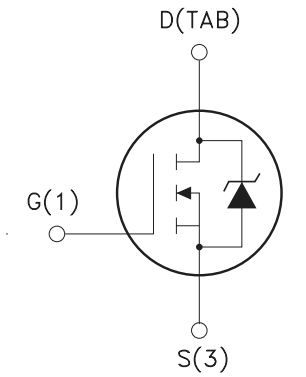


Table 2. Order Codes

Part Number	Marking	Package	Packaging
STB80NE06-10T4	B80NE06	D²PAK	TAPE & REEL

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (cont.) at T_C = 25 °C	80	A
I_D	Drain Current (cont.) at T_C = 100 °C	57	A
I_{DM} (1)	Drain Current (pulsed)	320	A
P_{tot}	Total Dissipation at T_C = 25 °C	150	W
	Derating Factor	1	W°/C
dv/dt (2)	Peak Diode Recovery voltage slope	7	V/ns
T_{stg}	Storage Temperature	-65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

Note: 1. Pulse width limited by safe operating area
2. I_{SD} ≤80 A, di/dt ≤ 300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 4. Thermal Data

Symbol	Parameter		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

Table 5. Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, δ < 1%)	80	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C; $I_D = I_{AR}$; V_{DD} = 30 V)	250	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Table 6. Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 mA; V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (VGS = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating Tc = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (VDS = 0)	V_{GS} = ± 20 V			± 100	nA

Table 7. On (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}; I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V; I_D = 40 A		8.5	10	mΩ

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Table 8. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$; I_D = 40 A	19	38		S
C_{iss}	Input Capacitance	V_{DS} = 25 V; f = 1 MHz; V_{GS} = 0		7600	10000	pF
C_{oss}	Output Capacitance			890	1100	pF
C_{rss}	Reverse Transfer Capacitance			150	200	pF

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Table 9. Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	V_{DD} = 30 V; I_D = 40 A; R_G = 4.7 Ω; V_{GS} = 10 V (see test circuit, Figure 16)		50	65	ns
t_r	Rise Time			150	200	ns
Q_g	Total Gate Charge	V_{DD} = 48 V; I_D = 80 A; V_{GS} = 10 V		140		nC
Q_{gs}	Gate-Source Charge			20		nC
Q_{gd}	Gate-Drain Charge			50		nC

Table 10. Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 48 V; I_D = 40 A; R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, Figure 18)		45	60	ns
t_r	Fall Time			75	100	ns
t_c	Cross-over Time			130	170	ns

Table 11. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				80	A
I_{SDM} (1)	Source-drain Current (pulsed)				320	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 80 A; V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 80 A; di/dt = 100 A/µs; V_{DD} = 30 V; T_j = 150 °C(see test circuit, Figure 18)		100		ns
Q_{rr}	Reverse Recovery Charge			0.4		nC
I_{rrm}	Reverse Recovery Current			8		A

Note: 1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Figure 3. Safe Operating Area

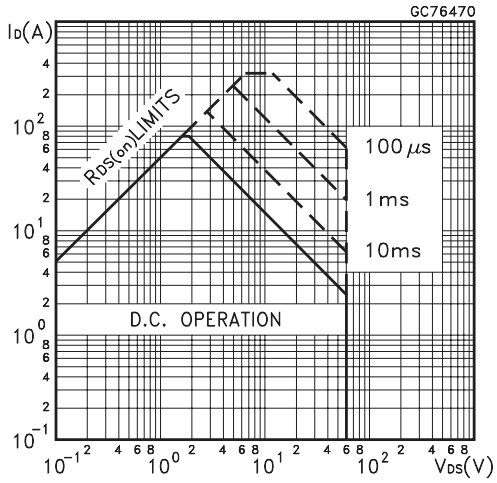


Figure 4. Thermal Impedance

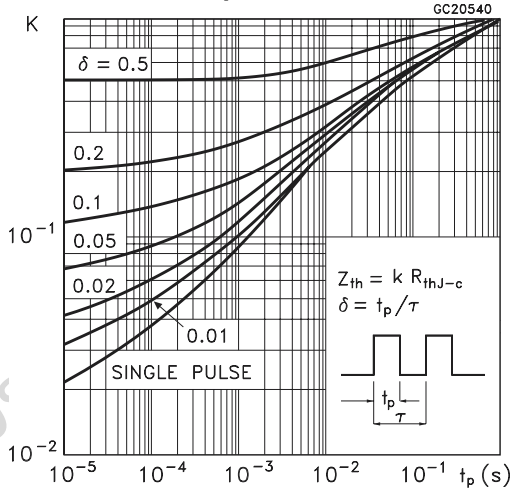


Figure 5. Output Characteristics

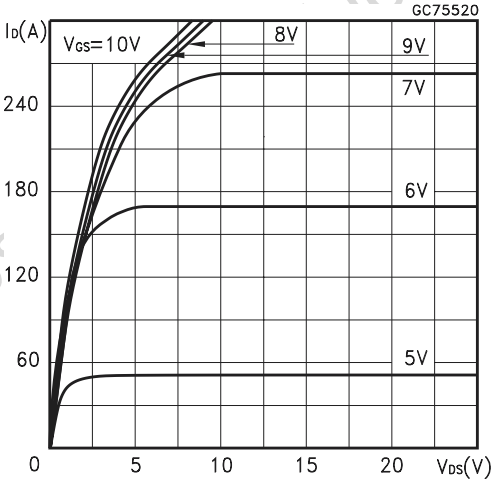


Figure 6. Transfer Characteristics

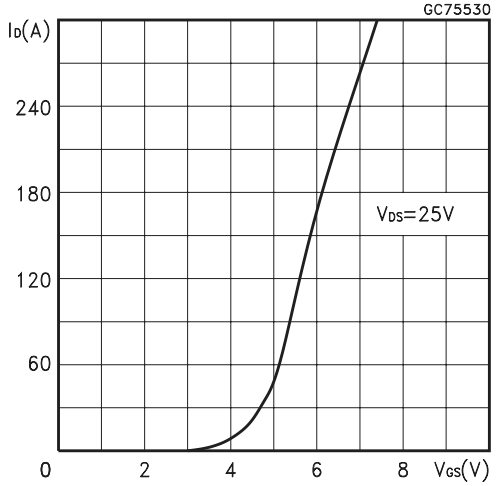


Figure 7. Transconductance

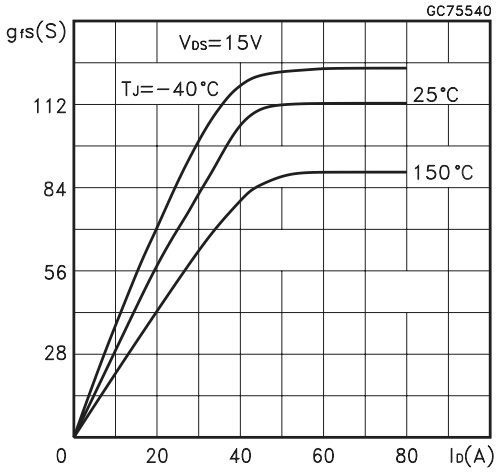


Figure 8. Static Drain-source On Resistance

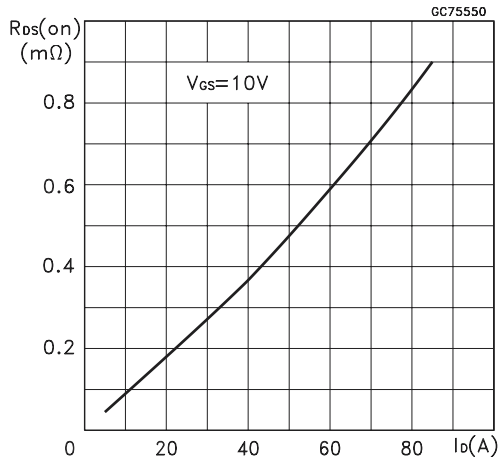


Figure 9. Gate Charge vs Gate-source Voltage

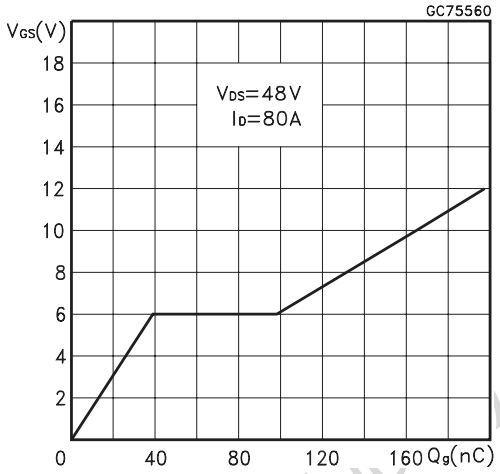


Figure 10. Capacitance Variations

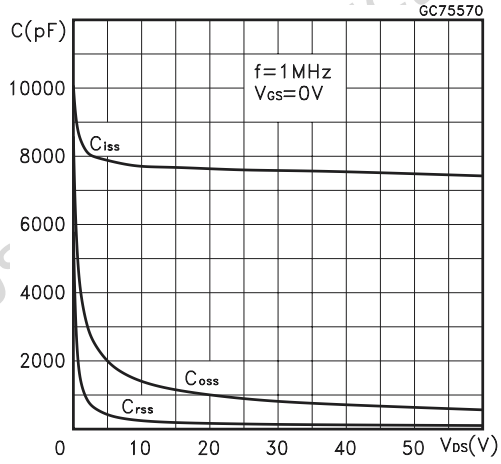


Figure 11. Normalized Gate Thresold Voltage vs Temperature

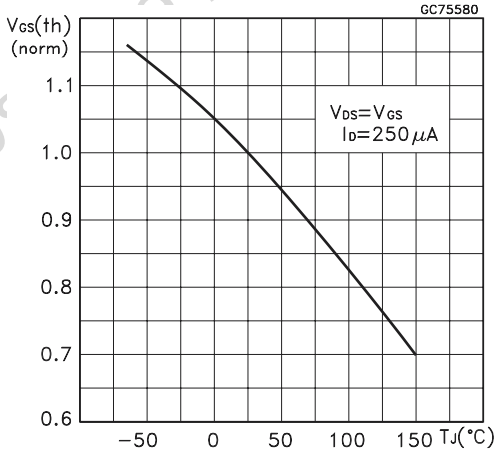


Figure 12. Normalized on Resistance vs Temperature

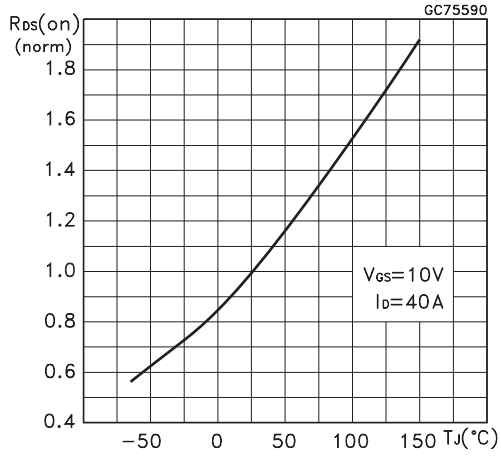


Figure 13. Source-drain Diode Forward Characteristics

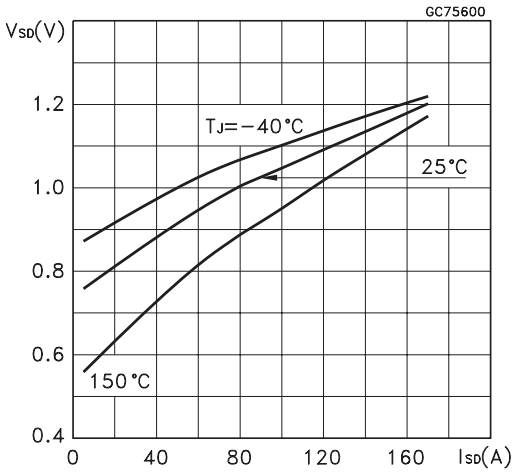


Figure 14. Unclamped Inductive Load Test Circuit

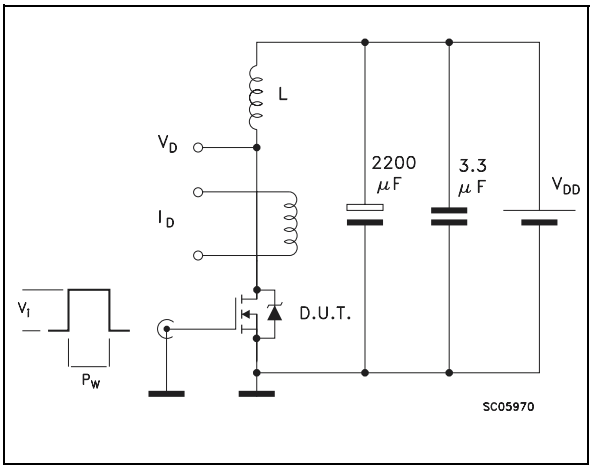


Figure 15. Unclamped Inductive Waveforms

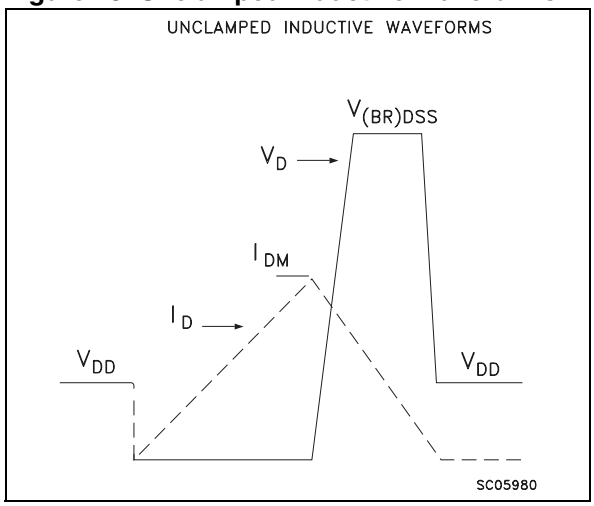


Figure 16. Switching Time Test Circuit For Resistive Load

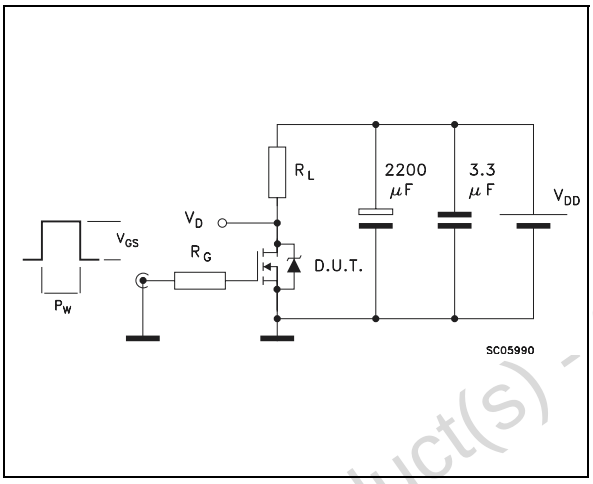


Figure 17. Gate Charge Test Circuit

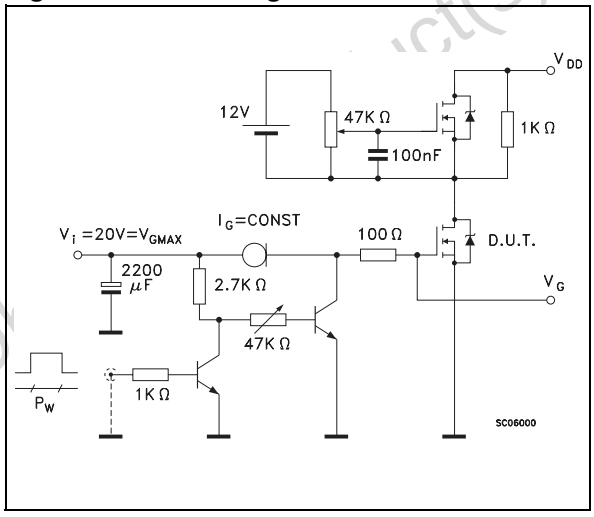
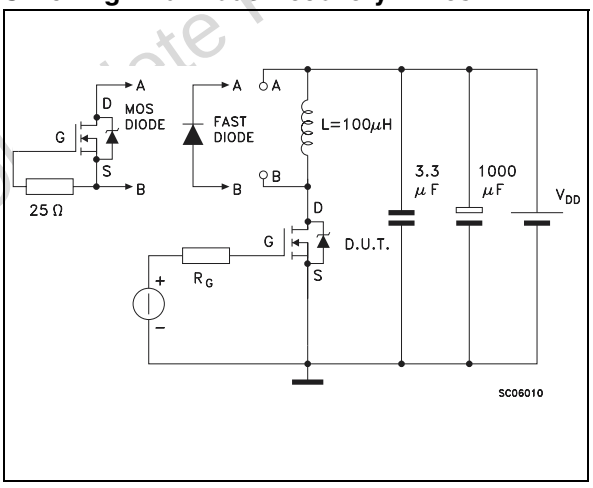


Figure 18. Test Circuit For Inductive Load Swiching And Diode Recovery Times

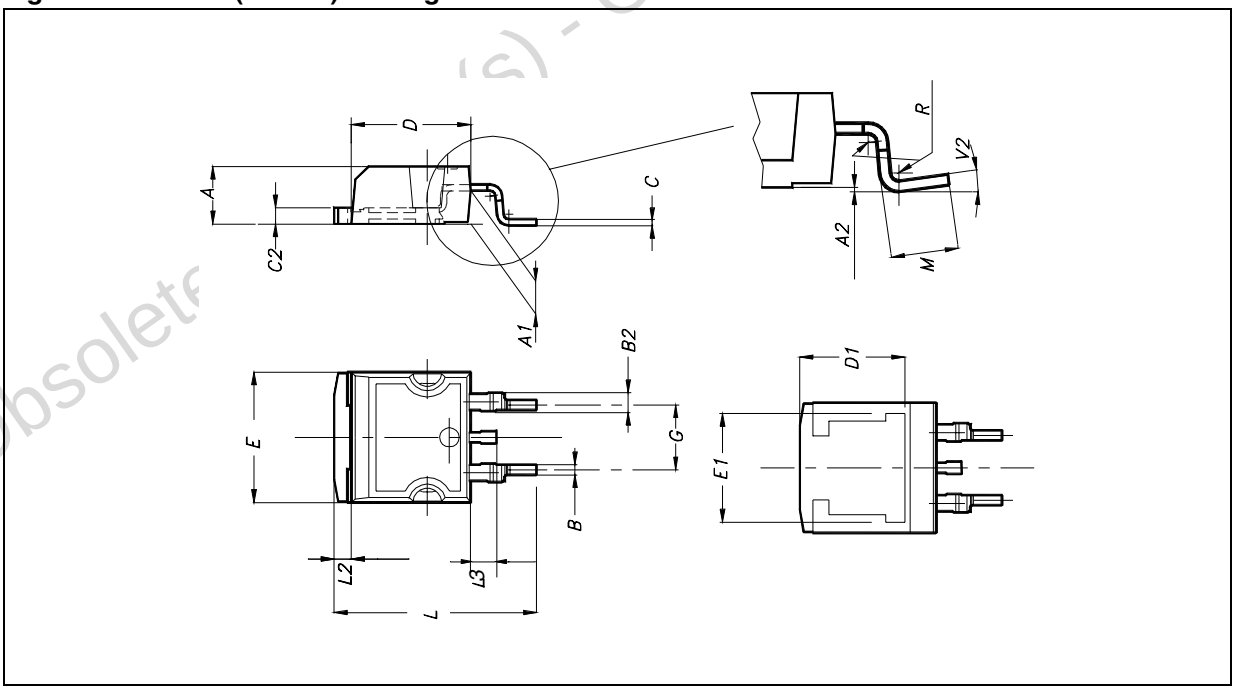


PACKAGE MECHANICAL

Table 12. TO-263 (D^2PAK) Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

Figure 19. TO-263 (D^2PAK) Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY

Table 13. Revision History

Date	Revision	Description of Changes
February-1998	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.