FQD2N60C / FQU2N60C

N-Channel QFET® MOSFET

600 V, 1.9 A, 4.7 Ω

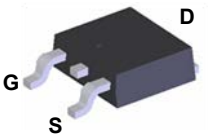
Features

- 1.9 A, 600 V, $R_{DS(on)}$ = 4.7 Ω (Max.) @ V_{GS} = 10 V, I_D = 0.95 A
- Low Gate Charge (Typ. 8.5 nC)
- Low Crss (Typ. 4.3 pF)
- 100% Avalanche Tested
- RoHS Compliant

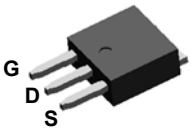
Description

These N-Channel enhancement mode power field effect transistors are produced using Corise Semiconductorÿs proprietary, planar stripe, DMOS technology.

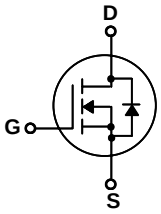
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.



D-PAK



I-PAK



Absolute Maximum Ratings

Symbol	Parameter		FQD2N60C / FQU2N60C	Unit
V_{DSS}	Drain-Source Voltage		600	V
I_D	Drain Current - Continuous (T_C = 25°C)		1.9	A
	- Continuous (T_C = 100°C)		1.14	A
I_{DM}	Drain Current - Pulsed	(Note 1)	7.6	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	120	mJ
I_{AR}	Avalanche Current	(Note 1)	1.9	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)*		2.5	W
	Power Dissipation (T_C = 25°C)		44	W
	- Derate above 25°C		0.35	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQD2N60C / FQU2N60C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.87	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD2N60C	FQD2N60C	D-PAK	-	-	
FDU2N60C	FDU2N60C	I-PAK	-	-	

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	600	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 480 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.95 A	--	3.6	4.7	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 0.95 A (Note 4)	--	5.0	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	180	235	pF
C_{oss}	Output Capacitance		--	20	25	pF
C_{rss}	Reverse Transfer Capacitance		--	4.3	5.6	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 2 A, R_G = 25 Ω	--	9	28	ns
t_r	Turn-On Rise Time		--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	24	58	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	28	66	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 2 A, V_{GS} = 10 V	--	8.5	12	nC
Q_{gs}	Gate-Source Charge		--	1.3	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	4.1	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	7.6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.9 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2 A, dI_F / dt = 100 A/μs (Note 4)	--	230	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.0	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 56mH, I_{AS} = 2A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 2A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Figure 1. On-Region Characteristics

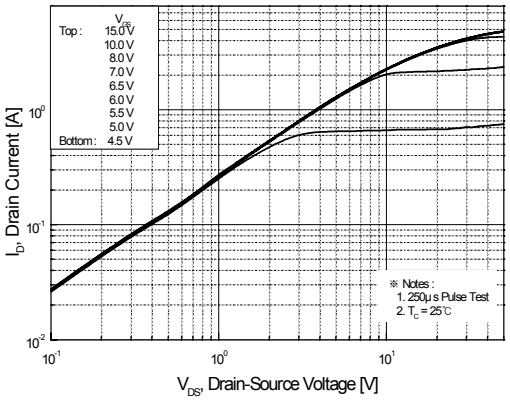


Figure 2. Transfer Characteristics

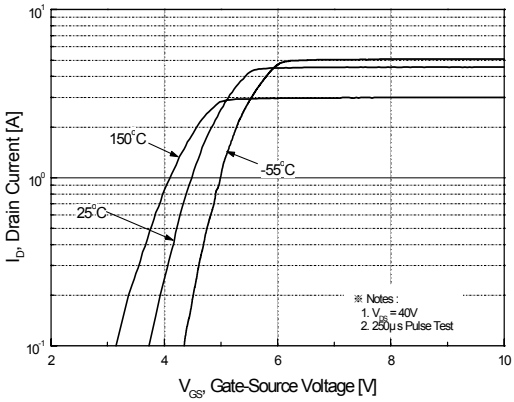


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

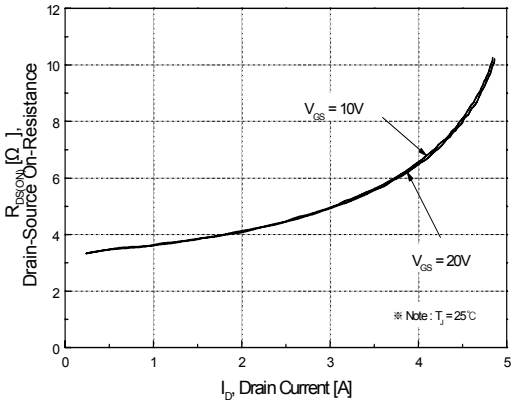


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

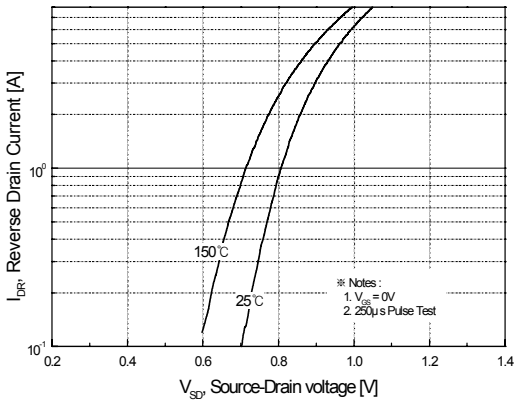


Figure 5. Capacitance Characteristics

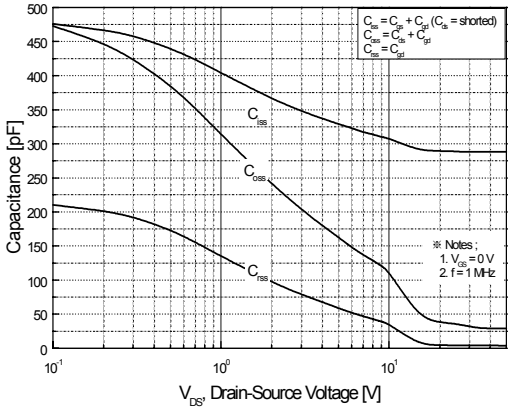


Figure 6. Gate Charge Characteristics

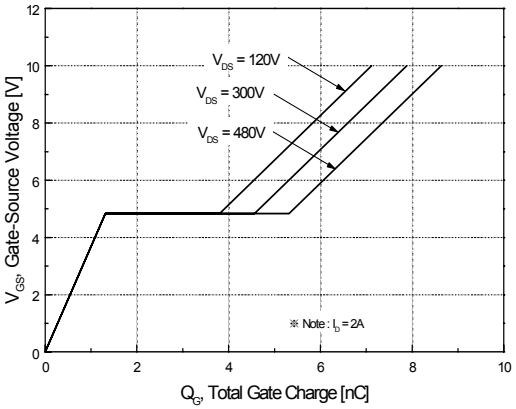


Figure 7. Breakdown Voltage Variation vs. Temperature

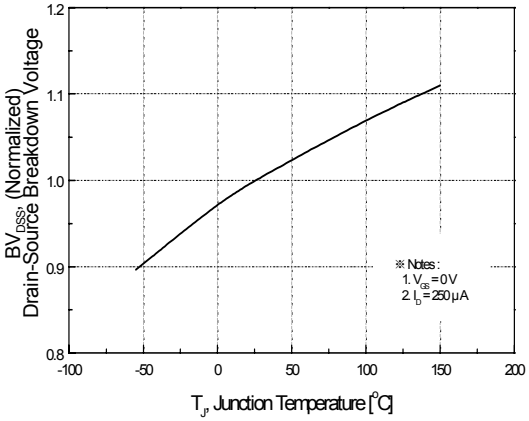


Figure 8. On-Resistance Variation vs. Temperature

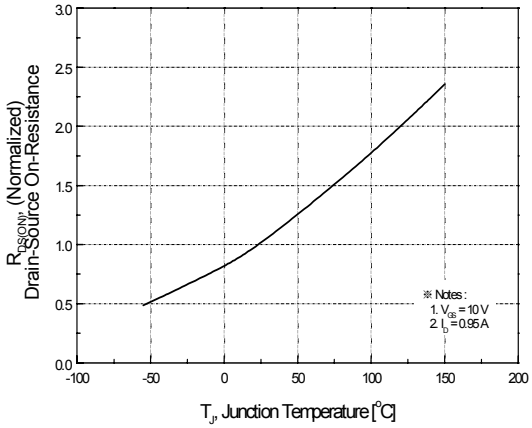


Figure 9. Maximum Safe Operating Area

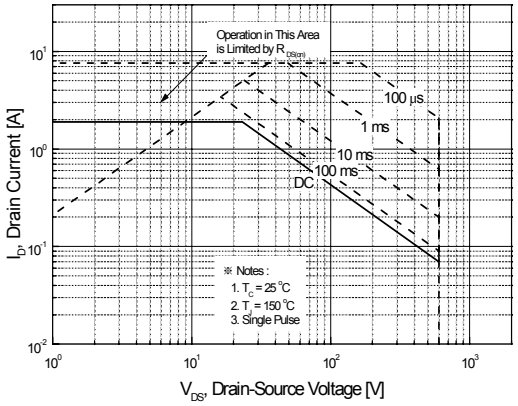


Figure 10. Maximum Drain Current vs. Case Temperature

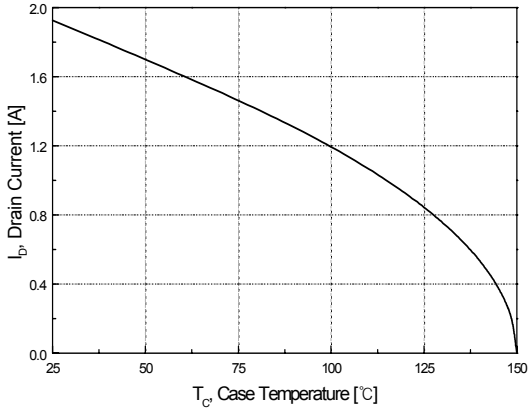
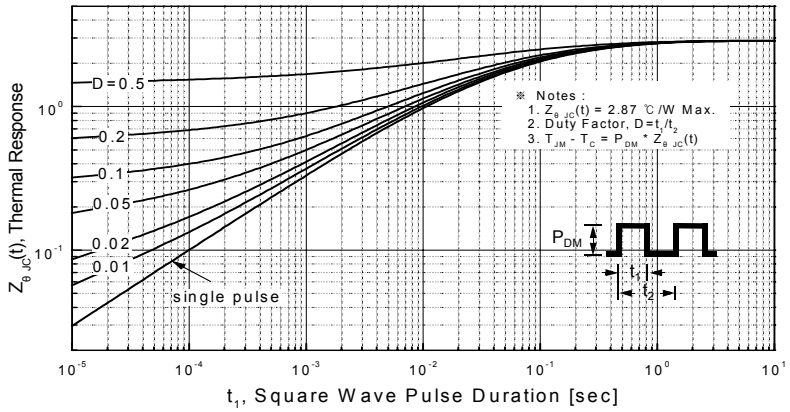
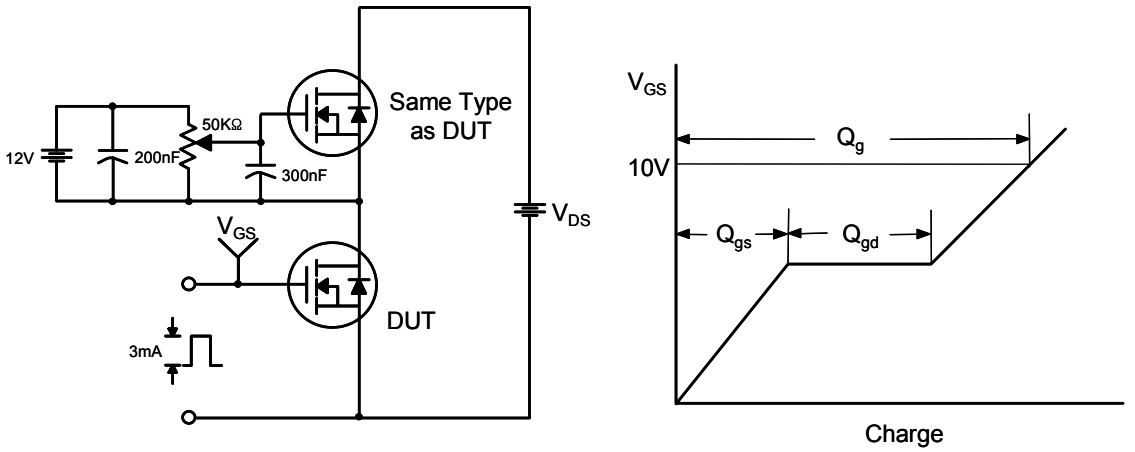


Figure 11. Typical Drain Current Slope vs. Gate Resistance

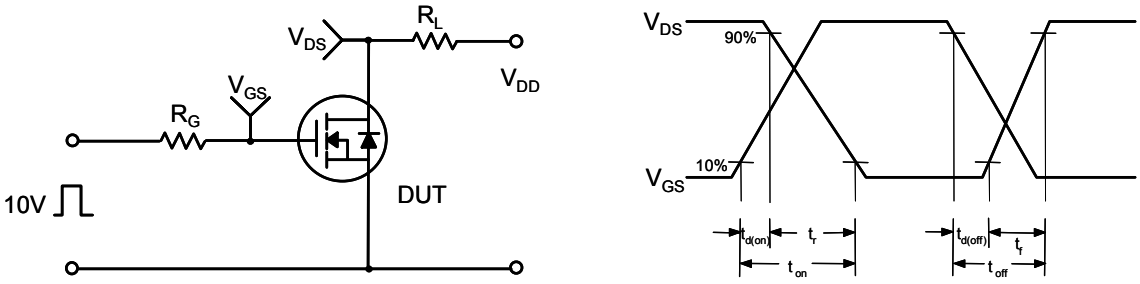
Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance



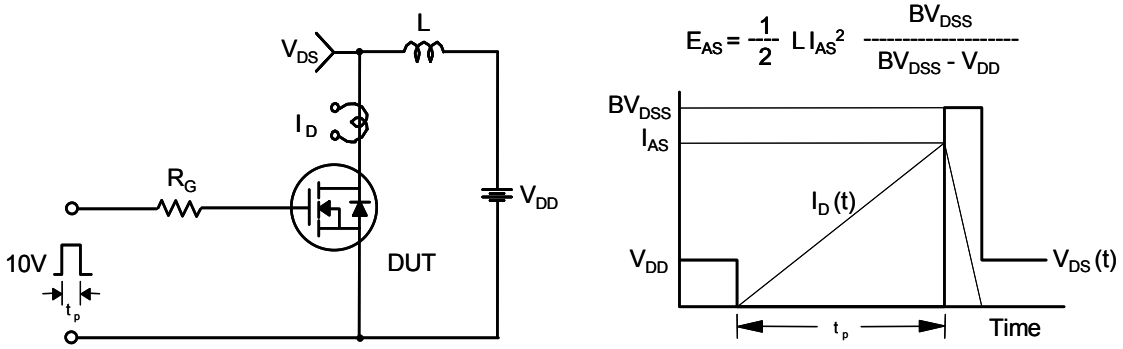
Gate Charge Test Circuit & Waveform

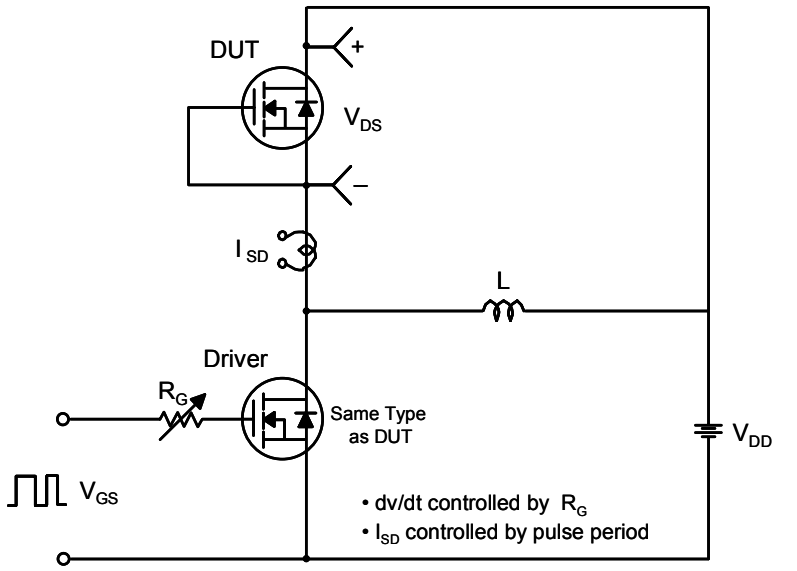


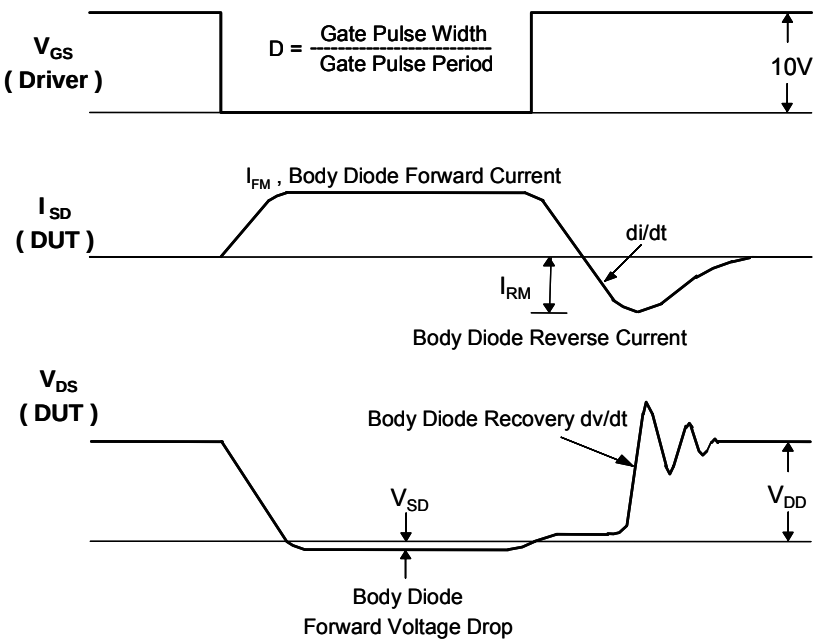
Resistive Switching Test Circuit & Waveforms



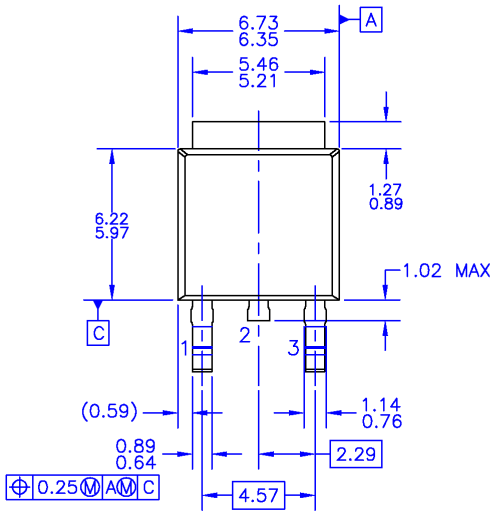
Unclamped Inductive Switching Test Circuit & Waveforms

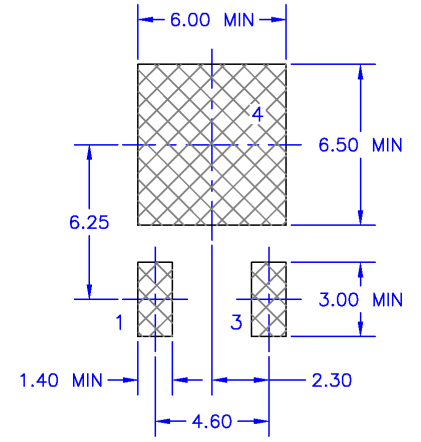



DUT
+
V_{DS}
–
I_{SD}
L
Driver
R_G
Same Type
as DUT
V_{DD}
V_{GS}
• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

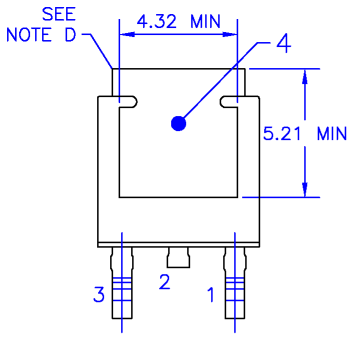

V_{GS}
(Driver)
D = Gate Pulse Width / Gate Pulse Period
10V
I_{FM} , Body Diode Forward Current
I_{SD}
(DUT)
di/dt
I_{RM}
Body Diode Reverse Current
V_{DS}
(DUT)
Body Diode Recovery dv/dt
V_{SD}
V_{DD}
Body Diode
Forward Voltage Drop

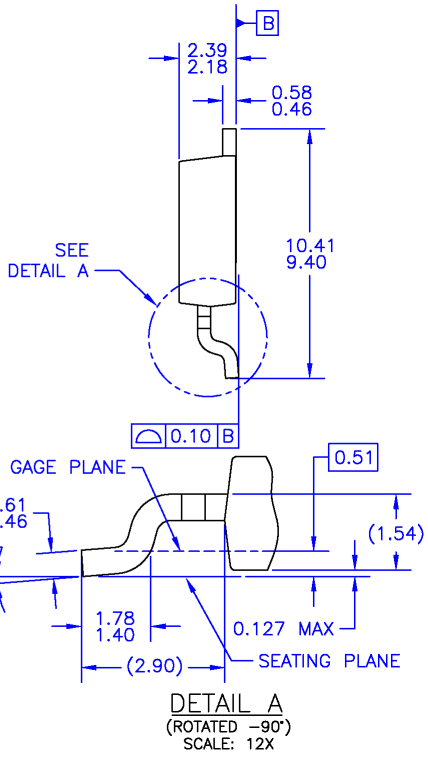
D-PAK





LAND PATTERN RECOMMENDATION



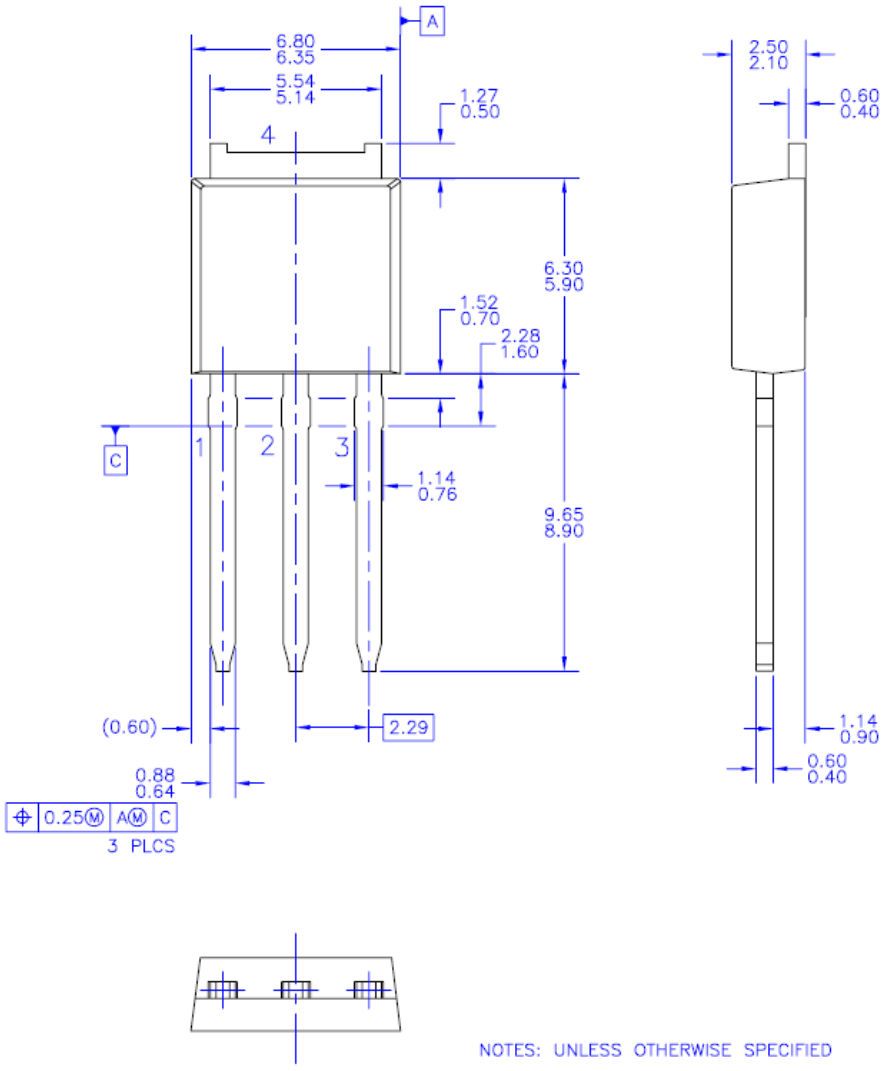


DETAIL A
(ROTATED −90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238−3N.
H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

I-PAK



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A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.