Microprocessor Reset Monitors

FEATURES

- Tight Reset Voltage Tolerances ±1.5%
- 4 Reset Active Timeout Period Options
- Low Quiescent Current: < 3 A
- 6 Reset Threshold Options From 2.63 V to 4.63 V
- Reset Output Guaranteed Down to 1.0 V
- No External Components
- V_{CC} Transient immunity
- Wide Temperature Range −40°C to + 85°C

APPLICATIONS

- Computers
- Critical μP/μC Power Supply Monitoring
- Battery Powered Equipment

DESCRIPTION

The SiP809C/SiP810C are system supervisor circuits designed to monitor V_{CC} in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

When the processor power supply voltage drops below the reset threshold, the reset output is driven active, in less than 40 μs (T_{D1}). Reset is maintained active for a time period (T_{D2}), after the V_{cc} rises above the threshold voltage.

To prevent jitter, the reset threshold voltage has a built-in hysteresis of 0.4% of V_{TH}.

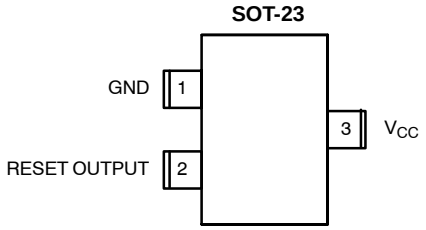
The SiP809C has an active-low $\overline{\text{RESET}}$ output, while the SiP810C has an active-high reset output. Both devices have push/pull output drives.

The reset signal is guaranteed valid, down to V_{CC} = 1.0 V.

Low supply current of 3 μA makes these devices well suited for battery powered applications. They are designed to reject fast transients from causing false resets.

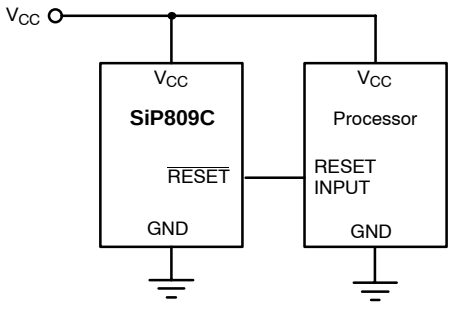
Both devices are available in a space-saving SOT-23 package.

PACKAGING AND PIN DEFINITION

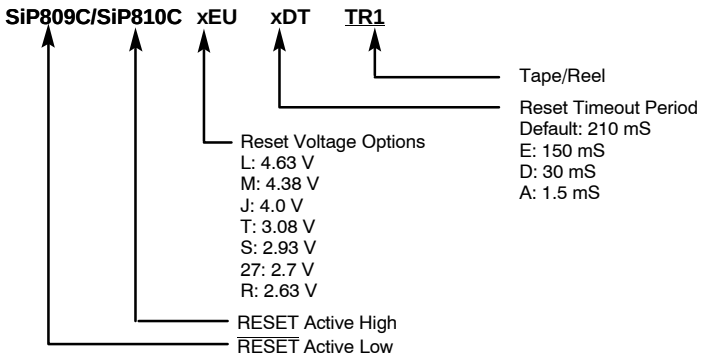


See page 2 for ordering and marking information.

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION



Please contact your local Vishay Semiconductor Sales Office for availability of other threshold voltage options.

MARKING INFORMATION-SiP809C	
SiP809CREUADT	DIxxx
SiP809C27EUADT	DKxxx
SiP809CSEUADT	DLxxx
SiP809CTEUADT	DMxxx
SiP809CJEUADT	DNxxx
SiP809CMEUADT	DOxxx
SiP809CLEUADT	DPxxx
SiP809CREUDDT	DSxxx
SiP809C27EUDDT	DTxxx
SiP809CSEEUDDT	DVxxx
SiP809CTEUDDT	DWxxx
SiP809CJEUDDT	DXxxx
SiP809CMEUDDT	DYxxx
SiP809CLEUDDT	DZxxx
SiP809CREUEDT	EBxxx
SiP809C27EUEDT	ECxxx
SiP809CSEUEDT	EDxxx
SiP809CTEUEDT	EExxx
SiP809CJEUEDT	EGxxx
SiP809CMEUEDT	EHxxx
SiP809CLEUEDT	EIxxx
SiP809CREUDT	ELxxx
SiP809C27EUDT	EMxxx
SiP809CSEUDT	ENxxx
SiP809CTEUDT	EOxxx
SiP809CJEUDT	EPxxx
SiP809CMEUDT	ERxxx
SiP809CCLEUDT	ESxxx

MARKING INFORMATION-SiP810C	
SiP810CREUADT	EVxxx
SiP810C27EUADT	EWxxx
SiP810CSEUADT	EXxxx
SiP810CTEUADT	EYxxx
SiP810CJEUADT	EZxxx
SiP810CMEUADT	FAxxx
SiP810CLEUADT	FBxxx
SiP810CREUDDT	FDxxx
SiP810C27EUDDT	FExxx
SiP810CSEUDDT	FGxxx
SiP810CTEUDDT	FHxxx
SiP810CJEUDDT	FIxxx
SiP810CMEUDDT	FKxxx
SiP810CLEUDDT	FLxxx
SiP810CREUEDT	FNxxx
SiP810C27EUEDT	FOxxx
SiP810CSEUEDT	FPxxx
SiP810CTEUEDT	FRxxx
SiP810CJEUEDT	FSxxx
SiP810CMEUEDT	FTxxx
SiP810CLEUDT	FVxxx
SiP810CREUDT	FXxxx
SiP810C27EUDT	FYxxx
SiP810CSEUDT	FZxxx
SiP810CTEUDT	GAxxx
SiP810CJEUDT	GBxxx
SiP810CMEUDT	GCxxx
SiP810CLEUDT	GDxxx

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

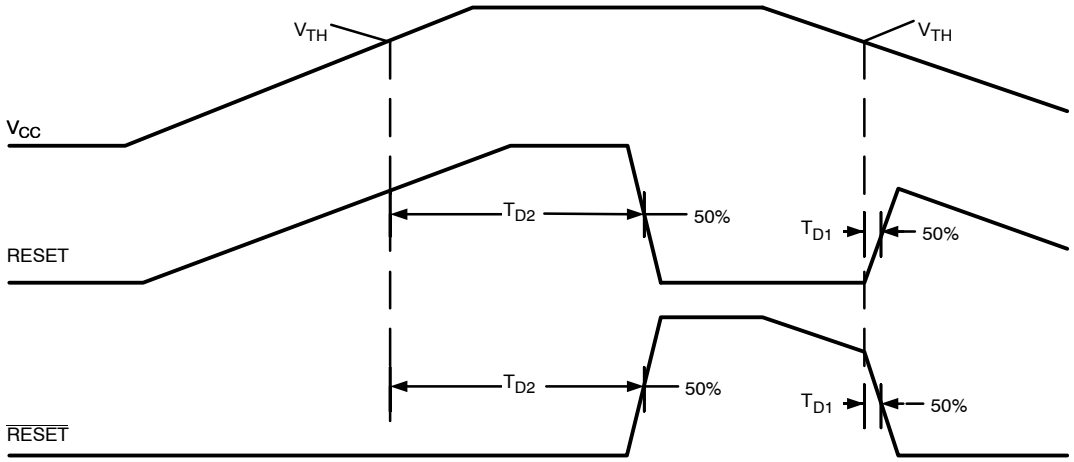
Parameter	Symbol	Limit	Unit
Supply Voltage	V_{CC}	6.0	V
RESET/$\overline{\text{RESET}}$		−0.3 to (V_{CC} + 0.3)	
Input Current	I_{CC}	20	mA
Output Current, RESET/$\overline{\text{RESET}}$		20	
dv/dt		100	V/µS
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	
Power Dissipation ($T_A \leq 70°C$) SOT-23 (Derate 4 mW/°C above 70°C)	P_D	260	mW

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified T_A = 25°C	Limits Min[a]	Typ[b]	Max[a]	Unit
V_{CC} Range	V_{RANGE}		1		5.5	V
		T_A = −40°C to 85°C	1		5.5	
Supply Current (Reset Not Active)	I_{CC}	V_{CC} = 3.0 V			3.0	µA
		V_{CC} = 3.0 V, T_A = −40°C to 85°C			5.0	
Reset Threshold	V_{TH}		$V_{TH(nom)}$ −1.5%	$V_{TH(nom)}$	$V_{TH(nom)}$ +1.5%	V
		T_A = −40°C to 85°C	$V_{TH(nom)}$ −2.0%	$V_{TH(nom)}$	$V_{TH(nom)}$ +2.0%	
Threshold Hysteresis	$V_{TH(hys)}$			0.4		%V_{TH}
Reset Threshold Temperature Coefficient				30		ppm/°C
Reset Output Voltage Low	V_{OL}	T_A = −40°C to 85°C, I_{SINK} = 1.2 mA SiP809C—V_{CC} < $V_{TH(min)}$ SiP810C—V_{CC} > $V_{TH(max)}$			0.5	V
Reset Output Voltage High	V_{OH}	T_A = −40°C to 85°C, I_{SOURCE}= 0.5 mA SiP809C—V_{CC} > $V_{TH(max)}$ SiP810C—V_{CC} < $V_{TH(min)}$	0.8 V_{CC}			
V_{CC} to Reset Delay	T_{D1}	V_{CC} = V_{TH} − 100 mV, T_A = −40°C to 85°C		40		µS
Reset Timeout Period	T_{D2}	T_A = −40°C to 85°C	$T_{D2(nom)}$ −35%	$T_{D2(nom)}$	$T_{D2(nom)}$ +35%	mS

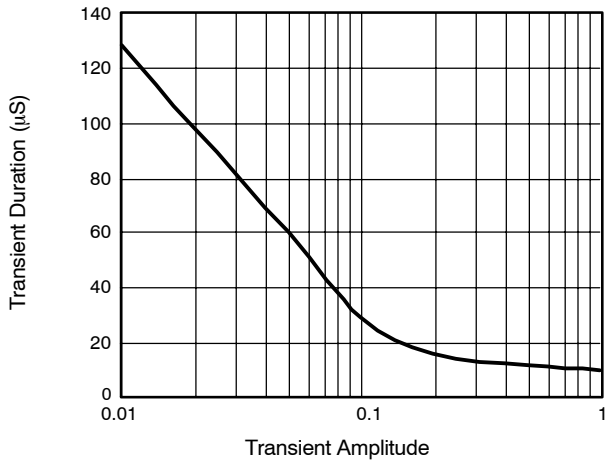
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.

TYPICAL CHARACTERISTICS (T_A = 25°C Unless Otherwise Noted)

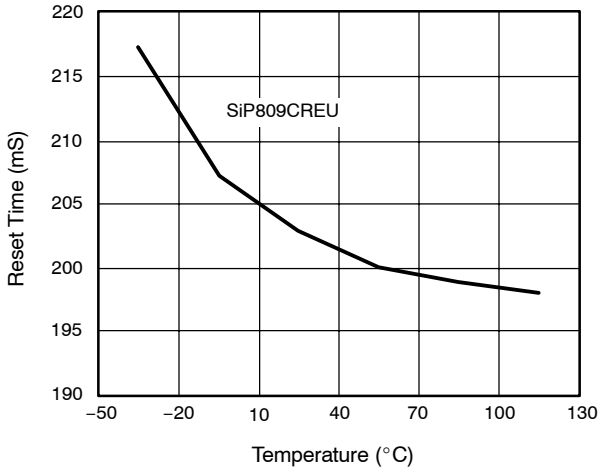


These devices have a certain immunity to fast negative going transients. The graph titled “Transient Rejection” shows the maximum allowable transient amplitude and duration to avoid triggering an unintended reset. As shown in the graph shorter transients can have larger amplitudes without triggering resets.

Transient Rejection

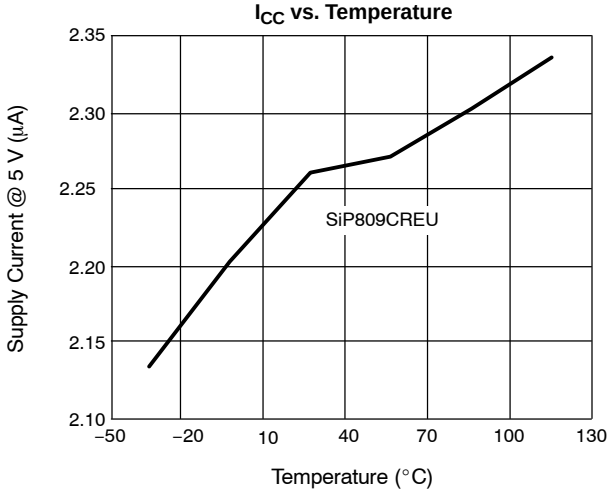


Reset Time vs. Temperature

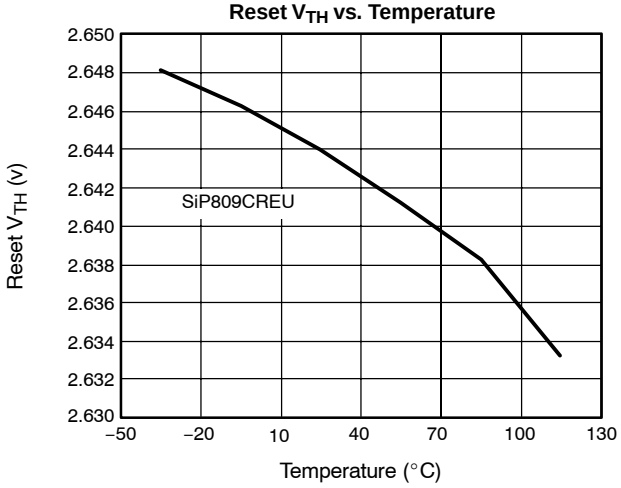


TYPICAL CHARACTERISTICS (T_A = 25°C Unless Otherwise Noted)

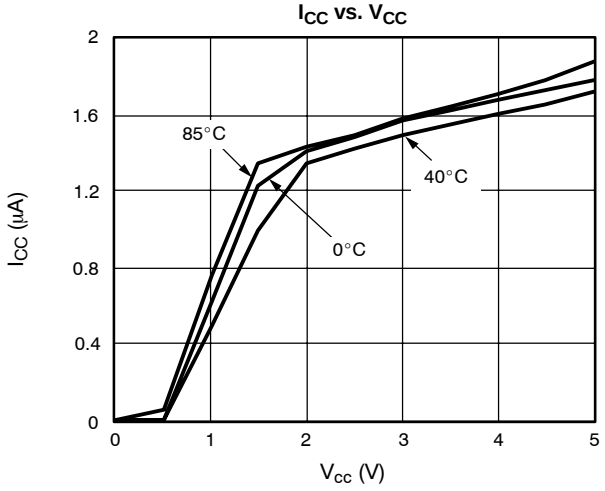
I_{CC} vs. Temperature



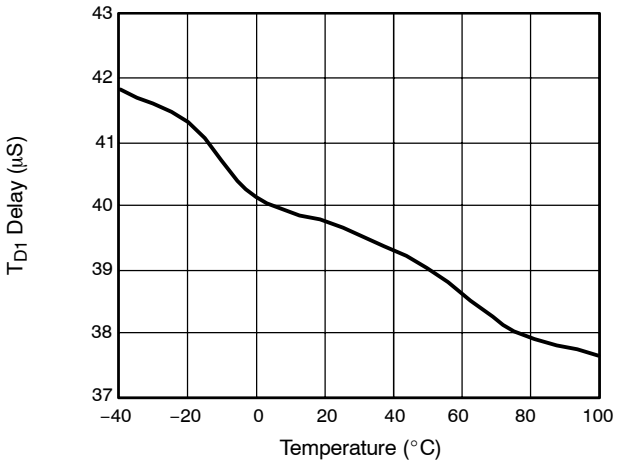
Reset V_{TH} vs. Temperature



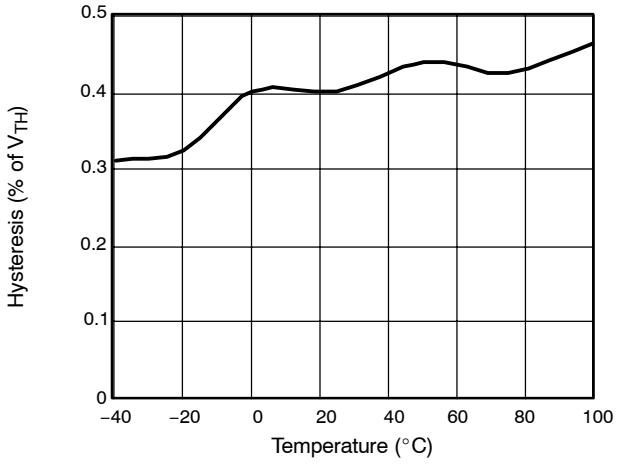
I_{CC} vs. V_{CC}



T_{D1} Delay vs. Temperature



Threshold Hysteresis vs. Temperature



Reset V_{OL} vs. Temperature