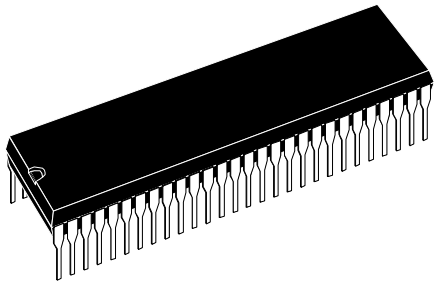
SGS-THOMSON MICROELECTRONICS

ST92195

64K ROM HCMOS MCU WITH ON-SCREEN-DISPLAY AND TELETEXT DATA SLICER

BRIEF DATA

- Register File based 8/16 bit Core Architecture with RUN, WFI, SLOW and HALT modes
- 0°C to +70°C Operating Temperature Range available
- Up to 24 MHz Operation @ 5V±10%
- Minimum instruction cycle time: 375nS at 16MHz internal clock
- 64K Bytes ROM
- 256 Bytes RAM of Register file (accumulators or index registers)
- 256 Bytes of on-chip static RAM
- 8K Bytes of TDSRAM (Teletext and Display RAM)
- 56-lead Shrink DIP package
- 28 fully programmable I/O pins
- Serial Peripheral Interface
- Flexible Clock controller for OSD, Data Slicer and Core clocks running from one single low frequency external crystal.
- Enhanced Display Controller with 26 rows of 40/80 characters
  - Serial and Parallel attributes
  - 10x10 dot Matrix, 512 ROM characters, definable by user
  - 4/3 and 16/9 supported
  - Rounding, fringe, double width, double height, scrolling, cursor, full background colour, semi-transparent mode and reduced intensity colour supported
- Teletext unit, including Data slicer, Acquisition Unit and up to 8K Bytes RAM for Data Storage
- VPS and Wide Screen Signalling slicer
- Integrated Sync Extractor and Sync Controller
- 14-bit Voltage Synthesis for tuning reference voltage
- Up to 6 External Interrupts plus 1 non-maskable interrupt



PSDIP56

(See end of Datasheet for Ordering Information)

- 8 x 8-bit programmable PWM outputs with 5V open-drain or push-pull capability
- 16-bit Watchdog timer with 8-bit prescaler
- 16-bit standard timer with 8-bit prescaler usable as a Watchdog timer
- 3-channel Analog-to-Digital converter; 6-bit guaranteed
- Rich instruction set and 14-Addressing modes
- Versatile Development Tools, including Assembler, Linker, C-compiler, Archiver, Source Level Debugger and Hardware Emulators with Real-Time Operating System available from third parties
- Piggyback board available for prototyping

1 DESCRIPTION OF THE ST92195

The ST92195 is a member of the ST9+ family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

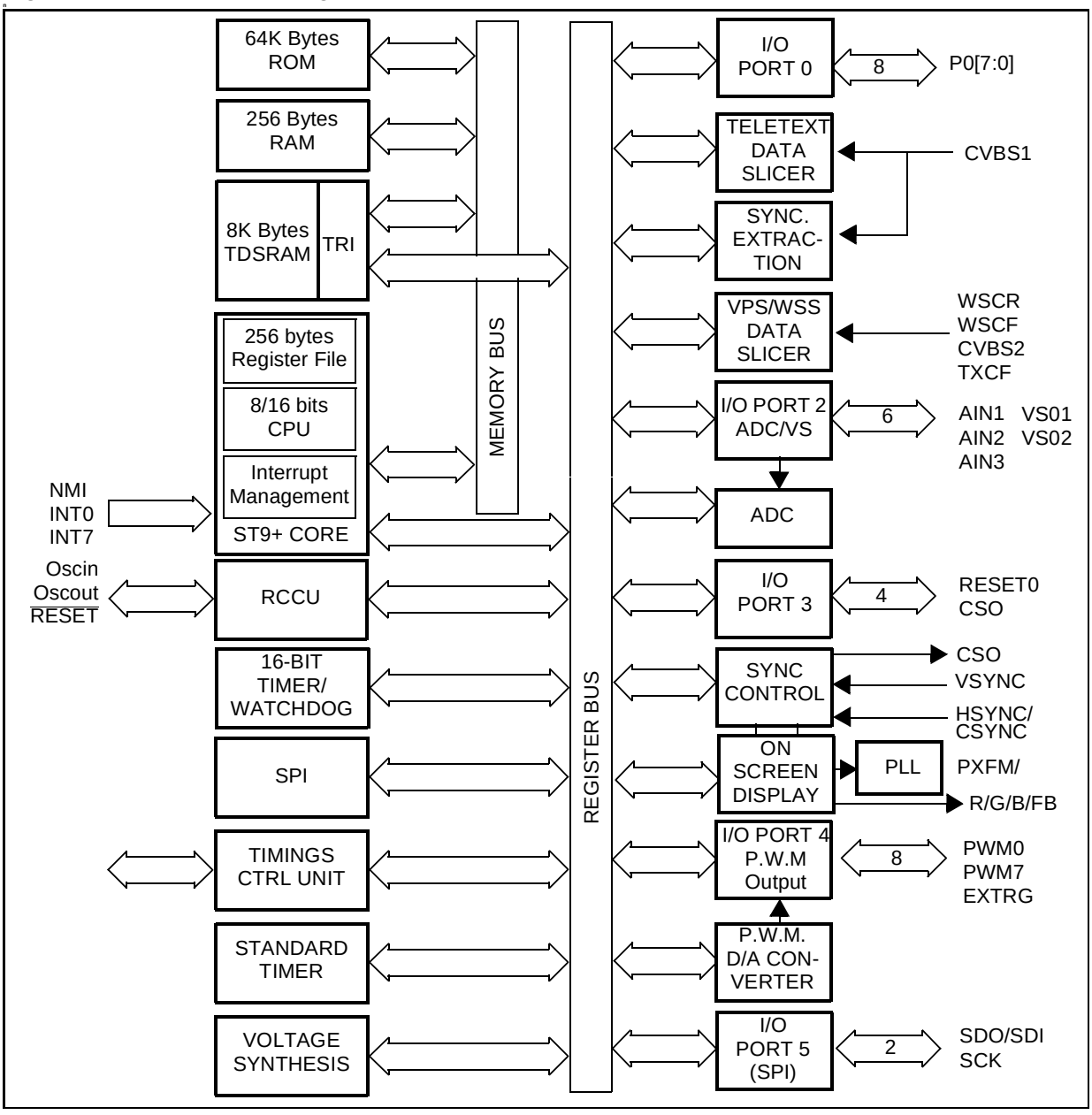
The nucleus of the ST92195 is the advanced Core which includes the Central Processing Unit (CPU), the ALU, the Register File and the interrupt controller. The Core has independent memory and register buses to add to the efficiency of the code.

A set of on-chip peripherals form a complete system for TV set and VCR applications:

– Voltage Synthesis
– VPS/WSS Slicer
– Teletext Slicer
– Teletext Display RAM
– OSD

Additional peripherals include a watchdog timer , a serial peripheral interface (SPI), a 16-bit timer and an A/D converter.

Figure 1. ST92195 Block Diagram



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