M68HC11 M Series

## *Technical Summary*
8-Bit Microcontroller

M68HC11 M-series high-performance microcontroller units (MCU) are enhanced members of the M68HC11 family of microcontrollers. The M series includes the MC68HC11M2 and MC68HC711M2. These devices incorporate highly sophisticated on-chip peripheral functions and, with a nonmultiplexed expanded bus, are characterized by high speed and low power consumption. Their fully static design allows these devices to operate at frequencies from 4 MHz to dc.

This technical summary contains information concerning standard and custom-ROM devices. Standard devices are those with EPROM replacing ROM (MC68HC711M2). Standard devices in a non-windowed package are one-time-programmable (OTPROM). Custom-ROM devices have a ROM array that is programmed at the factory to customer specifications.

ROM/EPROM refers to ROM for ROM-based devices and refers to EPROM for EPROM-based devices. The diagrams for these devices are combined and differences are noted where necessary.

Features

WARNING
MC68HC711M2 EPROM cannot be programmed with a standard EPROM programmer. User of PROG mode described on pp. 14 and 15 can damage the device.

- M68HC11 CPU
- 32 Kbytes of ROM/EPROM
- 1,280 Bytes of On-Chip RAM, All Saved During Standby
- Power Saving STOP and WAIT Modes
- Nonmultiplexed Address/Data Bus
- Eight CPU Key Wakeup Interrupt Pins
- Four-Channel Direct Memory Access Controller (DMAC)
- Four Pulse-Width Modulation (PWM) Timer Channels (Two Available with Extended-Rate PWMs)
- On-Chip 16-Bit Math Coprocessor
- Eight-Channel 8-Bit Analog-to-Digital (A/D) Converter
- 16-Bit Timer System
  - Three Input Capture (IC) Channels
  - Four Output Compare (OC) Channels
  - One Additional Channel, Software Selectable as Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog
- Enhanced Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- Dual Enhanced Synchronous Serial Peripheral Interface (SPI) with Chip Select Function
- Eight Input/Output (I/O) Ports (62 Pins)
  - 54 Bidirectional Pins
  - 8 Input Only Pins
- Available in 80-Pin Windowed Ceramic Quad Flat Pack (EPROM), and 80-Pin Plastic Quad Flat Pack (ROM/OTPROM)
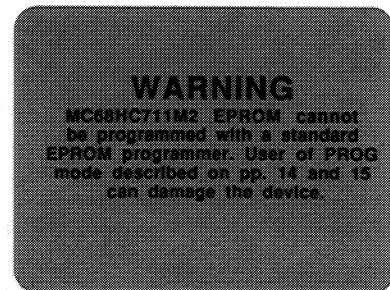
This document contains information on a new product. Specifications and information herein are subject to change without notice.

Standard Device Ordering Information

Package	Temperature	CONFIG	Description	Frequency	MC Order Number
80-Pin Ceramic Quad Flat Pack (Windowed)	– 40° to + 85° C	$02	EPROM	2 MHz	MC68HC711M2CFE2
				3 MHz	MC68HC711M2CFE3
				4 MHz	MC68HC711M2CFE4
	– 40° to + 105° C	$02	EPROM	2 MHz	MC68HC711M2VFE2
				3 MHz	MC68HC711M2VFE3
				4 MHz	MC68HC711M2VFE4
80-Pin Plastic Quad Flat Pack	– 40° to + 85° C	$02	OTPROM	2 MHz	MC68HC711M2CFU2
				3 MHz	MC68HC711M2CFU3
				4 MHz	MC68HC711M2CFU4
	– 40° to + 105° C	$02	OTPROM	2 MHz	MC68HC711M2VFU2
				3 MHz	MC68HC711M2VFU3
				4 MHz	MC68HC711M2VFU4
84-Pin Plastic Leaded Chip Carrier	– 40° to + 85° C	$02	OTPROM	2 MHz	MC68HC711M2CFN2
				3 MHz	MC68HC711M2CFN3
				4 MHz	MC68HC711M2CFN4
	– 40° to + 105° C	$02	OTPROM	2 MHz	MC68HC711M2VFN2
				3 MHz	MC68HC711M2VFN3
				4 MHz	MC68HC711M2VFN4
	– 40° to + 125° C	$02	OTPROM	2 MHz	MC68HC711M2MFN2
				3 MHz	MC68HC711M2MFN3
				4 MHz	MC68HC711M2MFN4

(Shaded areas indicate packages not available at this time)

Custom ROM Device Ordering Information

Package	Temperature	Description	Frequency	MC Order Number
80-Pin Plastic Quad Flat Pack	– 40° to + 85° C	Custom ROM	2 MHz	MC68HC11M2CFU2
			3 MHz	MC68HC11M2CFU3
			4 MHz	MC68HC11M2CFU4
	– 40° to + 105° C	Custom ROM	2 MHz	MC68HC11M2VFU2
			3 MHz	MC68HC11M2VFU3
			4 MHz	MC68HC11M2VFU4
84-Pin Plastic Leaded Chip Carrier	– 40° to + 85° C	Custom ROM	2 MHz	MC68HC11M2CFN2
			3 MHz	MC68HC11M2CFN3
			4 MHz	MC68HC11M2CFN4
	– 40° to + 105° C	Custom ROM	2 MHz	MC68HC11M2VFN2
			3 MHz	MC68HC11M2VFN3
			4 MHz	MC68HC11M2VFN4
	– 40° to + 125° C	Custom ROM	2 MHz	MC68HC11M2MFN2
			3 MHz	MC68HC11M2MFN3
			4 MHz	MC68HC11M2MFN4

(Shaded areas indicate packages not available at this time)

Table of Contents

Register Index

Register Index (Continued)

Left side pins (top to bottom):
MOSI1/PD3 — 1
SCK1/PD4 — 2
$\overline{SS1}$/PD5 — 3
PAI/PA7 — 4
OC2/PA6 — 5
OC3/PA5 — 6
OC4/PA4 — 7
I4/O5/PA3 — 8
IC1/PA2 — 9
IC2/PA1 — 10
IC3/PA0 — 11
V_{DD} — 12
V_{SS} — 13
ADDR15/PB7 — 14
ADDR14/PB6 — 15
ADDR13/PB5 — 16
ADDR12/PB4 — 17
ADDR11/PB3 — 18
ADDR10/PB2 — 19
ADDR9/PB1 — 20

Top pins (left to right, 80 to 61):
80 MISO1/PD2
79 TxD/PD1
78 RxD/PD0
77 MODA/$\overline{LIR}$
76 MODB/V_{STBY}
75 $\overline{RESET}$
74 XTAL
73 EXTAL
72 E
71 V_{DD}
70 V_{SS}
69 DATA7/PC7
68 DATA6/PC6
67 DATA5/PC5
66 DATA4/PC4
65 DATA3/PC3
64 DATA2/PC2
63 DATA1/PC1
62 DATA0/PC0
61 $\overline{IRQ}$

Right side pins (top to bottom):
60 — ADDR0/PF0
59 — ADDR1/PF1
58 — ADDR2/PF2
57 — ADDR3/PF3
56 — ADDR4/PF4
55 — ADDR5/PF5
54 — ADDR6/PF6
53 — ADDR7/PF7
52 — AV_{SS}
51 — V_{RH}
50 — V_{RL}
49 — PE0/AN0
48 — PE1/AN1
47 — PE2/AN2
46 — PE3/AN3
45 — PE4/AN4
44 — PE5/AN5
43 — PE6/AN6
42 — PE7/AN7
41 — AV_{DD}

Bottom pins (left to right, 21 to 40):
21 ADDR8/PB0
22 PW1/PH0
23 PW2/PH1
24 PW3/PH2
25 PW4/PH3
26 PH4
27 PH5
28 PH6
29 PH7
30 $\overline{XIRQ}$/V_{PPE} *
31 V_{DD}
32 V_{SS}
33 R/$\overline{W}$/PG7
34 PG6
35 $\overline{SS2}$/PG5
36 SCK2/PG4
37 MOSI2/PG3
38 MISO2/PG2
39 PG1
40 PG0

Center label: MC68HC(7)11M2

* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM.

(7)M2 80-PIN QFP

Pin Assignments for MC68HC11M2 80-Pin Plastic Quad Flat Pack and 80-Pin Windowed Ceramic Quad Flat Pack

MC68HC11M2 Block Diagram

32 KBYTES EPROM

1280 BYTES RAM

PULSE ACCUMULATOR

TIMER

PERIODIC INTERRUPT

COP WATCHDOG

PAI
OC2
OC1 { OC3
OC4
I4/O5
IC1
IC2
IC3

DDRA · PORT A

PA7/PAI
PA6/OC2
PA5/OC3
PA4/OC4
PA3/I4/O5
PA2/IC1
PA1/IC2
PA0/IC3

PORT E

PE7/AN7
PE6/AN6
PE5/AN5
PE4/AN4
PE3/AN3
PE2/AN2
PE1/AN1
PE0/AN0

A/D

AN7
AN6
AN5
AN4
AN3
AN2
AN1
AN0

V_{RH}
V_{RL}
AV_{DD}
AV_{SS}

$\overline{XIRQ}/V_{PPE}$[1]
$\overline{IRQ}$
$\overline{RESET}$

INTERRUPT LOGIC

MODA/$\overline{LIR}$
MODB/V_{STBY}

MODE CONTROL

XTAL
EXTAL

OSCILLATOR

E

CLOCK

V_{DD}
V_{SS}

SPI 1

$\overline{CS}/\overline{SS}$
SCK
SDO/MOSI
SDI/MISO

DDRD · PORT D

PD5/$\overline{SS}$
PD4/SCK
PD3/MOSI
PD2/MISO

SCI

TxD
RxD

PD1/TxD
PD0/RxD

CPU

$E\overline{R/W}$[2]

ER/W
R/W

SPI 2

$\overline{CS}/\overline{SS}$
SCK
SDO/MOSI
SDI/MISO

DDRG · PORT G

PG7/R/W
PG6
PG5/$\overline{SS}$
PG4/SCK
PG3/MOSI
PG2/MISO
PG1
PG0

DMA 1 2 3 4

DMHALT
BURST } 2
STEAL

MATH COPROCESSOR

DDRH KEY WAKEUP PORT H

PH7
PH6
PH5
PH4
PH3/PW4
PH2/PW3
PH1/PW2
PH0/PW1

PWM

PW4
PW3
PW2
PW1

ADDRESS/DATA BUS

ADDR15 ADDR14 ADDR13 ADDR12 ADDR11 ADDR10 ADDR9 ADDR8

ADDR7 ADDR6 ADDR5 ADDR4 ADDR3 ADDR2 ADDR1 ADDR0

DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0

DDRB · PORT B

ADDR15/PB7 ADDR14/PB6 ADDR13/PB5 ADDR12/PB4 ADDR11/PB3 ADDR10/PB2 ADDR9/PB1 ADDR8/PB0

DDRF · PORT F

ADDR7/PF7 ADDR6/PF6 ADDR5/PF5 ADDR4/PF4 ADDR3/PF3 ADDR2/PF2 ADDR1/PF1 ADDR0/PF0

DDRC · PORT C

DATA7/PC7 DATA6/PC6 DATA5/PC5 DATA4/PC4 DATA3/PC3 DATA2/PC2 DATA1/PC1 DATA0/PC0

NOTES:
1. V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM.
2. FOR EMULATION CHIP MODE. NOT AVAILABLE ON 80-PIN VERSION.

(7)M2 BLOCK

Operating Modes and On-Chip Memory

Operating Modes

In single-chip operating mode, the MC68HC11M2 is a stand-alone microcontroller with no external address or data bus.

In expanded operating mode, the MCU can access a 64-Kbyte physical address space. This space includes the same on-chip memory addresses used for single-chip mode, in addition to addressing capabilities for external peripheral and memory devices. The expansion bus is made up of ports B, C, and F, and the R/W signal. In expanded mode, high order address bits are output on the port B pins, low order address bits on the port F pins, and the data bus on port C. The R/W pin, which is output on port G bit 7, controls the direction of data transfer on the port C bus. The R/W signal reflects the state of the internal CPU R/W signal. Note that the timing of the R/W signal is the same as that for ports B and F address outputs except that the hold time from the falling edge of E is extended so that no special circuitry is required in an expanded system.

Special bootstrap mode allows special-purpose programs to be entered into internal RAM. The bootloader program uses the serial communications interface (SCI) to read a program of up to 1280 bytes into on-chip RAM. After a four-character delay, or after receiving the character for address $05FF, control passes to the loaded program at $0100.

Special test mode is used primarily for factory testing.

Mode Select Summary

Mode Selected	MODA	MODB
Bootstrap	0	0
Special Test	0	1
Single Chip	1	0
Expanded	1	1

Emulation chip mode, available only on 84-Pin versions of the MC68HC11M2, adds several capabilities. The DMA process can be temporarily suspended using the DMHALT pin. The DMHALT pin is an input-only pin with an internal pull-up resistor and is also used to switch to the emulation chip mode. If DMHALT is pulled low immediately after reset, the chip is put into emulation chip mode. The BURST pin indicates the bus cycle of the DMA when burst mode DMA is selected. The STEAL pin indicates the bus cycle of the DMA when steal mode DMA is selected. When in emulation chip mode, the ER/W pin acts the same as PG7/R/W and frees PG7 for general-purpose I/O.

On-Chip Memory

Bits in the INIT and CONFIG registers control the presence and location of the registers, RAM and ROM/EPROM in the physical 64-Kbyte memory space.

The 256-byte register block originates at $0000 after reset and can be remapped to any 4K boundary ($x000) after reset by writing an appropriate value to the INIT register.

The on-board 1,280 bytes of RAM are initially located immediately following the register block beginning at $0100 after reset. The RAM is divided into two sections of 256 bytes and 1024 bytes. If RAM and registers are both mapped to the same 4K boundary, the register block starts at $x000, and RAM starts at $x100. Otherwise, RAM starts at $x000. Remapping is accomplished by writing appropriate values to the INIT register. Refer to the register and RAM mapping examples that follow the MC68HC11M2 memory map.

The ROMON control bit in the CONFIG register controls the presence of ROM/EPROM in the memory map. In special test, bootstrap, and single-chip modes, ROMON = 1 out of reset and the ROM/EPROM is enabled and located at $8000–$FFFF. In expanded mode, ROMON = 0 out of reset and the ROM/EPROM is removed from the memory map. To use the ROM/EPROM in expanded mode, begin in single-chip mode, then change to expanded mode by setting the MDA bit in HPRIO register.
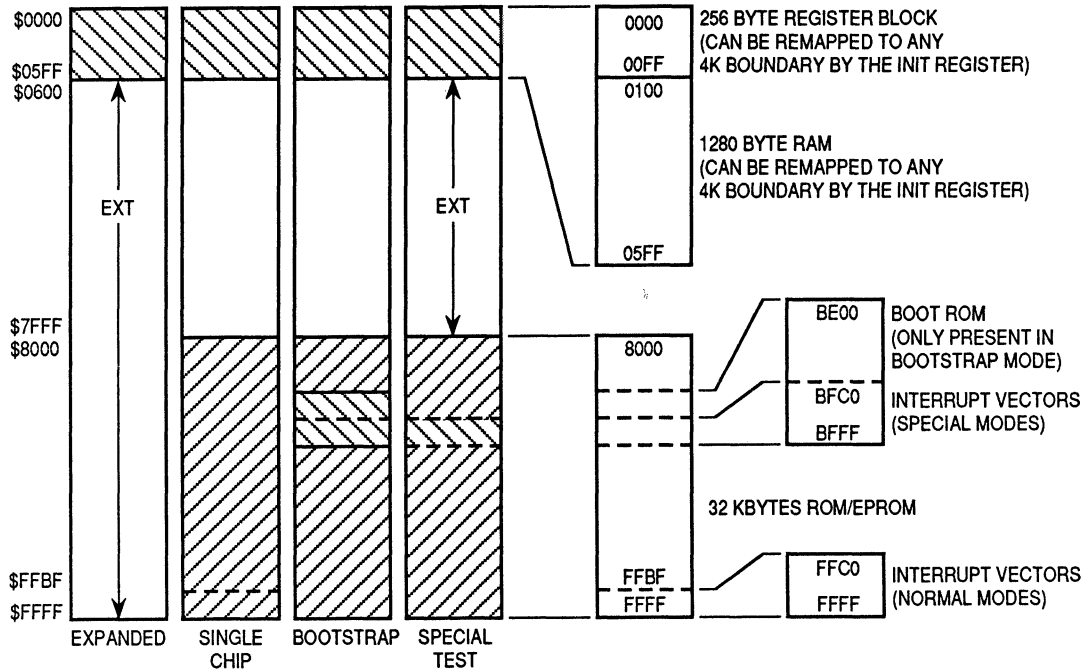
NOTE: ROM/EPROM CAN BE USED WITH EXPANDED BUS BY BEGINNING IN SINGLE-CHIP MODE AND SETTING MDA BIT IN HPRIO REGISTER.

(7)M2 MEM MAP

MC68HC11M2 Memory Map
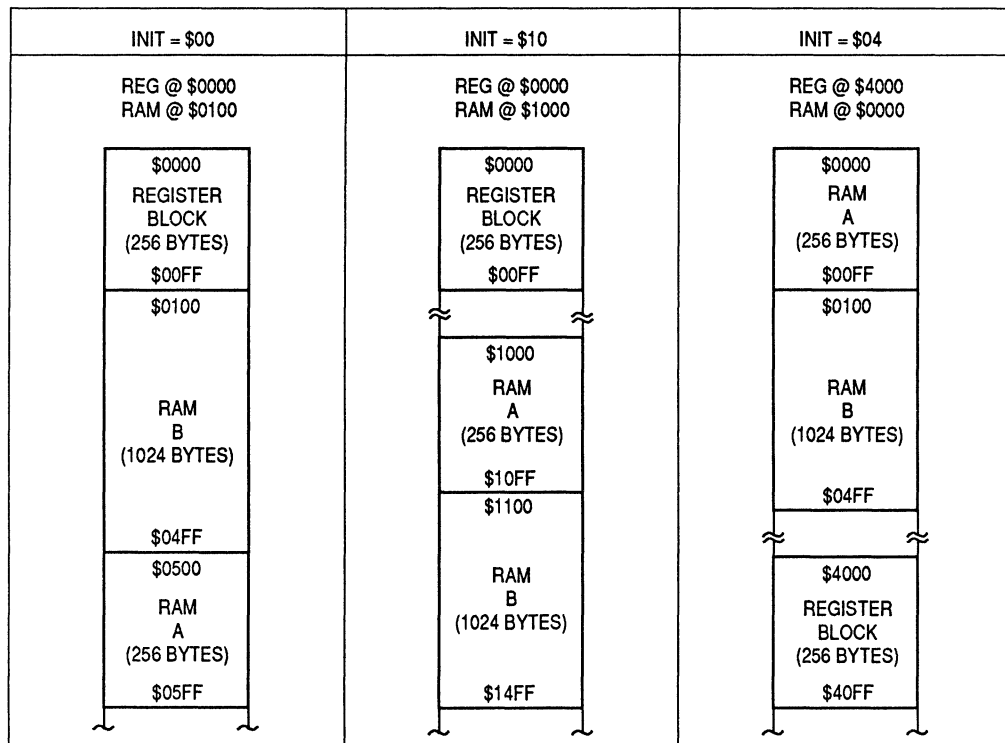
(7)M2
REGISTER
MAP

MC68HC11M2 RAM and Register Mapping

	Bit 7	6	5	4	3	2	1	Bit 0	
$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$0001	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
$0002	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
$0003	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	DDRF
$0004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$0005	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PORTF
$0006	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$0007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$0008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$0009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$000A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$000B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$000C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$000D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$000E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$000F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$0010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$0011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$0012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$0013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$0014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$0015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$0016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1(High)
$0017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$0018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$0019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$001A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$001B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$001C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$001D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$001E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (High)
$001F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (Low)
$0020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$0021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$0022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I	TMSK1
$0023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F	TFLG1
$0024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$0025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2

Address	Bit 7	6	5	4	3	2	1	Bit 0	Register
$0026	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0	PACTL
$0027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$0028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR1
$0029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR1
$002A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR1
$002B	MBE	0	ELAT	EXCOL	EXROW	0	0	EPGM	EPROG*
$002C	0	0	0	0	HPPUE	GPPUE	FPPUE	BPPUE	PPAR
$002D	—	—	—	—	—	—	—	—	Reserved
$002E	—	—	—	—	—	—	—	—	Reserved
$002F	—	—	—	—	—	—	—	—	Reserved
$0030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
$0031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$0032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$0033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$0034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$0035	—	—	—	—	—	—	—	—	Reserved
$0036	—	—	—	—	—	—	—	—	Reserved
$0037	—	—	—	—	—	—	—	—	Reserved
$0038	SPIM1	CWOM	LDSP1	IRVNE	LSBF1	SPR21	0	FCS1	OPT2
$0039	ADPU	CSEL	IRQE	DLY	CME	FCME	CR1	CR0	OPTION
$003A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$003B	—	—	—	—	—	—	—	—	Reserved
$003C	RBOOT	SMOD	MDA	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$003D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$003E	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	0	TEST1**
$003F	0	0	0	0	0	NOCOP	ROMON	0	CONFIG
$0040 to $005B	—	—	—	—	—	—	—	—	Reserved
$005C	Bit 7	6	5	4	3	2	1	0	PWDTY3
$005D	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY4
$005E	0	0	Bit 5	4	3	2	1	Bit 0	PWDT4R
$005F	—	—	—	—	—	—	—	—	Reserved
$0060	CON34	CON12	PCKA2	PCKA1	0	PCKB3	PCKB2	PCKB1	PWCLK
$0061	PCLK4	PCLK3	PCLK2	PCLK1	PPOL4	PPOL3	PPOL2	PPOL1	PWPOL
$0062	Bit 7	6	5	4	3	2	1	Bit 0	PWSCAL

* MC68HC711M2 only.
**For factory test only.

	Bit 7	6	5	4	3	2	1	Bit 0	
$0063	TPWSL	DISCP	CON4R	CON2R	PWEN4	PWEN3	PWEN2	PWEN1	PWEN
$0064	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT1
$0065	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT2
$0066	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT3
$0067	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT4
$0068	Bit 7	6	5	4	3	2	1	Bit 0	PWPER1
$0069	Bit 7	6	5	4	3	2	1	Bit 0	PWPER2
$006A	Bit 7	6	5	4	3	2	1	Bit 0	PWPER3
$006B	Bit 7	6	5	4	3	2	1	Bit 0	PWPER4
$006C	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY1
$006D	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY2
$006E	Bit 7	6	5	4	3	Bit 2	0	0	PWDT2R
$006F	—	—	—	—	—	—	—	—	Reserved
$0070	BTST	BSPL	0	SBR12	SBR11	SBR10	SBR9	SBR8	SCBDH
$0071	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SCBDL
$0072	LOOPS	WOMS	0	M	WAKE	ILT	PE	PT	SCCR1
$0073	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$0074	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SCSR1
$0075	0	0	0	0	0	0	0	RAF	SCSR2
$0076	R8	T8	0	0	0	0	0	0	SCDRH
$0077	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDRL
$0078	—	—	—	—	—	—	—	—	Reserved
$007B	—	—	—	—	—	—	—	—	Reserved
$007C	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	PORTH
$007D	DDH7	DDH6	DDH5	DDH4	DDH3	DDH2	DDH1	DDH0	DDRH
$007E	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	PORTG
$007F	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	DDRG
$0080 to $0087	—	—	—	—	—	—	—	—	Reserved
$0088	SPIE	SPE	GWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR2
$0089	SPIF	WCOL	0	MODF	0	0	0	0	SPSR2
$008A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR2
$008B	SPIM2	0	LDSP2	0	LSBF2	SPR22	0	FCS2	OPT4
$008C	—	—	—	—	—	—	—	—	Reserved

MC68HC11M2 Register and Control Bit Assignments (4 of 4)

	Bit 7	6	5	4	3	2	1	Bit 0	
$008D	KPOL7	KPOL6	KPOL5	KPOL4	KPOL3	KPOL2	KPOL1	KPOL0	KPOL
$008E	KWIF7	KWIF6	KWIF5	KWIF4	KWIF3	KWIF2	KWIF1	KWIF0	KWIF
$008F	KWIE7	KWIE6	KWIE5	KWIE4	KWIE3	KWIE2	KWIE2	KWIE1	KWIE
$0090	—	—	—	—	—	—	—	—	Reserved
to									
$00AF	—	—	—	—	—	—	—	—	Reserved
$00B0	DR1	DR0	TI2	TI1	TI0	FIT	TRS1	TRS0	DMAR
$00B1	DE4	DE3	DE2	DE1	DI4	DI3	DI2	DI1	DMAI
$00B2	DT4	DT3	DT2	DT1	DF4	DF3	DF2	DF1	DMAF
$00B3	STL	REP	RQ2	RQ1	RQ0	—	RS1	RS0	DMAC
$00B4	DSW	SW2	SW1	SW0	DDW	DW2	DW1	DW0	DMAW
$00B5	A15	A14	A13	A12	A11	A10	A9	A8	DMAS (High)
$00B6	A7	A6	A5	A4	A3	A2	A1	A0	DMAS (Low)
$00B7	A15	A14	A13	A12	A11	A10	A9	A8	DMAD (High)
$00B8	A7	A6	A5	A4	A3	A2	A1	A0	DMAD (Low)
$00B9	Bit 7	6	5	4	3	2	1	Bit 0	DMAT
$00BA	SPI1R	SPI1E	SPI2R	SPI2E	RTIOF	RTI	I4/O5I	ALU	DMATST*
$00BB	—	—	—	—	—	—	—	—	Reserved
to									
$00BF	—	—	—	—	—	—	—	—	Reserved
$00C0	Bit 31	30	29	28	27	26	25	Bit 24	CREG (High)
$00C1	Bit 23	22	21	20	19	18	17	Bit 16	CREG (High)
$00C2	Bit 15	14	13	12	11	10	9	Bit 8	CREG (Low)
$00C3	Bit 7	6	5	4	3	2	1	Bit 0	CREG (Low)
$00C4	SIG	DIV	MAC	DCC	TRG	OVE	DZE	ACE	ALUC
$00C5	Bit 15	14	13	12	11	10	9	Bit 8	AREG (High)
$00C6	Bit 7	6	5	4	3	2	1	Bit 0	AREG (Low)
$00C7	Bit 15	14	13	12	11	10	9	Bit 8	BREG (High)
$00C8	Bit 7	6	5	4	3	2	1	Bit 0	BREG (Low)
$00C9	NEG	RZF	0	0	0	OVF	DZF	ACF	ALUF
$00CA	—	—	—	—	—	—	—	—	Reserved
to									
$00CF	—	—	—	—	—	—	—	—	Reserved

*For factory test only.

Erasable Programmable Read-Only Memory

The MC68HC711M2 has 32 Kbytes of EPROM (OTPROM in a non-windowed package). The MC68HC11M2 has 32 Kbytes of mask-programmed ROM. ROM/EPROM can be mapped at $8000–$FFFF. In single-chip mode the ROM/EPROM is enabled, regardless of the value in the CONFIG register.

There are two methods used to program and verify EPROM. In PROG mode, the EPROM is programmed as a stand-alone EPROM by adapting the MCU footprint to the 27256-type EPROM and using an appropriate EPROM programmer. Refer to the Wiring Diagram for MC68HC711M2 EPROM in PROG Mode. In normal MCU mode, EPROM can be programmed in any operating mode — special test, bootstrap, expanded, or single chip. Normal programming is accomplished through the EPROG register.

Programming EPROM requires an external 12.25 volt nominal power supply (V_{PPE}).

To program the EPROM, complete the following steps using the EPROG register:

1. Write to EPROG with the ELAT bit set.
2. Write data to the desired address.
3. Write to EPROG with the ELAT and EPGM bits set.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EPGM bit in EPROG to turn off the V_{PPE} voltage.
6. Clear the EPROG register to reconfigure the EPROM address and data buses for normal operation.

CAUTION

PROG mode is initiated when $\overline{RESET}$, $\overline{MODA}$, and $\overline{MODB}$ pins are pulled low (the pin state required to enter bootstrap mode). This means that if these three pins are pulled low and V_{PPE} is present on the $\overline{XIRQ}$ pin, the EPROM can be programmed. To prevent this, place a pull-up resistor on the $\overline{IRQ}$ pin which is the chip select in PROG mode. When the device goes into reset, the EPGM bit is forced to the voltage disable state (EPGM = 0) before the address/data latches are enabled to the external input lines. Only after this occurs is voltage control returned to the $\overline{IRQ}$ pin.

Wiring Diagram for MC68HC711M2 EPROM in PROG Mode

EPROM MODE PIN CONNECTIONS
MCU PIN FUNCTIONS
EPROM PIN FUNCTIONS

Left side (MC68HC711M2, INTERNAL 32 KBYTE EPROM, 27256 FOOTPRINT):

EPROM MODE	MCU PIN FUNCTIONS	EPROM PIN FUNCTIONS
ADDR0	PF0/ADDR0	ADDR0
ADDR1	PF1/ADDR1	ADDR1
ADDR2	PF2/ADDR2	ADDR2
ADDR3	PF3/ADDR3	ADDR3
ADDR4	PF4/ADDR4	ADDR4
ADDR5	PF5/ADDR5	ADDR5
ADDR6	PF6/ADDR6	ADDR6
ADDR7	PF7/ADDR7	ADDR7
ADDR8	PB0/ADDR8	ADDR8
ADDR9	PB1/ADDR9	ADDR9
ADDR10	PB2/ADDR10	ADDR10
ADDR11	PB3/ADDR11	ADDR11
ADDR12	PB4/ADDR12	ADDR12
ADDR13	PB5/ADDR13	ADDR13
ADDR14	PB6/ADDR14	ADDR14

Right side:

EPROM PIN FUNCTIONS	MCU PIN FUNCTIONS	EPROM MODE
O0	PC0/DATA0	O0
O1	PC1/DATA1	O1
O2	PC2/DATA2	O2
O3	PC3/DATA3	O3
O4	PC4/DATA4	O4
O5	PC5/DATA5	O5
O6	PC6/DATA6	O6
O7	PC7/DATA7	O7
$\overline{OE}$	PB7/ADDR15	$\overline{OE}$
$\overline{CE}$	$\overline{IRQ}$	$\overline{CE}$
V_{PP}	XIRQ/V_{PPE}	V_{PP}
V_{CC}	V_{DD}	V_{CC}
V_{SS}	V_{SS}	V_{SS}

NOTE 4:
GND	PA0/IC3
GND	PA1/IC2
GND	PA2/IC1

NOTE 1:
GND	PA3/IC4/OC5/OC1
GND	PA4/OC4/OC1
GND	PA5/OC3/OC1
GND	PA6/OC2/OC1
GND	PA7/PAI/OC1
GND	PG0
GND	PG1
GND	PG2/SDI/MISO
GND	PG3/SDO/MOSI
GND	PG4/SCK
GND	PG5/$\overline{SS}$
GND	PG6
GND	PG7/R$\overline{W}$
GND	PD0/RxD
GND	PD1/TxD
GND	PD2/SDI/MISO
GND	PD3/SDO/MOSI
GND	PD4/SCK
GND	PD5/$\overline{SS}$

MC68HC711M2

UNUSED INPUTS NOTE 2:
PE0/AN0
PE1/AN1
PE2/AN2
PE3/AN3
PE4/AN4
PE5/AN5
PE6/AN6
PE7/AN7

NOTE 1:
PH0/PW1	GND
PH1/PW2	GND
PH2/PW3	GND
PH3/PW4	GND
PH4	GND
PH5	GND
PH6	GND
PH7	GND
V_{RL}	GND
V_{RH}	GND
EXTAL	GND

UNUSED OUTPUTS NOTE 3:
XTAL
XOUT
E
TESTxx (3)

NOTE 4:
MODA/$\overline{LIR}$	GND
MODB/V_{STBY}	GND
$\overline{RESET}$	GND

NOTES:
1. UNUSED INPUTS — GROUNDING IS RECOMMENDED.
2. UNUSED INPUTS — THESE PINS MAY BE LEFT UNTERMINATED.
3. UNUSED OUTPUTS — THESE PINS SHOULD BE LEFT UNCONNECTED.
4. GROUNDING THESE SIX PINS CONFIGURES THE MC68HC711M2 FOR EPROM EMULATION MODE.

7M2 EPROM PC

Wiring Diagram for MC68HC711M2 EPROM in PROG Mode

Bit 7	6	5	4	3	2	1	Bit 0
MBE	—	ELAT	EXCOL	EXROW	—	—	EPGM

RESET: 0   0   0   0   0   0   0   0

MBE — Multiple Byte Program Enable
    0 = Normal programming
    1 = Program two bytes with same data. This command allows EPROM to be programmed whether the value of ELAT is one or zero.

Bit 6 — Not implemented
    Always reads zero

ELAT — EPROM Latch Control
    0 = ROM/EPROM address and data bus configured for normal reads
    1 = ROM/EPROM address and data bus configured for programming

EXCOL — Select Extra Columns
    0 = User array selected
    1 = Extra columns selected and user array disabled

EXROW — Select Extra Row
    0 = User array selected
    1 = Extra rows selected and user array disabled

Bits [2:1] — Not implemented
    Always read zero

EPGM — EPROM Program Command
    0 = Program or erase voltage to EPROM array off
    1 = Program or erase voltage to EPROM array on

CONFIG — COP, ROM/EPROM Enable   **$003F**

Bit 7	6	5	4	3	2	1	Bit 0
—	—	—	—	—	NOCOP	ROMON	—

RESET: 0   0   0   0   0   1   0   0

These bits can be read at any time. The value read is the one latched into the register from the last reset sequence.

Bits [7:3] — Not implemented
    Always read zero

NOCOP — COP System Disable
    Refer to **Resets and Interrupts**.

ROMON — ROM/EPROM Enable

If SMOD = 1, this bit can be written at any time. If SMOD = 0, this bit **cannot** be written. In single-chip mode ROMON is forced to one out of reset. In special test, boot, and normal expanded modes, ROMON is forced to zero out of reset.

0 = 32 Kbytes of ROM/EPROM removed from the memory map
1 = 32 Kbytes of ROM/EPROM present in the memory map

Bit 0 — Not implemented
Always reads zero

OPT2 — System Configuration Options 2 $0038

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIM1	CWOM	LDSP1	IRVNE	LSBF1	SPR21	—	FCS1
RESET:	0	0	0	—	0	0	0	0

SPIM1 — SPI Mode Select
0 = SPI 1 configured for normal operation
1 = MOSI, MISO, and SS pins configured as serial data out (SDO), serial data in (SDI), and chip select (CS) pins. MODF flag in SPSR1 has no meaning.

CWOM — Port C Wired-OR Mode
Refer to **Parallel Input/Output**.

LDSP1 — Link DMA and SPI 1
Refer to **Serial Peripheral Interface**.

IRVNE — Internal Read Visibility/Not E
In expanded modes, IRVNE determines whether IRV is on or off. In special test mode, IRVNE is reset to one. In all other modes, IRVNE is reset to zero.
0 = No internal read visibility on external bus
1 = Data from internal reads is driven out of the external data bus.
In single-chip modes, this bit determines whether the E clock drives out from the chip.
0 = E is driven out from the chip.
1 = E pin is driven low.

Mode	IRVNE Out of Reset	E Clock Out of Reset	IRV Out of Reset	IRVNE Affects Only	IRVNE Can Be Written
Single Chip	0	On	Off	E	Once
Expanded	0	On	Off	IRV	Once
Bootstrap	0	On	Off	E	Any Time
Special Test	1	On	On	IRV	Any Time

LSBF1 — SPI LSB First Enable
Refer to **Serial Peripheral Interface**.

SPR21 — SPI 1 Clock Rate Select
Refer to **Serial Peripheral Interface**.

Bit 1 — Not implemented
Always reads zero

FCS1 — Force $\overline{CS}$ for SPI 1
   Refer to **Serial Peripheral Interface**.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous   **$003C**

Bit 7	6	5	4	3	2	1	Bit 0	
RBOOT*	SMOD*	MDA*	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0	
RESET: 0	0	0	0	0	1	1	0	Single Chip
0	0	0	0	0	1	1	0	Expanded
1	1	0	0	0	1	1	0	Bootstrap
0	1	1	0	0	1	1	0	Special Test

*The value of RBOOT, SMOD, and MDA at reset depends on the mode selected at power up.

RBOOT — Read Bootstrap ROM
   Valid only when SMOD is set to one (special bootstrap or special test mode). Can only be written in special modes.
   0 = Bootloader ROM disabled and not in map
   1 = Bootloader ROM enabled and in map at $BE00–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A
   These two bits can be read at any time. SMOD can only be written to zero. MDA can only be written once in normal modes or any time in special modes.

Inputs			Latched at Reset	
MODB	MODA	Mode	SMOD	MDA
1	0	Single Chip	0	0
1	1	Expanded	0	1
0	0	Bootstrap	1	0
0	1	Special Test	1	1

PSEL[4:0] — Priority Select Bits [4:0]
   Refer to **Resets and Interrupts**.

INIT — RAM and I/O Mapping   **$003D**

Bit 7	6	5	4	3	2	1	Bit 0
RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
RESET: 0	0	0	0	0	0	0	0

   Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes.

RAM[3:0] — Internal RAM Map Position
   Specifies upper four bits of RAM address. At reset, RAM is mapped to $0000 along with register block.

REG[3:0] — 256-Byte Register Block Map Position
   Specifies upper four bits of register space address. At reset, registers are mapped to $0000.

Parallel Input/Output

The MC68HC11M2 has up to 62 input/output lines, depending on the operating mode. To improve the I/O functions, the data bus of this microcontroller is expanded and not multiplexed. The following table is a summary of the configuration and features of each port.

Port	Input Pins	Output Pins	Bidirectional Pins	Shared Functions
Port A	—	—	8	Timer
Port B	—	—	8	High Order Address/General I/O
Port C	—	—	8	Data Bus/General I/O
Port D	—	—	6	SCI and SPI 1
Port E	8	—	—	A/D Converter
Port F	—	—	8	Low Order Address/General I/O
Port G	—	—	8	SPI 2
Port H	—	—	8	PWM/Key Wakeup/General I/O

NOTE

Do not confuse pin function with the electrical state of the pin at reset. All general-purpose I/O pins configured as inputs at reset are in a high-impedance state and the contents of port data registers is undefined. In port descriptions, a "U" indicates this condition. The pin function is mode dependent.

PORTA — Port A Data $0000

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	U	U	U	U	U	U	U	U
Alt. Pin Func.:	PAI	OC2	OC3	OC4	IC4/OC5	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

DDRA — Data Direction Register for Port A $0001

	Bit 7	6	5	4	3	2	1	Bit 0
	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
RESET:	0	0	0	0	0	0	0	0

DDA[7:0] — Data Direction for Port A
   0 = Bits set to zero to configure corresponding I/O pin for input only
   1 = Bits set to one to configure corresponding I/O pin for output

PORTB — Port B Data $0004

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	U	U	U	U	U	U	U	U
Expan. or Test:	ADDR15	ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8

Reset state is mode dependent. In single-chip or bootstrap modes, port B pins are high-impedance inputs with selectable internal pull-up resistors. In expanded or test modes, port B pins are high order address outputs and PORTB is not in the memory map.

DDRB — Data Direction Register for Port B $0002

	Bit 7	6	5	4	3	2	1	Bit 0
	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
RESET:	0	0	0	0	0	0	0	0

DDB[7:0] — Data Direction for Port B
    0 = Bits set to zero to configure corresponding I/O pin for input only
    1 = Bits set to one to configure corresponding I/O pin for output

PORTC — Port C Data $0006

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	U	U	U	U	U	U	U	U
Expan. or Test:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Reset state is mode dependent. In single-chip or bootstrap modes, port C pins are high-impedance inputs. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. In expanded or test modes, port C pins are data bus inputs and outputs and PORTC is not in the memory map.

DDRC — Data Direction Register for Port C $0007

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction for Port C
    0 = Bits set to zero to configure corresponding I/O pin for input only
    1 = Bits set to one to configure corresponding I/O pin for output

---

PORTD — Port D Data $0008

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	—	—	U	U	U	U	U	U
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	SDO/ MOSI	SDI/ MISO	TxD	RxD

In all modes, port D bits [5:0] can be used either for general-purpose I/O, or with the SCI and SPI 1 subsystems. During reset, port D pins PD[5:0] are configured as high impedance inputs (DDRD bits cleared).

DDRD — Data Direction Register for Port D $0009

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

Bits [7:6] — Not implemented
    Always read zero

DDD[5:0] — Data Direction for Port D
    0 = Bits set to zero to configure corresponding I/O pin for input only
    1 = Bits set to one to configure corresponding I/O pin for output

PORTE — Port E Data $000A

	Bit 7	6	5	4	3	2	1	Bit 0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	U	U	U	U	U	U	U	U
Alt. Pin Func.:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Port E has eight general-purpose input pins and shares functions with the A/D converter system. When some port E pins are being used for general-purpose input and others are being used as A/D inputs, PORTE should not be read during the sample portion of an A/D conversion.

PORTF — Port F Data $0005

	Bit 7	6	5	4	3	2	1	Bit 0
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
S. Chip or Boot:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
RESET:	U	U	U	U	U	U	U	U
Expan. or Test:	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

Reset state is mode dependent. In single-chip or bootstrap modes, port F is high-impedance input with selectable internal pull-up resistors. In expanded or test modes, port F pins are low order address outputs and PORTF is not in the memory map.

DDRF — Data Direction Register for Port F $0003

	Bit 7	6	5	4	3	2	1	Bit 0
	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0
RESET:	0	0	0	0	0	0	0	0

DDF[7:0] — Data Direction for Port F
    0 = Bits set to zero to configure corresponding I/O pin for input only
    1 = Bits set to one to configure corresponding I/O pin for output

PORTG — Port G Data $007E

Bit 7	6	5	4	3	2	1	Bit 0
PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0

RESET: U U U U U U U U

Alt. Pin
Func.: R/W̄ — S̄S̄ SCK SDO/MOSI SDI/MISO — —

PG7 is available only in single-chip mode because it is the R/W̄ pin in expanded and test modes. PG6 is available in all modes. In all modes, port G bits [5:2] can be used either for general-purpose I/O, or with the SPI 2 subsystem. PG[1:0] are available in all modes. During reset, port G pins are configured as high impedance inputs (DDRG bits cleared) with selectable internal pull-up resistors.

DDRG — Data Direction Register for Port G $007F

Bit 7	6	5	4	3	2	1	Bit 0
DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0

RESET: 0 0 0 0 0 0 0 0

DDG[7:0] — Data Direction for Port G
0 = Bits set to zero to configure corresponding I/O pin for input only
1 = Bits set to one to configure corresponding I/O pin for output

NOTE

When SPE bit in SPCR2 register is set (SPI 2 enabled), bits [5:2] are dedicated to the SPI 2 subsystem. However, port G bit 5 still responds to DDG5. If DDG5 is set port G bit 5 is given up by SPI 2.

PORTH — Port H Data $007C

Bit 7	6	5	4	3	2	1	Bit 0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0

RESET: U U U U U U U U

Alt. Pin
Func.: KWI7 KWI6 KWI5 KWI4 KWI3/PW4 KWI2/PW3 KWI1/PW2 KWI0/PW1

PH[7:0] are available for the key wakeup function in any mode since KWI is an input-only function and does not affect the operation of general-purpose I/O or the PWM outputs. PH[3:0] are available for the PWM function in any mode provided those pins are not used for general-purpose I/O. In all modes, port H bits [7:0] can be used for general-purpose I/O when not in use by the KWI or the PWM. During reset, port H pins are configured as high impedance inputs (DDRH bits cleared) with selectable internal pull-up resistors.

DDRH — Data Direction Register for Port H $007D

Bit 7	6	5	4	3	2	1	Bit 0
DDH7	DDH6	DDH5	DDH4	DDH3	DDH2	DDH1	DDH0
RESET: 0	0	0	0	0	0	0	0

DDH[7:0] — Data Direction for Port H
    0 = Bits set to zero to configure corresponding I/O pin for input only
    1 = Bits set to one to configure corresponding I/O pin for output

NOTE

PWM circuitry forces the I/O state to be an output for each port H line associated with an enabled pulse-width modulator in any mode. In this case, data direction bits are not changed and have no effect on these lines. DDRH reverts to controlling the I/O state of a pin when the associated function is disabled.

PPAR — Port Pull-Up Assignment $002C

Bit 7	6	5	4	3	2	1	Bit 0
—	—	—	—	HPPUE	GPPUE	FPPUE	BPPUE
RESET: 0	0	0	0	1	1	1	1

Bits [7:4] — Not implemented
    Always read zero

xPPUE — Port x Pin Pull-Up Enable
    0 = Port x pin on-chip pull-up devices disabled
    1 = Port x pin on-chip pull-up devices enabled

NOTE

FPPUE and BPPUE do not apply in expanded modes because port F and B are address outputs.

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIM1	CWOM	LDSP1	IRVNE	LSBF1	SPR21	—	FCS1
RESET:	0	0	0	—	0	0	0	0

SPIM1 — SPI Mode Select
    Refer to **Serial Peripheral Interface**.

CWOM — Port C Wired-OR Mode
        0 = Port C operates normally.
        1 = Port C outputs are open-drain.

LDSP1 — Link DMA and SPI 1
    Refer to **Serial Peripheral Interface**.

IRVNE — Internal Read Visibility/Not E
    Refer to **Operating Modes and On-Chip Memory**.

LSBF1 — SPI LSB First Enable
    Refer to **Serial Peripheral Interface**.

SPR21 — SPI Clock (SCK) Rate Select
    Refer to **Serial Peripheral Interface**.

Bit 1 — Not implemented
    Always reads zero

FCS1 — Force $\overline{\text{CS}}$ for SPI 1
    Refer to **Serial Peripheral Interface**.

Resets and Interrupts

The MC68HC11M2 has 3 reset vectors and 18 interrupt vectors. The reset vectors are as follows:

- $\overline{RESET}$, or Power-On Reset
- Clock Monitor Fail
- COP Failure

The 18 interrupt vectors service 22 interrupt sources (3 nonmaskable, 19 maskable). The three nonmaskable interrupt vectors are as follows:

- $\overline{XIRQ}$ Pin (X-Bit Interrupt)
- Illegal Opcode Trap
- Software Interrupt

On-chip peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the condition code register (CCR) is clear. Maskable interrupts are prioritized according to a default arrangement; however, any one source can be elevated to the highest maskable priority position by a software-accessible control register, HPRIO. The HPRIO register can be written at any time, provided the I bit in the CCR is set.

Nineteen interrupt sources in the MC68HC11M2 are subject to masking by a global interrupt mask bit (I bit in the CCR). In addition to the global I bit, all of these sources, except the external interrupt ($\overline{IRQ}$) pin, are controlled by local enable bits in control registers. Most interrupt sources in the M68HC11 have separate interrupt vectors; therefore, there is usually no need for software to poll control registers to determine the cause of an interrupt.

For some interrupt sources, such as the SCI interrupts, the flags are automatically cleared during the normal course of responding to the interrupt requests. For example, the RDRF flag in the SCI system is cleared by the automatic clearing mechanism consisting of a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request would be to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

Refer to the following table for a list of interrupt and reset vector assignments

Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CCR Mask Bit	Local Mask	Priority (1=High)
FFC0, C1– FFCE,CF	Reserved	—	—	—
FFD0, D1	DMA Terminal Count	I	DI[4:1]	18
FFD2, D3	ALU Complete	I	ACE, DZE	16
FFD4, D5	KWI Key Wakeup	I	KWIE[7:1]	15
FFD6, D7	SCI Serial System	I		
	• SCI Receive Data Register Full		RIE	
	• SCI Receiver Overrun		RIE	22
	• SCI Transmit Data Register Empty		TIE	
	• SCI Transmit Complete		TCIE	
	• SCI Idle Line Detect		ILIE	
FFD8, D9	SPI Serial Transfer Complete	I	SPIE	21
FFDA, DB	Pulse Accumulator Input Edge	I	PAII	20
FFDC, DD	Pulse Accumulator Overflow	I	PAOVI	19
FFDE, DF	Timer Overflow	I	TOI	17
FFE0, E1	Timer Input Capture 4/Output Compare 5	I	I4/O5I	14
FFE2, E3	Timer Output Compare 4	I	OC4I	13
FFE4, E5	Timer Output Compare 3	I	OC3I	12
FFE6, E7	Timer Output Compare 2	I	OC2I	11
FFE8, E9	Timer Output Compare 1	I	OC1I	10
FFEA, EB	Timer Input Capture 3	I	IC3	9
FFEC, ED	Timer Input Capture 2	I	IC2I	8
FFEE, EF	Timer Input Capture 1	I	IC1I	7
FFF0, F1	Real Time Interrupt	I	RTII	6
FFF2, F3	IRQ (External Pin)	I	None	5
FFF4, F5	XIRQ Pin	X	None	4
FFF6, F7	Software Interrupt	None	None	*
FFF8, F9	Illegal Opcode Trap	None	None	*
FFFA, FB	COP Failure	None	NOCOP	3
FFFC, FD	Clock Monitor Fail	None	FCME/CME	2
FFFE, FF	RESET	None	None	1

* Same level as an instruction

MC68HC11M2TS/D

MOTOROLA
27

Bit 7	6	5	4	3	2	1	Bit 0
ADPU	CSEL	IRQE*	DLY*	CME	FCME*	CR1*	CR0*

RESET: 0   0   0   1   0   0   0   0

*Can be written only once in first 64 cycles out of reset in normal mode, or at any time in special modes.

ADPU — Analog-to-Digital Converter Power Up
Refer to **Analog-to-Digital Converter**.

CSEL — Clock Select
Refer to **Analog-to-Digital Converter**.

IRQE — $\overline{\text{IRQ}}$ Select Edge Sensitive Only
0 = Low level recognition
1 = Falling edge recognition

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
0 = No stabilization delay on exit from STOP
1 = Stabilization delay enabled on exit from STOP

CME — Clock Monitor Enable
0 = Clock monitor disabled; slow clocks can be used
1 = Slow or stopped clocks cause clock failure reset

FCME — Force Clock Monitor Enable
0 = Clock monitor follows the state of the CME bit
1 = Clock monitor circuit is enabled until next reset

CR[1:0] — COP Timer Rate Select

COP Timer Rate Select

CR[1:0]	Divide $E/2^{15}$ By	XTAL = 8.0 MHz Timeout −0/+16.4 ms	XTAL = 12.0 MHz Timeout −0/+10.9 ms	XTAL = 16.0 MHz Timeout −0/+8.2 ms
0 0	1	16.384 ms	10.923 ms	8.192 ms
0 1	4	65.536 ms	43.691 ms	32.768 ms
1 0	16	262.14 ms	174.76 ms	131.07 ms
1 1	64	1.049 sec	699.05 ms	524.29 ms
	E =	2.0 MHz	3.0 MHz	4.0 MHz

COPRST — Arm/Reset COP Timer Circuitry $003A

Bit 7	6	5	4	3	2	1	Bit 0
7	6	5	4	3	2	1	0

RESET: 0   0   0   0   0   0   0   0

Write $55 to COPRST to arm COP watchdog clearing mechanism. Write $AA to COPRST to reset COP watchdog.

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT*	SMOD*	MDA*	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	0	0	1	1	0

*RBOOT, SMOD, and MDA reset depend on power-up initialization mode and can only be written in special modes.

RBOOT — Read Bootstrap ROM
Refer to **Operating Modes and On-Chip Memory**.

SMOD — Special Mode Select
Refer to **Operating Modes and On-Chip Memory**.

MDA — Mode Select A
Refer to **Operating Modes and On-Chip Memory**.

PSEL[4:0] — Priority Select Bits [4:0]
Can be written only while bit I in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources.

PSELx					Interrupt Source Promoted
4	3	2	1	0	
0	0	0	X	X	Reserved (Default to IRQ)
0	0	1	0	0	Reserved (Default to IRQ)
0	0	1	0	1	Reserved (Default to IRQ)
0	0	1	1	0	IRQ (External Pin)
0	0	1	1	1	Real-Time Interrupt
0	1	0	0	0	Timer Input Capture 1
0	1	0	0	1	Timer Input Capture 2
0	1	0	1	0	Timer Input Capture 3
0	1	0	1	1	Timer Output Compare 1
0	1	1	0	0	Timer Output Compare 2
0	1	1	0	1	Timer Output Compare 3
0	1	1	1	0	Timer Output Compare 4
0	1	1	1	1	Timer Output Compare 5/Input Capture 4
1	0	0	0	0	Timer Overflow
1	0	0	0	1	Pulse Accumulator Overflow
1	0	0	1	0	Pulse Accumulator Input Edge
1	0	0	1	1	SPI Serial Transfer Complete
1	0	1	0	0	SCI Serial System
1	0	1	0	1	Key Wakeup
1	0	1	1	0	ALU Complete
1	0	1	1	1	DMA Terminal Count
1	1	X	X	X	Reserved (Default to IRQ)

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	—	—	—	NOCOP	ROMON	—
RESET:	0	0	0	0	0	1	0	0

Bits [7:3] — Not implemented
  Always read zero

NOCOP — COP System Disable
  Resets to programmed value
    0 = COP enabled (forces reset on timeout)
    1 = COP disabled (does not force reset on timeout)

ROMON — ROM/EPROM Enable
  Refer to **Operating Modes and On-Chip Memory**.

Bit 1 — Not implemented
  Always reads zero

Key Wakeup Interrupt

There are eight key wakeup interrupt (KWI) input pins that are shared with the port H and PWM functions. Because KWI is an input only function, its use does not affect the functions of the general-purpose I/O and PWM outputs. Refer to the following block diagram.
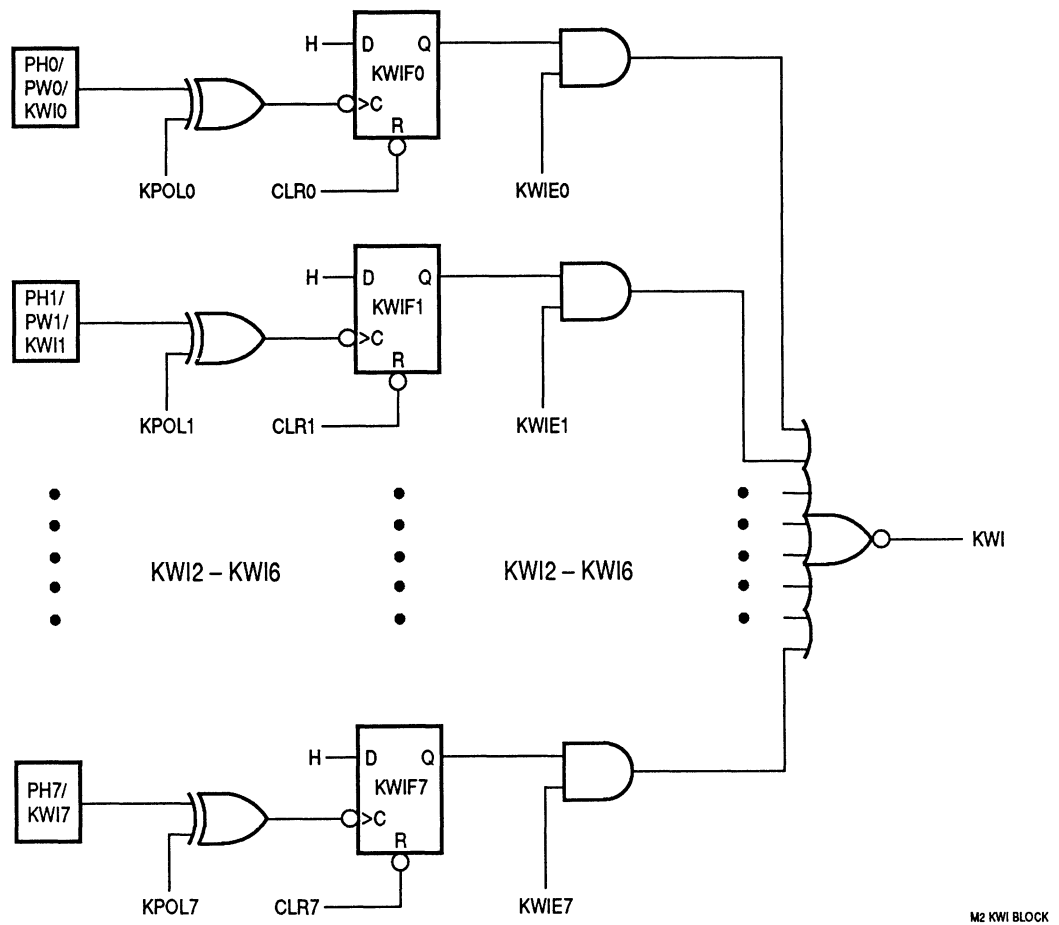
Key Wakeup Interrupt Block Diagram

When the active edge, as defined by bit x of the KPOL register, is detected on the pin, the KWIF bit x is set. The active edge may generate an interrupt request to the CPU if the corresponding KWIEx bit and the I bit are not masked. Key interrupts share the same interrupt vector address.

KPOL — Key Wakeup Polarity $008D

Bit 7	6	5	4	3	2	1	Bit 0
KPOL7	KPOL6	KPOL5	KPOL4	KPOL3	KPOL2	KPOL1	KPOL0

RESET: 0   0   0   0   0   0   0   0

KPOL[7:0] — Key Polarity Select
    0 = Falling edge on KWI pin sets KWIFx in the KWIF register
    1 = Rising edge on the KWIx pin sets KWIFx in the KWIF register

---

KWIF — KWI Input Flag Register $008E

Bit 7	6	5	4	3	2	1	Bit 0
KWIF7	KWIF6	KWIF5	KWIF4	KWIF3	KWIF2	KWIF1	KWIF0

RESET: 0   0   0   0   0   0   0   0

KWIF[7:0] — Key Wakeup Input Flag
    To erase illegal input flag, initialize this register after initializing the KPOL register. Refer to KPOL
    register.

KWIE — KWI Interrupt Enable $008F

Bit 7	6	5	4	3	2	1	Bit 0
KWIE7	KWIE6	KWIE5	KWIE4	KWIE3	KWIE2	KWIE1	KWIE0

RESET: 0   0   0   0   0   0   0   0

KWIE[7:0] — Key Wakeup Interrupt Enable
    An interrupt is generated when the KWIFx bit in the KWIF register and the corresponding KWIEx bit
    are set. KWIE[7:0] share the same interrupt vector and can wake the CPU when it is in STOP mode.

Main Timer

The design of the main timer is based on a free-running 16-bit counter with a four-stage programmable prescaler. A timer overflow function allows software to extend the system's timing capability beyond the counter's 16-bit range.

The timer has three input capture channels, four output compare channels, and one channel that can be configured as a fourth input capture or a fifth output compare.

Refer to the following table for a summary of the crystal-related frequencies and periods.

Timer Summary

Control Bits	XTAL Frequencies			
	8.0 MHz	12.0 MHz	16.0 MHz	Other Rates
	2.0 MHz	3.0 MHz	4.0 MHz	(E)
	500 ns	333 ns	250 ns	(1/E)
PR[1:0]	Main Timer Count Rates			
0 0				
1 count —	500 ns	333 ns	250 ns	(E/1)
overflow —	32.768 ms	21.845 ms	16.384 ms	$(E/2^{16})$
0 1				
1 count —	2.0 µs	1.333 µs	1.0 µs	(E/4)
overflow —	131.07 ms	87.381 ms	65.536 ms	$(E/2^{18})$
1 0				
1 count —	4.0 µs	2.667 µs	2.0 µs	(E/8)
overflow —	262.14 ms	174.76 ms	131.07 ms	$(E/2^{19})$
1 1				
1 count —	8.0 µs	5.333 µs	4.0 µs	(E/16)
overflow —	524.29 ms	349.52 ms	262.14 ms	$(E/2^{20})$
RTR[1:0]	Periodic Interrupt (RTI) Rates			
0 0	4.096 ms	2.731 ms	2.048 ms	$(E/2^{13})$
0 1	8.192 ms	5.461 ms	4.096 ms	$(E/2^{14})$
1 0	16.384 ms	10.923 ms	8.192 ms	$(E/2^{15})$
1 1	32.768 ms	21.845 ms	16.384 ms	$(E/2^{16})$
CR[1:0]	COP Watchdog Timeout Rates			
0 0	16.384 ms	10.923 ms	8.192 ms	$(E/2^{15})$
0 1	65.536 ms	43.691 ms	32.768 ms	$(E/2^{17})$
1 0	262.14 ms	174.76 ms	131.07 ms	$(E/2^{19})$
1 1	1.049 s	699.05 ms	524.28 ms	$(E/2^{21})$
Timeout Tolerance (− 0 ms/+...)	16.4 ms	10.9 ms	8.192 ms	$(E/2^{15})$
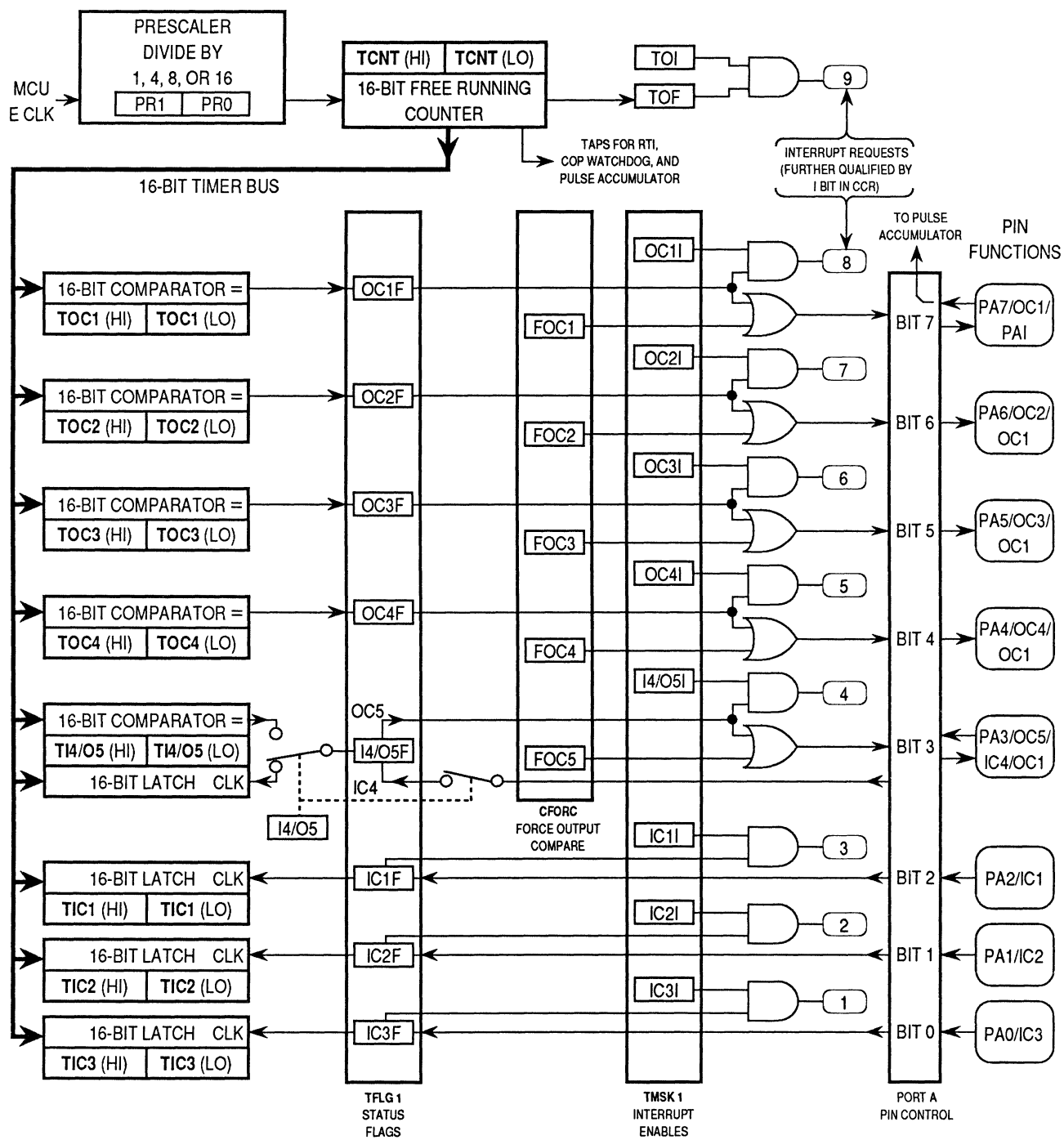
Timer Block Diagram

CFORC — Timer Compare Force $000B

Bit 7	6	5	4	3	2	1	Bit 0
FOC1	FOC2	FOC3	FOC4	FOC5	—	—	—

RESET: 0   0   0   0   0   0   0   0

FOC[5:1] — Force Output Comparison
When the FOC bit associated with an output compare circuit is set, the output compare circuit immediately performs the action it is programmed to do when an output match occurs.
0 = Not affected
1 = Output x action occurs

Bits [2:0] — Not implemented
Always read zero

OC1M — Output Compare 1 Mask $000C

Bit 7	6	5	4	3	2	1	Bit 0
OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	—	—	—

RESET: 0   0   0   0   0   0   0   0

Set bit(s) to enable OC1 to control corresponding pin(s) of port A

Bits [2:0] — Not implemented
Always read zero

OC1D — Output Compare 1 Data $000D

Bit 7	6	5	4	3	2	1	Bit 0
OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	—	—	—

RESET: 0   0   0   0   0   0   0   0

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits [2:0] — Not implemented
Always read zero

TCNT — Timer Count $000E, $000F

	Bit 15	14	13	12	11	10	9	Bit 8	High	**TCNT**
$000E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TCNT**
$000F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000. In normal modes, TCNT is read-only.

TIC1–TIC3 — Timer Input Capture $0010–$0015

$0010	Bit 15	14	13	12	11	10	9	Bit 8	High **TIC1**
$0011	Bit 7	6	5	4	3	2	1	Bit 0	Low
$0012	Bit 15	14	13	12	11	10	9	Bit 8	High **TIC2**
$0013	Bit 7	6	5	4	3	2	1	Bit 0	Low
$0014	Bit 15	14	13	12	11	10	9	Bit 8	High **TIC3**
$0015	Bit 7	6	5	4	3	2	1	Bit 0	Low

TICx not affected by reset.

TOC1–TOC4 — Timer Output Compare $0016–$001D

$0016	Bit 15	14	13	12	11	10	9	Bit 8	High **TOC1**
$0017	Bit 7	6	5	4	3	2	1	Bit 0	Low
$0018	Bit 15	14	13	12	11	10	9	Bit 8	High **TOC2**
$0019	Bit 7	6	5	4	3	2	1	Bit 0	Low
$001A	Bit 15	14	13	12	11	10	9	Bit 8	High **TOC3**
$001B	Bit 7	6	5	4	3	2	1	Bit 0	Low
$001C	Bit 15	14	13	12	11	10	9	Bit 8	High **TOC4**
$001D	Bit 7	6	5	4	3	2	1	Bit 0	Low

All TOCx register pairs reset to ones ($FFFF).

TI4/O5 — Timer Input Capture 4/Output Compare 5 $001E, $001F

$001E	Bit 15	14	13	12	11	10	9	Bit 8	High
$001F	Bit 7	6	5	4	3	2	1	Bit 0	Low

All TI4/O5 register pairs reset to ones ($FFFF).

TCTL1 — Timer Control 1 $0020

	Bit 7	6	5	4	3	2	1	Bit 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM[5:2] — Output Mode

OL[5:2] — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to 0
1	1	Set OCx output line to 1

TCTL2 — Timer Control 2 $0021

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TMSK1 — Timer Interrupt Mask 1 $0022

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I – OC4I — Output Compare x Interrupt Enable

I4/O5I — Input Capture 4 or Output Compare 5 Interrupt Enable

IC1I – IC3I — Input Capture x Interrupt Enable

NOTE

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

TFLG1 — Timer Interrupt Flag 1 $0023

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

OC1F – OC4F — Output Compare x Flag
Set each time the counter matches output compare x value

I4/O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on which function was enabled by I4/O5 of PACTL

IC1F – IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line

---

TMSK2 — Timer Interrupt Mask 2 $0024

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable

RTII — Real-time Interrupt Enable

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

PAOVI — Pulse Accumulator Overflow Interrupt Enable
Refer to **Pulse Accumulator**.

PAII — Pulse Accumulator Input Interrupt Enable
Refer to **Pulse Accumulator**.

Bits [3:2] — Not implemented
Always read zero

PR[1:0] — Timer Prescaler Select

In normal modes, PR0 and PR1 can only be written once, and the write must occur within 64 cycles after reset. The following table shows the prescaler selected with each combination of PR[1:0]. Refer to **Timer Summary** table for specific timing values.

PR[1:0]	Prescaler
0 0	÷ 1
0 1	÷ 4
1 0	÷ 8
1 1	÷ 16

TFLG2 — Timer Interrupt Flag 2 $0025

Bit 7	6	5	4	3	2	1	Bit 0
TOF	RTIF	PAOVF	PAIF	—	—	—	—

RESET: 0   0   0   0   0   0   0   0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time (Periodic) Interrupt Flag
Set periodically. Refer to RTR[1:0] in PACTL register.

PAOVF — Pulse Accumulator Overflow Flag
Refer to **Pulse Accumulator**.

PAIF — Pulse Accumulator Input Edge Flag
Refer to **Pulse Accumulator**.

Bits [3:0] — Not implemented
Always read zero

Bit 7	6	5	4	3	2	1	Bit 0
—	PAEN	PAMOD	PEDGE	—	I4/O5	RTR1	RTR0

RESET: 0   0   0   0   0   0   0   0

Bit 7 — Not implemented
   Always read zero

PAEN — Pulse Accumulator System Enable
   Refer to **Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode
   Refer to **Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Control
   Refer to **Pulse Accumulator**.

Bit 3 — Not implemented
   Always reads zero

I4/O5 — Input Capture 4/Output Compare 5
   Configure TI4/O5 for input capture or output compare
      0 = OC5 enabled
      1 = IC4 enabled

RTR[1:0] — Real-Time Interrupt (RTI) Rate

Real-Time Interrupt Rates

RTR [1:0]	Divide E By	XTAL = 8.0 MHz	XTAL = 12.0 MHz	XTAL = 16.0 MHz
0 0	2^{13}	4.096 ms	2.731 ms	2.048 ms
0 1	2^{14}	8.192 ms	5.461 ms	4.096 ms
1 0	2^{15}	16.384 ms	10.923 ms	8.192 ms
1 1	2^{16}	32.768 ms	21.845 ms	16.383 ms
	E =	2.0 MHz	3.0 MHz	4.0 MHz

Bit 7	6	5	4	3	2	1	Bit 0
ADPU	CSEL	IRQE*	DLY*	CME	FCME*	CR1*	CR0*

RESET: 0   0   0   1   0   0   0   0

*Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes.

ADPU — A/D Converter Power up
    Refer to **Analog-to-Digital Converter**.

CSEL — Clock Select
    0 = A/D and ROM/EPROM use system E clock
    1 = A/D and ROM/EPROM use internal RC clock

IRQE — IRQ Select Edge-Sensitive Only
    Refer to **Resets and Interrupts**.

DLY — Enable Oscillator Startup Delay
    Refer to **Resets and Interrupts**.

CME — Clock Monitor Enable
    0 = Clock monitor disabled; slow clocks can be used
    1 = Slow or stopped clocks cause clock failure reset

FCME — Force Clock Monitor Enable
    0 = Clock monitor follows the state of the CME bit
    1 = Clock monitor circuit is enabled until next reset

CR[1:0] — COP Timer Rate Select
    Refer to the following table of COP timer rates.

COP Timer Rate Select

CR[1:0]	Divide $E/2^{15}$ By	XTAL = 8.0 MHz Timeout −0/+16.4 ms	XTAL = 12.0 MHz Timeout −0/+10.9 ms	XTAL = 16.0 MHz Timeout −0/+8.2 ms
0 0	1	16.384 ms	10.923 ms	8.192 ms
0 1	4	65.536 ms	43.691 ms	32.768 ms
1 0	16	262.14 ms	174.76 ms	131.07 ms
1 1	64	1.049 sec	699.05 ms	524.29 ms
	E =	2.0 MHz	3.0 MHz	4.0 MHz

Pulse Accumulator

The MC68HC11M2 has an 8-bit counter that can be configured for gated time accumulation or to operate as a simple event counter. The pulse accumulator counter can be read or written at any time.

The PA7 pin can be configured to act as a clock in event counting mode, or as a gate signal to enable a free-running clock (E divided by 64) to the 8-bit counter in gated time accumulation mode.

	Selected	Common XTAL Frequencies		
	Crystal	8.0 MHz	12.0 MHz	16.0 MHz
CPU Clock	(E)	2.0 MHz	3.0 MHz	4.0 MHz
Cycle Time	(1/E)	500 ns	333 ns	250 ns
Pulse Accumulator (in Gated Mode)				
$(E/2^6)$	1 count —	32.0 µs	21.330 µs	16.0 µs
$(E/2^{14})$	overflow —	8.192 ms	5.461 ms	4.096 ms
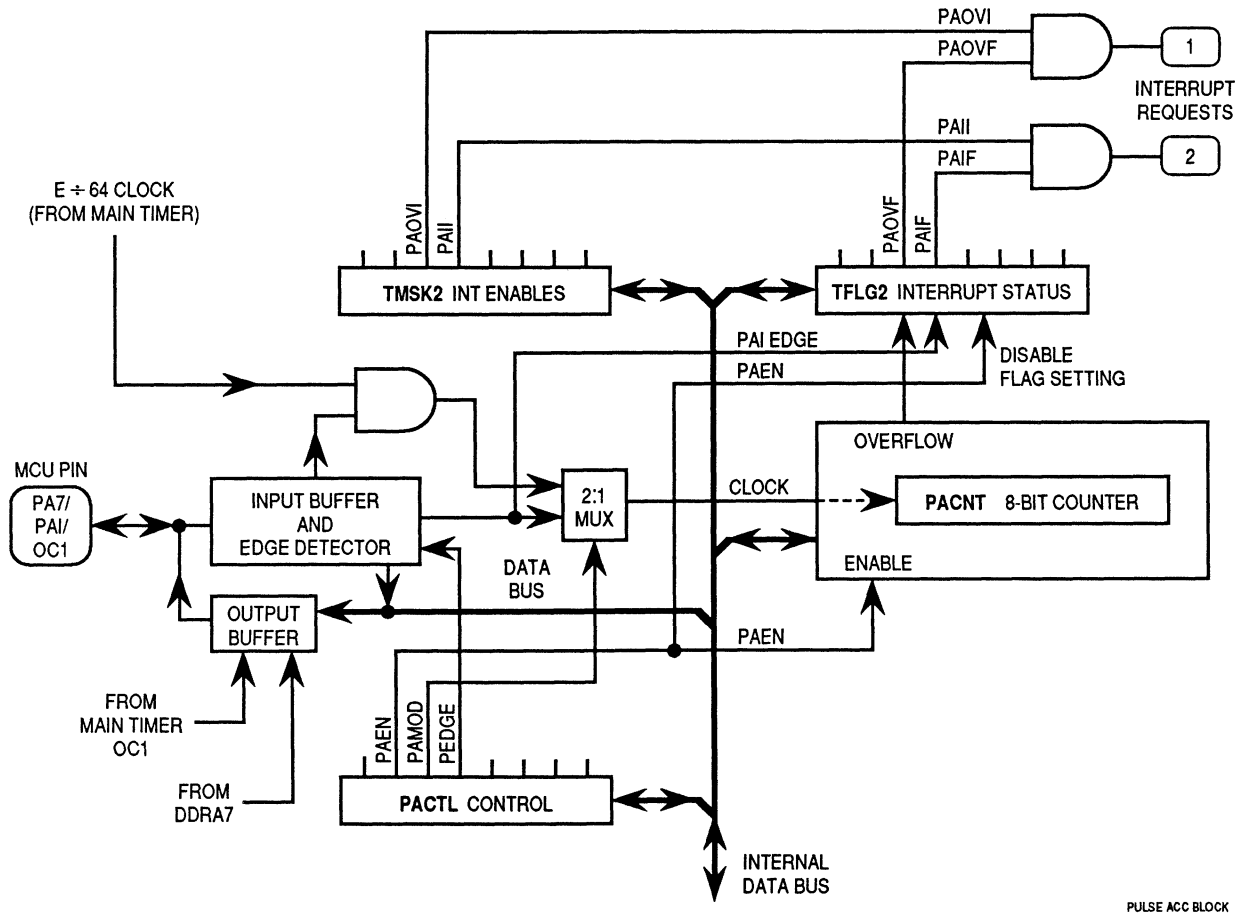
Pulse Accumulator System Block Diagram

Bit 7	6	5	4	3	2	1	Bit 0
TOI	RTII	PAOVI	PAII	—	—	PR1	PR0

RESET: 0 0 0 0 0 0 0 0

TOI — Timer Overflow Interrupt Enable
Refer to **Main Timer**.

RTII — Real-time Interrupt Enable
Refer to **Main Timer**.

PAOVI — Pulse Accumulator Overflow Interrupt Enable

PAII — Pulse Accumulator Input Edge Interrupt Enable

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

Bits [3:2] — Not implemented
Always read zero

PR[1:0] — Timer Prescaler Select
Refer to **Main Timer**.

TFLG2 — Timer Interrupt Flag 2 $0025

Bit 7	6	5	4	3	2	1	Bit 0
TOF	RTIF	PAOVF	PAIF	—	—	—	—

RESET: 0 0 0 0 0 0 0 0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Refer to **Main Timer**.

RTIF — Real-Time (Periodic) Interrupt Flag
Refer to **Main Timer**.

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line

Bits [3:0] — Not implemented
Always read zero

PACTL — Pulse Accumulator Control $0026

Bit 7	6	5	4	3	2	1	Bit 0
—	PAEN	PAMOD	PEDGE	—	I4/O5	RTR1	RTR0

RESET: 0   0   0   0   0   0   0   0

Bit 7 — Not implemented
   Always reads zero

PAEN — Pulse Accumulator System Enable
   0 = Pulse Accumulator disabled
   1 = Pulse Accumulator enabled

PAMOD — Pulse Accumulator Mode
   0 = Event counter
   1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control
   0 = Falling edges, high level enables accumulation
   1 = Rising edges, low level enables accumulation

Bit 3 — Not implemented
   Always reads zero

I4/O5 — Input Capture 4/Output Compare 5
   Refer to **Main Timer**.

RTR[1:0] — Real-Time Interrupt Rate
   Refer to **Main Timer**.

PACNT — Pulse Accumulator Counter $0027

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

Can be read and written.

Pulse-Width Modulation Timer

The MC68HC11M2 MCU contains a four-channel pulse-width modulation (PWM) timer. By concatenating channels, the period length of channels 1/2 and 3/4 can be up to 16 bits long. Each channel has a counter, a duty register, a control bit located in the PWM enable register, and a polarity bit located in the polarity select register. Two channels have the capability to produce extended-frequency PWM waveforms.

Each duty register is double buffered. When a channel is active, writes to the duty register are buffered until the counter rolls over or the channel is disabled. At this time the new duty takes effect. This design requires the output to be either the old duty waveform or the new duty waveform. If the channel is not enabled, writes to the duty register go directly to the latches and the buffer.

The previous MC68HC11 PWM system is a flexible 4-channel, 8-bit system with the ability to concatenate channels and produce waveforms with resolutions of up to 16 bits. However, as the frequency of the duty cycle increases, the maximum output frequency of the PWM decreases. The PWM system in the MC68HC11M2 has a rate multiplier added to channels two and four. Refer to the Extended Rate PWM Block Diagram.

The lower six bits of the new extended rate PWM extended duty register (PWDT2R and PWDT4R) are used as the input data to the rate modulation unit. Refer to the Extended Rate PWM Block Diagram. The upper bits of the corresponding old PWM channel are still used to select the period and duty. If a PWM resolution of 10 bits is selected (represented by the six bits of the extended duty register PWDTxR and four bits of the old PWM duty register PWDTYx), this duty cycle can be output up to 64 times the rate of the old PWM output. The shortest pulse that can be output is that of the prescaled clock — one E-clock pulse. This is referred to as a unit pulse. Unit pulses are appended to the duty cycle according to values written to the extended duty register. Refer to the following table.

Lower Six Bits of PWDTxR						Unit Pulse Appended Every:
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	1	64 Pulses
0	0	0	0	1	0	32 Pulses
0	0	0	1	0	0	16 Pulses
0	0	1	0	0	0	8 Pulses
0	1	0	0	0	0	4 Pulses
1	0	0	0	0	0	2 Pulses

MCU E CLOCK

÷1
÷2
÷4
÷8
÷16
÷32
÷64
÷128

PCKA1
PCKA2
SELECT

8-BIT COMPARE =
PWSCAL
÷2
CLOCK S

8

8-BIT COUNTER
RESET

CLOCK A

PCKB1
PCKB2
PCKB3
SELECT
CLOCK B

PCLK3
PCLK4
CLOCK SELECT
PWEN3
PWEN4
CON34

PCLK1
PCLK2
CLOCK SELECT
PWEN1
PWEN2
CON12

CNT4   CNT3

CNT2   CNT1

PPOL1

16-BIT PWM CONTROL

S   Q
R   Q̄
MUX
BIT 0
PH0/PW1

S   Q
R   Q̄
MUX
BIT 1
PH1/PW2

PPOL2

8-BIT COMPARE =
PWDTY1

8-BIT COMPARE =
PWDTY2

8-BIT COMPARE =
PWPER1

8-BIT COMPARE =
PWPER2

8

8

RESET
PWCNT1

RESET
PWCNT2
CARRY

CON12

PORT H PIN CONTROL

PPOL3

16-BIT PWM CONTROL

S   Q
R   Q̄
MUX
BIT 2
PH2/PW3

S   Q
R   Q̄
MUX
BIT 3
PH3/PW4

8-BIT COMPARE =
PWDTY3

8-BIT COMPARE =
PWDTY4

8-BIT COMPARE =
PWPER3

8-BIT COMPARE =
PWPER4

8

8

RESET
PWCNT3

RESET
PWCNT4
CARRY

CON34

PPOL4

PWMX

PWDTY
PWPER

PWM BLOCK 4CH

PWM Block Diagram
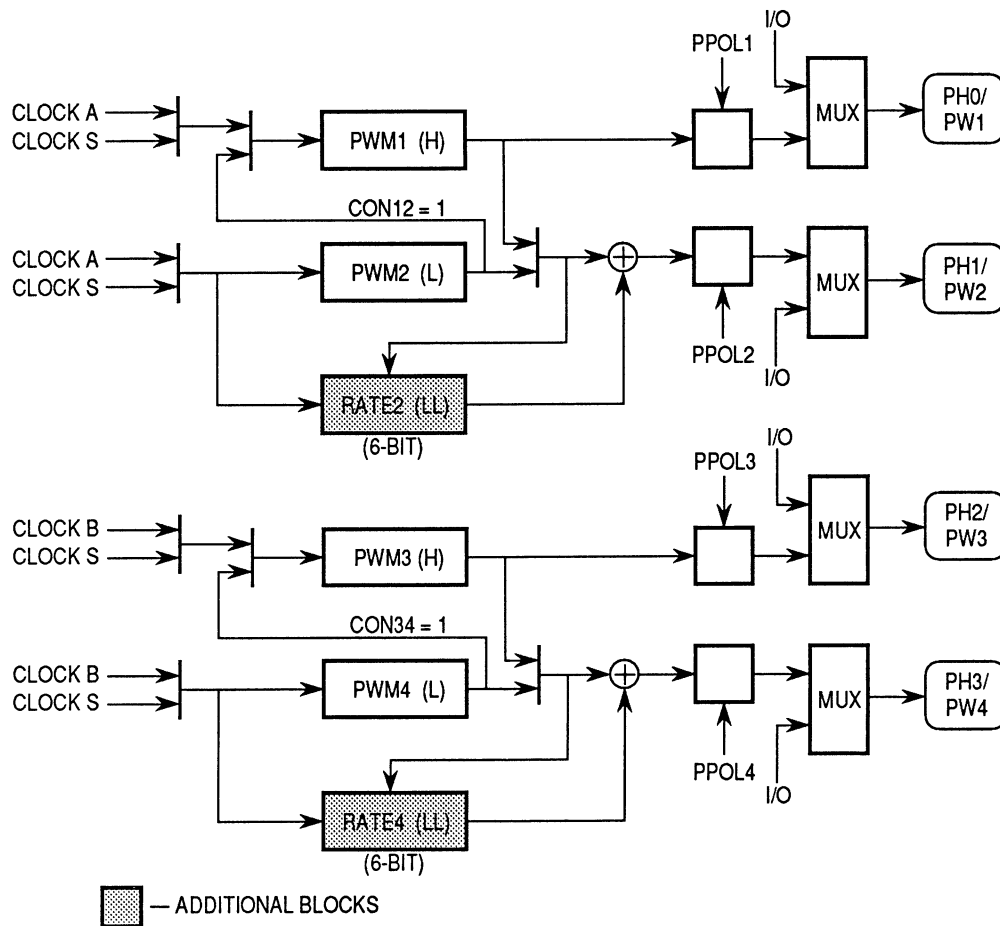
Maximum Frequency of PWM Outputs (E = 4 MHz)

Resolution	8-Bit (2 +6)	10-Bit (4 +6)	12-Bit (6 +6)	14-Bit (8 +6)	16-Bit (10 +6)	18-Bit (12 +6)	20-Bit (14 +6)	22-Bit (16 +6)
Normal PWM	15.6 kHz	3.9 kHz	976 Hz	244 Hz	61 Hz	—	—	—
Ext Rate PWM	1 MHz	250 kHz	62.4 kHz	15.6 kHz	3.9 kHz	976 Hz	244 Hz	61 Hz

EXTENDED RATE PWM BLOCK

Extended Rate PWM Block Diagram

	Bit 7	6	5	4	3	2	1	Bit 0
	CON34	CON12	PCKA2	PCKA1	—	PCKB3	PCKB2	PCKB1
RESET:	0	0	0	0	0	0	0	0

CON34 — Concatenate Channels 3 and 4
    1 = Channels 3 and 4 are concatenated to create one 16-bit PWM channel.
    0 = Channels 3 and 4 are separate 8-bit PWMs.

CON12 — Concatenate Channels 1 and 2
    1 = Channels 1 and 2 are concatenated to create one 16-bit PWM channel.
    0 = Channels 1 and 2 are separate 8-bit PWMs.

PCKA[2:1] — Prescaler for Clock A
    Determine rate of clock A

PCKA2	PCKA1	Value of Clock A
0	0	E
0	1	E/2
1	0	E/4
1	1	E/8

Bit 3 — Not implemented
    Always reads zero

PCKB[3:1] — Prescaler for Clock B
    Determine rate of clock B

PCKB3	PCKB2	PCKB1	Value of Clock B
0	0	0	E
0	0	1	E/2
0	1	0	E/4
0	1	1	E/8
1	0	0	E/16
1	0	1	E/32
1	1	0	E/64
1	1	1	E/128

PWPOL — Pulse-Width Polarity   **$0061**

Bit 7	6	5	4	3	2	1	Bit 0
PCLK4	PCLK3	PCLK2	PCLK1	PPOL4	PPOL3	PPOL2	PPOL1

RESET: 0   0   0   0   0   0   0   0

Note that while PWPOL can be written at any time, doing so while a PWM channel is active may produce a stretched or truncated waveform.

PCLK4 — Pulse Width Channel 4 Clock Select
    0 = Clock B is clock source for channel 4
    1 = Clock S (scaled) is the clock source for channel 4

PCLK3 — Pulse Width Channel 3 Clock Select
    0 = Pulse width channel 3 clock source is clock S
    1 = Clock B is clock source for channel 3

PCLK2 — Pulse Width Channel 2 Clock Select
    0 = Clock A is clock source for channel 2
    1 = Clock S (scaled) is the clock source for channel 2

PCLK1 — Pulse Width Channel 1 Clock Select
    0 = Clock A is clock source for channel 1
    1 = Clock S (scaled) is the clock source for channel 1

PPOL[4:1] — Pulse-Width Channel x Polarity
    0 = PWM channel x output is low at the beginning of the clock cycle and goes high when duty count is reached
    1 = PWM channel x output is high at the beginning of the clock cycle and goes low when duty count is reached

---

PWSCAL — Pulse-Width Scale   **$0062**

Bit 7	6	5	4	3	2	1	Bit 0
7	6	5	4	3	2	1	0

RESET: 0   0   0   0   0   0   0   0

PWEN — Pulse-Width Modulation Timer Enable   **$0063**

Bit 7	6	5	4	3	2	1	Bit 0
TPWSL	DISCP	CON4R	CON2R	PWEN4	PWEN3	PWEN2	PWEN1

RESET: 0   0   0   0   0   0   0   0

TPWSL — PWM Scaled Clock Test Bit (TEST)
    0 = Normal operation
    1 = Clock S is output and is readable on the PWSCAL register

DISCP — Disable Compare Scaled E Clock (TEST)
    0 = Normal Operation
    1 = Match of period does not reset associated count register

CON4R — Concatenate Channel 4

Ties the 6-bit extension duty register (PWDT4R) to the PWM channel 4. Depending on the state of CON34 and this bit, the order that data is written to the duty register is altered.

CON34	CON4R	
0	0	Value written into PWDTY3 or PWDTY4 transferred to PWM internal compare register upon completion of current period (8-bit mode PWM)
0	1	Upon completion of current period, values written to PWDTY4 and the concatenated PWDT4R are transferred to internal compare registers (14-bit effective PWM)
1	0	Upon completion of the current period, values written to PWDTY3 and the attached PWDTY4 are transferred to their respective internal compare registers (16-bit mode PWM)
1	1	Upon completion of the current PWM period, the values written to PWDTY3, PWDTY4, and PWDT4R are transferred to their respective internal compare registers (22-bit effective PWM)

CON2R — Concatenate Channel 2

Ties the PWM 6-bit extension duty register (PWDT2R) to the PWM channel 2. Depending on the state of CON12 and this bit, the order that data is written to the duty register is altered.

CON12	CON2R	
0	0	Value written into PWDTY1 or PWDTY2 transferred to PWM internal compare register upon completion of current period (8-bit mode PWM)
0	1	Upon completion of current period, values written to PWDTY2 and the concatenated PWDT2R are transferred to internal compare registers (14-bit effective PWM)
1	0	Upon completion of the current period, values written to PWDTY1 and the attached PWDTY2 are transferred to their respective internal compare registers (16-bit mode PWM)
1	1	Upon completion of the current PWM period, the values written to PWDTY1, PWDTY2, and PWDT2R are transferred to their respective internal compare registers (22-bit effective PWM)

PWEN[4:1] — Pulse-Width Channel 4–1

0 = Channel disabled
1 = Channel enabled

PWCNTx — Pulse-Width Channel Count   **$0064–$0067**

	Bit 7	6	5	4	3	2	1	Bit 0	
$0064	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT1
$0065	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT2
$0066	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT3
$0067	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT4
RESET:	0	0	0	0	0	0	0	0	

PWPER — Pulse-Width Channel Period $0068–$006B

	Bit 7	6	5	4	3	2	1	Bit 0	
$0068	Bit 7	6	5	4	3	2	1	Bit 0	PWPER1
$0069	Bit 7	6	5	4	3	2	1	Bit 0	PWPER2
$006A	Bit 7	6	5	4	3	2	1	Bit 0	PWPER3
$006B	Bit 7	6	5	4	3	2	1	Bit 0	PWPER4
RESET:	0	0	0	0	0	0	0	0	

PWDTYx — Pulse-Width Channel Duty $006C–$006E

	Bit 7	6	5	4	3	2	1	Bit 0	
$006C	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY1
$006D	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY2
$006E	Bit 7	6	5	4	3	2	1	Bit 0	PWDT2R
RESET:	$FF for PWM; $00 for extension								

PWDTYx — Pulse-Width Channel Duty $005C–$005E

	Bit 7	6	5	4	3	2	1	Bit 0	
$005C	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY3
$005D	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY4
$005E	—	—	Bit 5	4	3	2	1	Bit 0	PWDT4R
RESET:	$FF for PWM; $00 for extension								

The count in these registers determines the duty of the associated PWM channel.

Boundary Cases

Boundary cases are situations in which values in PWM control registers cause outputs or conditions that might not be what the user expects. These values and the resulting outputs are described as follows:

- If PWDTYx = $00, PWPERx > $00, and PPOLx = 0; then outputx is always high.

- If PWDTYx = $00, PWPERx > $00, and PPOLx = 1; then outputx is always low.

- If PWDTYx ≥ PWPERx and PPOLx = 0; then outputx is always low.

- If PWDTYx ≥ PWPERx and PPOLx = 1; then outputx is always high.

- If PWPERx = $00 and PPOLx = 0; then outputx is always low.

- If PWPERx = $00 and PPOLx = 1; then outputx is always high.

Serial Communications Interface

The serial communications interface (SCI), a universal asynchronous receiver transmitter (UART), is one of two independent serial I/O subsystems in the MC68HC11M2. Rearranging registers and control bits used in previous MC68HC11 family devices has enhanced the existing SCI system and added new features, which include the following:

- A 13-bit modulus prescaler that allows greater baud rate control
- A new idle mode detect, independent of preceding serial data
- A receiver active flag
- Hardware parity for both transmitter and receiver

The modulus prescaler allows baud rate selection from E/2 to E/2^{13}. Refer to the table of SCI baud rate control values for standard values and methods of calculation.

MODULUS BAUD GEN BLOCK
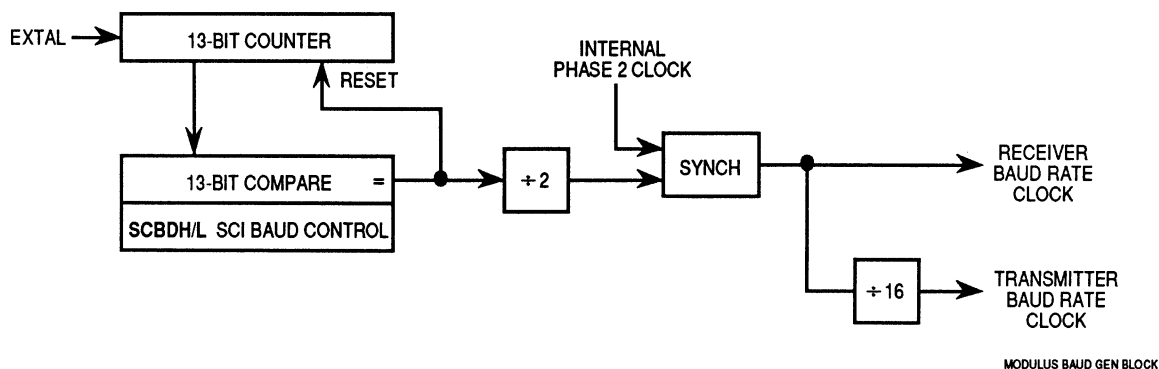
SCI Baud Generator Circuit Diagram
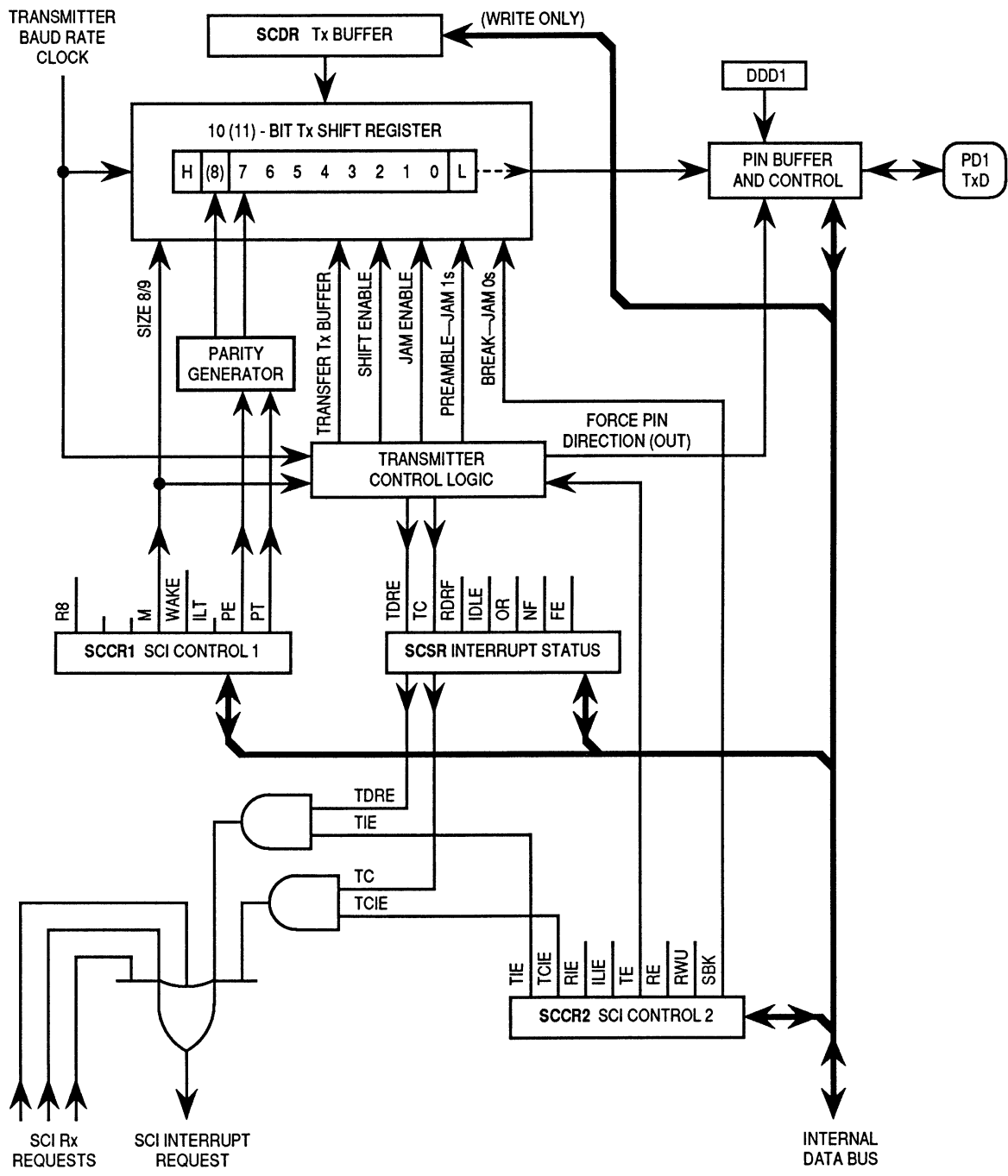
SCI Transmitter Block Diagram
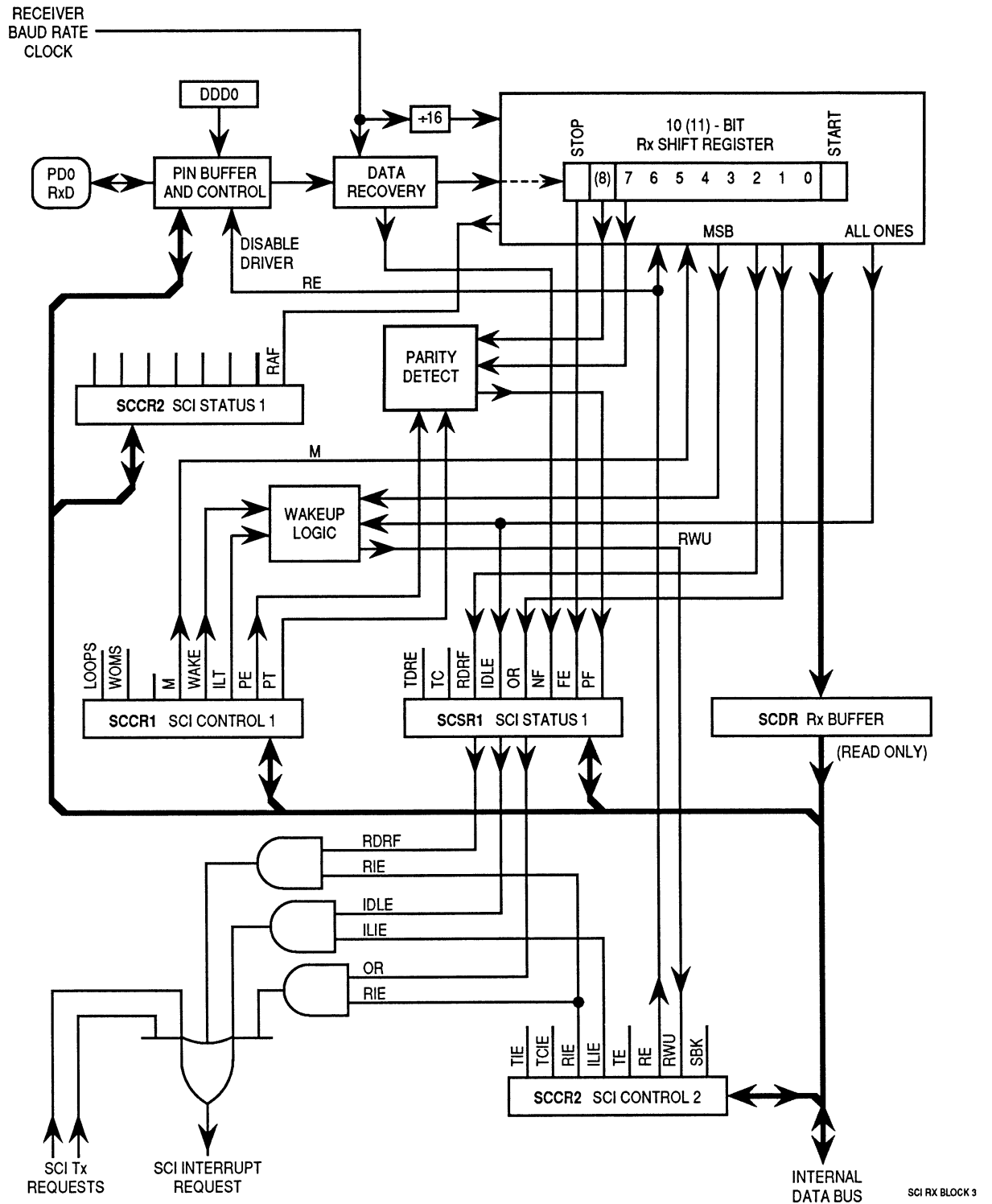
SCI Receiver Block Diagram

	Bit 7	6	5	4	3	2	1	Bit 0	
$0070	BTST	BSPL	—	SBR12	SBR11	SBR10	SBR9	SBR8	High
RESET:	0	0	0	0	0	0	0	0	
$0071	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	Low
RESET:	0	0	0	0	0	1	0	0	

BTST — Baud Register Test (TEST)

BSPL — Baud Rate Counter Split (TEST)

5 — Not implemented
Always reads zero

[12:0] — SCI Baud Rate Selects
Use the following formula to calculate SCI baud rate. Refer to the table of baud rate control values for example rates.

$$\text{SCI baud rate} = \text{EXTAL} \div [16 \cdot (2 \cdot BR)]$$

where

BR is the contents of SCBDH, L (BR = 1, 2, 3, ... 8191).

BR = 0 disables the baud rate generator.

SCI Baud Rate Control Values

Target Baud Rate	Crystal Frequency					
	8 MHz		12 MHz		16 MHz	
	Decimal	Hex	Decimal	Hex	Decimal	Hex
110	2272	$08E0	3409	$0D51	4545	$11C1
150	1666	$0682	2500	$09C4	3333	$0D05
300	833	$0341	1250	$04E2	1666	$0682
600	416	$01A0	625	$0271	833	$0341
1200	208	$00D0	312	$0138	416	$01A0
2400	104	$0068	156	$009C	208	$00D0
4800	52	$0034	78	$004E	104	$0068
9600	26	$001A	39	$0027	52	$0034
19.2 K	13	$000D	20	$0014	26	$001A
38.4 K	—	—	—	—	13	$000D

	Bit 7	6	5	4	3	2	1	Bit 0
	LOOPS	WOMS	—	M	WAKE	ILT	PE	PT
RESET:	0	0	0	0	0	0	0	0

LOOPS — SCI LOOP Mode Enable
 0 = SCI transmit and receive operate normally
 1 = SCI transmit and receive are disconnected from TxD and RxD pins, and transmitter output is fed back into the receiver input

WOMS — Wired-OR Mode for SCI Pins PD[1:0]
 See also DWOM bit in SPCR1.
 0 = TxD and RxD operate normally
 1 = TxD and RxD are open drains if operating as an output

Bit 5 — Not implemented
 Always reads zero

M — Mode (Select Character Format)
 0 = Start bit, 8 data bits, 1 stop bit
 1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup by Address Mark/Idle
 0 = Wakeup by IDLE line recognition
 1 = Wakeup by address mark (most significant data bit set)

ILT — Idle Line Type
 0 = Short (SCI counts consecutive ones after start bit)
 1 = Long (SCI counts ones only after stop bit)

PE — Parity Enable
 0 = Parity disabled
 1 = Parity enabled

PT — Parity Type
 0 = Parity even (even number of ones causes parity bit to be zero, odd number of ones causes parity bit to be one)
 1 = Parity odd (odd number of ones causes parity bit to be zero, even number of ones causes parity bit to be one)

	Bit 7	6	5	4	3	2	1	Bit 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
    0 = TDRE interrupts disabled
    1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
    0 = TC interrupts disabled
    1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
    0 = RDRF and OR interrupts disabled
    1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
    0 = IDLE interrupts disabled
    1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
    0 = Transmitter disabled
    1 = Transmitter enabled

RE — Receiver Enable
    0 = Receiver disabled
    1 = Receiver enabled

RWU — Receiver Wakeup Control
    0 = Normal SCI receiver
    1 = Wakeup enabled and receiver interrupts inhibited

SBK — Send Break
    0 = Break generator off
    1 = Break codes generated as long as SBK = 1

	Bit 7	6	5	4	3	2	1	Bit 0
	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag

This flag is set when SCDR is empty. Clear the TDRE flag by reading SCSR1 with TDRE set and then writing to SCDR.

    0 = SCDR busy
    1 = SCDR empty

TC — Transmit Complete Flag

This flag is set when the transmitter is idle (no data, preamble, or break transmission in progress). Clear the TC flag by reading SCSR1 with TC set and then writing to SCDR.

    0 = Transmitter busy
    1 = Transmitter idle

RDRF — Receive Data Register Full Flag

Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. RDRF is set if a received character is ready to be read from SCDR. Clear the RDRF flag by reading SCSR1 with RDRF set and then reading SCDR.

    0 = SCDR empty
    1 = SCDR full

IDLE — Idle Line Detected Flag

This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR1 with IDLE set and then reading SCDR.

    0 = RxD line is active
    1 = RxD line is idle

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR1 with OR set and then reading SCDR.

    0 = No overrun
    1 = Overrun detected

NF — Noise Error Flag

NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR1 with NF set and then reading SCDR.

    0 = Unanimous decision
    1 = Noise detected

FE — Framing Error

FE is set when a zero is detected where a stop bit was expected. Clear the FE flag by reading SCSR1 with FE set and then reading SCDR.

    0 = Stop bit detected
    1 = Zero detected

PF — Parity Error Flag

PF is set if received data has incorrect parity. Clear PF by reading SCSR1 with PE set and then reading SCDR.

0 = Parity correct
1 = Incorrect parity detected

SCSR2 — SCI Status Register 2   **$0075**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	—	—	—	—	—	RAF
RESET:	0	0	0	0	0	0	0	0

Bits [7:1] — Not implemented
Always read zero

RAF — Receiver Active Flag (Read Only)
0= A character is not being received.
1 = A character is being received.

SCDRH/L — SCI Data Register High/Low   **$0076, $0077**

	Bit 7	6	5	4	3	2	1	Bit 0	
$0076	R8	T8	—	—	—	—	—	—	SCDRH (High)
$0077	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDRL (Low)

R8 — Receiver Bit 8
Ninth serial data bit received when SCI is configured for nine data bit operation.

T8 — Transmitter Bit 8
Ninth serial data bit transmitted when SCI is configured for nine data bit operation.

Bits [5:0] — Not implemented
Always read zero

R[7:0]/T[7:0] — Receiver/Transmitter Data Bits 7 to 0
SCI data is double buffered in both directions.

Serial Peripheral Interface

The SPI is one of two independent serial communications subsystems on the MC68HC11M2 and allows the MCU to communicate synchronously with peripheral devices and other microprocessors. Data rates can be as high as 2 Mbits per second when configured as a master and 4 Mbits per second when configured as a slave (assuming 4 MHz bus speed). New serial configuration mode and DMA link features have been added to both the SPI 1 and SPI 2.

Two control bits in OPT2 and OPT4 allow the user to transfer either MSB or LSB first and select an additional divide by four stage to be inserted before the SPI baud rate clock divider.

When the SPI is enabled, all pins that are defined by the configuration as inputs are inputs regardless of the state of the DDR bits for those pins. All pins that are defined as outputs will be outputs only if the DDR bits for those pins are set to one. Any SPI output whose corresponding DDR bit is set to zero can be used as a general-purpose input. If the SPI system is in master mode and DDRD (G) is set to one, the port D (G) bit 5 pin becomes a general-purpose output bit instead of the $\overline{SS}$ input to the SPI system. The MODF mode error flag function for which $\overline{SS}$ was used becomes disabled to avoid interference between the general-purpose output function and the SPI system.

SPI (1 and 2) Block Diagram

Bit 7	6	5	4	3	2	1	Bit 0
SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0

RESET: 0   0   0   0   0   1   U   U

SPIE — Serial Peripheral Interrupt Enable
    0 = SPI interrupts disabled
    1 = SPI interrupts enabled

SPE — Serial Peripheral System Enable
    0 = SPI off
    1 = SPI on

DWOM — Port D Wired-OR Mode Option for SPI Pins PD[5:2]
    See also WOMS bit in SCCR1.
    0 = Normal CMOS outputs
    1 = Open-drain outputs

MSTR — Master Mode Select
    0 = Slave mode
    1 = Master mode

CPOL, CPHA — Clock Polarity, Clock Phase
    Refer to **SPI (1 and 2) Transfer Format**.
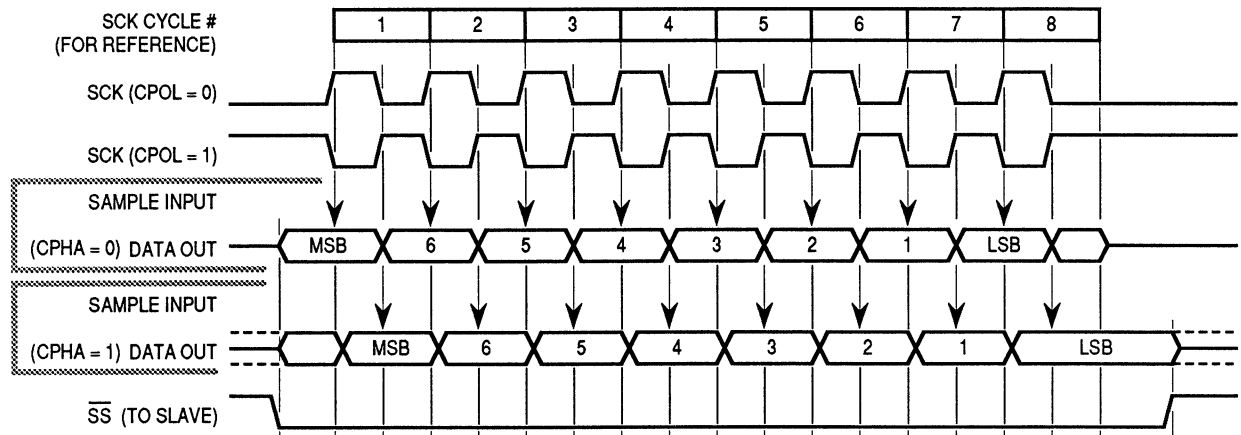
SPI TRANSFER FORMAT

SPI (1 and 2) Transfer Format

NOTE

This figure shows LSBF = 0 default. If LSBF = 1, data is transferred in reverse order (LSB first).

SPR21, SPR[1:0] — SPI Clock Rate Selects
(SPR21 is located in OPT2 register, SPR[1:0] are located in SPCR1 register)

SPI 1 Clock Rate Selects

SPR21	SPR1	SPR0	E Clock Divided by	Freqency at E = 4 MHz (Baud Rate)
0	0	0	2	2.0 MHz
0	0	1	4	1.0 MHz
0	1	0	16	250 kHz
0	1	1	32	125 kHz
1	0	0	8	500 kHz
1	0	1	16	250 kHz
1	1	0	64	62.5 kHz
1	1	1	128	31.3 kHz

SPCR2 — Serial Peripheral Control 2 $0088

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	GWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
    0 = SPI interrupts disabled
    1 = SPI interrupts enabled

SPE — Serial Peripheral System Enable
    0 = SPI off
    1 = SPI on

GWOM — Port G Wired-OR Mode Option for SPI Pins PG[5:2]
    0 = Normal CMOS outputs
    1 = Open-drain outputs

MSTR — Master Mode Select
    0 = Slave mode
    1 = Master mode

CPOL, CPHA — Clock Polarity, Clock Phase
    Refer to **SPI (1 and 2) Transfer Format** figure shown in SPCR1.

SPR22, SPR[1:0] — SPI Clock Rate Selects
(SPR22 is located in OPT2 register, SPR[1:0] are located in SPCR2 register)

SPI 2 Clock Rate Selects

SPR22	SPR1	SPR0	E Clock Divided by	Freqency at E = 4 MHz (Baud Rate)
0	0	0	2	2.0 MHz
0	0	1	4	1.0 MHz
0	1	0	16	250 kHz
0	1	1	32	125 kHz
1	0	0	8	500 kHz
1	0	1	16	250 kHz
1	1	0	64	62.5 kHz
1	1	1	128	31.3 kHz

SPSR1 — Serial Peripheral Status 1 $0029

Bit 7	6	5	4	3	2	1	Bit 0
SPIF	WCOL	—	MODF	—	—	—	—

RESET: 0   0   0   0   0   0   0   0

SPIF — SPI Transfer Complete Flag
This flag is set when an SPI transfer is complete (after eight SCK cycles in a data transfer). Clear this flag by reading SPSR1 (with SPIF = 1), then access SPDR1 (LDSP1 = 0 in OPT2). If the SPI 1 system is linked with the DMA controller (LDSP1 = 1 in OPT2), WCOL has no meaning and SPIF is cleared only by accessing SPDR1.
0 = No SPI 1 transfer complete or SPI 1 transfer still in progress
1 = SPI 1 transfer complete

WCOL — Write Collision Error Flag
This flag is set if the MCU tries to write data into SPDR1 while an SPI 1 data transfer is in progress. Clear this flag by reading SPSR1 (WCOL = 1), then access SPDR1 (LDSP1 = 0 in OPT2). If the SPI 1 system is linked with the DMA controller (LDSP1 = 1 in OPT2), WCOL has no meaning and SPIF is cleared only by accessing SPDR1.
0 = No write collision
1 = Write collision

Bits 5 and [3:0] — Not implemented
Always read zero

MODF — Mode Fault (Mode fault terminates SPI operation)
0 = No mode fault
1 = Mode fault ($\overline{SS}$ is pulled low while MSTR = 1)

Bit 7	6	5	4	3	2	1	Bit 0
SPIF	WCOL	—	MODF	—	—	—	—
RESET: 0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag

This flag is set when an SPI transfer is complete (after eight SCK cycles in a data transfer). Clear this flag by reading SPSR2 (with SPIF = 1), then access SPDR2 data register (LDSP2 = 0 in OPT2). If the SPI 2 system is linked with the DMA controller (LDSP2 = 1 in OPT4), WCOL has no meaning and SPIF is cleared only by accessing SPDR1.

0 = No SPI 2 transfer complete or SPI 2 transfer still in progress
1 = SPI 2 transfer complete

WCOL — Write Collision Error Flag

This flag is set if the MCU tries to write data into SPDR1 while an SPI 1 data transfer is in progress. Clear this flag by reading SPSR1 (WCOL = 1), then access SPDR1 (LDSP1 = 0 in OPT2). If the SPI 1 system is linked with the DMA controller (LDSP1 = 1 in OPT2), WCOL has no meaning and SPIF is cleared only by accessing SPDR1.

0 = No write collision
1 = Write collision

Bits 5 and [3:0] — Not implemented
Always read zero

MODF — Mode Fault (Mode fault terminates SPI operation)
0 = No mode fault
1 = Mode fault ($\overline{SS}$ is pulled low while MSTR = 1)

SPDR1 — SPI Data 1 $002A

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

SPI is double buffered in, single buffered out.

SPDR2 — SPI Data 2 $008A

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

SPI is double buffered in, single buffered out.

Bit 7	6	5	4	3	2	1	Bit 0
SPIM1	CWOM	LDSP1	IRVNE	LSBF1	SPR21	—	FCS1

RESET: 0   0   0   —   0   0   0   0

SPIM1 — SPI Mode Select
   0 = SPI 1 configured for normal operation
   1 = MOSI, MISO, and $\overline{SS}$ pins configured as serial data out (SDO), serial data in (SDI), and chip
      select ($\overline{CS}$) pins. MODF flag in SPSR1 has no meaning.

CWOM — Port C Wired-OR Mode
   Refer to **Parallel Input/Output.**

LDSP1 — Link DMA and SPI 1
   0 = DMA link with SPI 1 active
   1 = DMA link with write buffer of SPDR1 enabled, WCOL flag not used, SPIF flag in SPSR1
      cleared only by the accessing SPDR1.

IRVNE — Internal Read Visibility/Not E
   Refer to **Operating Modes and On-Chip Memory**.

LSBF1 — SPI LSB First Enable
   SPI 1 option
   0 = Data transferred LSB first
   1 = Data transferred MSB first

SPR21 — SPI Clock (SCK) Rate Select
   Adds a divide by four to the SPI 1 clock chain and, with the two bits in SPCR1, specifies the SPI 1
   clock rate. Refer to the table of SPI 1 clock rate selects.

Bit 1 — Not implemented
   Always reads zero

FCS1 — Force $\overline{CS}$ for SPI 1
   0 = $\overline{CS}$ pin state controls SDO and SCK pin. If $\overline{CS}$ is 0, SDO and SCK (if MSTR = 1) become
      output. If $\overline{CS}$ is 1, SDO and SCK become high-impedance input.
   1 = SDO and SCK (if MSTR = 1) pins become output pins regardless of $\overline{CS}$ pin state.

Bit 7	6	5	4	3	2	1	Bit 0
SPIM2	—	LDSP2	—	LSBF2	SPR22	—	FCS2

RESET: 0   0   0   0   0   0   0   0

SPIM2 — SPI Mode Select
    0 = SPI 2 configured for normal operation
    1 = MOSI, MISO, and $\overline{SS}$ pins configured as serial data out (SDO), serial data in (SDI), and chip select ($\overline{CS}$) pins. MODF flag in SPSR2 has no meaning.

Bit 6 — Not Implemented
    Always reads zero

LDSP2 — Link DMA and SPI 2
    0 = DMA link with SPI 2 active
    1 = DMA link with write buffer of SPDR2 enabled, WCOL flag not used, SPIF flag in SPSR2 cleared only by the accessing SPDR2.

Bit 4 — Not Implemented
    Always reads zero

LSBF2 — SPI 2 LSB First Enable
    SPI 2 option
        0 = Data transferred LSB first
        1 = Data transferred MSB first

SPR22 — SPI 2 Clock (SCK) Rate Select
    Adds a divide by four to the SPI 2 clock chain and, with the two bits in SPCR2, specifies the SPI 2 clock rate. Refer to the table of SPI 2 clock rate selects.

Bit 1 — Not implemented
    Always reads zero

FCS2 — Force $\overline{CS}$ for SPI 2
    0 = $\overline{CS}$ pin state controls SDO and SCK pin. If $\overline{CS}$ is 0, SDO and SCK (if MSTR = 1) become output. If $\overline{CS}$ is 1, SDO and SCK become high-impedance input.
    1 = SDO and SCK (if MSTR = 1) pins become output pins regardless of $\overline{CS}$ pin state.

Direct Memory Access Link to SPI

Each SPI system can be linked with the direct memory access controller (DMAC). This allows peripheral devices to transfer data directly into memory using the SPI systems' data registers. The link is enabled using the LDSP1 or LDSP2 bit in the OPT2 or OPT4 register. When the LDSP1 or LDSP2 bit is set to one, the write buffer of the corresponding SPDR is enabled and linked with the DMA system. SPIF is cleared by accessing SPDR. The WCOL flag is not used and has no meaning. Refer to the following table.

SPI Operating Modes

SPIM1 SPIM2	LDSP1 LDSP2	CPHA1 CPHA2	PD2 PG2	PD3 PG3	PD4 PG4	PD5 PG5	MODF1 MODF2	Write Buffer	Accesses to Clear Flag
0	0	X	MISO	MOSI	SCK	$\overline{SS}$	Yes	No	SPSR and SPDR
0	1	1	MISO	MOSI	SCK	$\overline{SS}$	Yes	Yes	SPDR Only
1	0	X	SDI	SDO	SCK	$\overline{CS}$	No	No	SPSR and SPDR
1	1	1	SDI	SDO	SCK	$\overline{CS}$	No	Yes	SPDR Only

Direct Memory Access Controller

The four-channel direct memory access (DMA) controller allows fast data transfer between two blocks of memory, between registers and memory, or between registers. It can also include externally mapped memory in expanded mode. Each byte transfer cycle takes two E clocks and is performed by a read and a write in the same 64 Kbyte address space.

Except for the DMA control registers themselves, any peripheral control register can be accessed in the same way. Selecting one of the two bus arbitration modes, burst or cycle steal, enables the CPU and the DMA controller to share the same data bus.

In burst mode, the DMA controller requests the bus from the CPU, causing the CPU to go into a hold state until the last DMA instruction is completed. In burst mode, the DMA controller can transfer the data at maximum speed. The CPU throughput may be slow, however, or the CPU may not respond to any interrupt request. This may be a consideration if the DMA controller is in possession of the bus for an extended period of time.

Cycle steal mode allows the DMA controller to access the data bus during the clock phases when the CPU is not using the bus. Although the CPU is not disturbed by the DMA controller access, the DMA transfer rate may be comparatively slow.

A hardware timer allows delays to be inserted between transfers. In some cases a delay is necessary when accessing slow peripherals or when using the transferred data in calculations. The delay period of the timer is controlled by values written to TI[2:0] in DMAR register. There are five methods for triggering the start of the interval timer. Setting the FIT bit in DMAR register forces the count to begin. Values written to TRS[1:0] in DMAR allow selection of four additional triggering sources. Refer to the description of DMAR register.

Wrap around mode can be selected for both source and destination addresses. This capability allows multiple-byte transfers either from the source, to the destination, or both. Refer to the description of DMAW register.

Emulation chip mode (84-pin versions only), provides three pins that augment the functionality of the DMA system. DMHALT is an active-low input pin that allows suspension of the current DMA transfer. The BURST pin is an active-high output that indicates the bus cycle while the DMA system is in burst mode. The STEAL pin is an active-high output that indicates the bus cycle when the DMA system is in steal mode. Refer to **Operating Modes and On-Chip Memory** for a description of emulation chip mode.

DMA Control Registers

Each of the four DMA channels has a bank of seven 8-bit control registers. Each bank overlaps the others. There are also three 8-bit control registers that affect the entire DMA system and do not overlap. Refer to the following diagram.
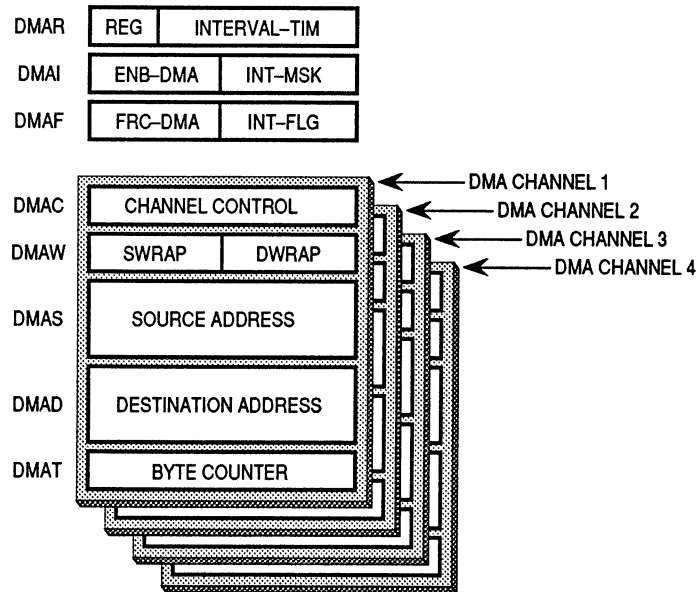
DMA Control Register Organization

	Bit 7	6	5	4	3	2	1	Bit 0
	DR1	DR0	TI2	TI1	TI0	FIT	TRS1	TRS0
RESET:	0	0	0	0	0	0	0	0

DR[1:0] — Channel Select for Overlapping Register Banks

DR1	DR0	Registers
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

TI[2:0] — Timer Interval Value Select

TI2	TI1	TI0	Interval
0	0	0	0 (No interval time)
0	0	1	1/32 x E (8 µs at 4 MHz)
0	1	0	1/64 x E (16 µs at 4 MHz)
0	1	1	1/128 x E (32 µs at 4 MHz)
1	0	0	1/256 x E (64 µs at 4 MHz)
1	0	1	1/512 x E (128 µs at 4 MHz)
1	1	0	1/1024 x E (256 µs at 4 MHz)
1	1	1	1/2048 x E (512 µs at 4 MHz)

If the value selected is changed while the timer is running, the current timeout may be irregular.

FIT — Force Start of Interval Timer Count
A write to this register with bit 2 set forces the interval timer to start.

TRS[1:0] — Request Source Selection for Interval Timer

TRS1	TRS0	Source
0	0	SPI 1 Transmitter Buffer Empty
0	1	SPI 2 Transmitter Buffer Empty
1	0	Real-Time Interrupt
1	1	DMA Channel 3 Transfer Complete

DMAI — DMA Channel Interrupt Enable $00B1

	Bit 7	6	5	4	3	2	1	Bit 0
	DE4	DE3	DE2	DE1	DI4	DI3	DI2	DI1
RESET:	0	0	0	0	0	0	0	0

DE[4:1] — DMA Channel Transfer Enable
    Bits reset upon completion of corresponding channel transfer unless repeat mode is enabled.
        0 = Disables transfer of the corresponding channel
        1 = Enables transfer of the corresponding channel

DI[4:1] — DMA Channel Interrupt on Transfer Complete Enable
    This causes an interrupt at end of last byte transfer cycle only when corresponding channel of DI bit is enabled.
        0 = Disables corresponding channel's transfer complete interrupt
        1 = Enables corresponding channel's transfer complete interrupt

---

DMAF — DMA Interrupt Flag $00B2

	Bit 7	6	5	4	3	2	1	Bit 0
	DT4	DT3	DT2	DT1	DF4	DF3	DF2	DF1
RESET:	0	0	0	0	0	0	0	0

DT[4:1] — DMA Start Trigger
    DMA channels are forced to start a transfer by a write to this register with the corresponding bit set. These bits always read as zero.

DF[4:1] — DMA Interrupt Flag
    The DMA interrupt flag is set at the end of the last byte transfer cycle on the corresponding channel. These flag bits cause an interrupt request only when the corresponding channel of the DI bit in DMAI is enabled. Flag bits are cleared by a write to this register with the corresponding bit set.

DMAC — DMA Channel Control $00B3

	Bit 7	6	5	4	3	2	1	Bit 0
	BST	REP	RQ2	RQ1	RQ0	—	RS1	RS0
RESET:	0	0	0	0	0	0	0	0

BST — Burst Mode Transfer Enable
    Determines which bus arbitration mode is used
        0 = Cycle steal mode used by this DMA channel
        1 = DMA channel uses burst mode

REP — Repeat Mode Enable

Enables repeat, reloading the same counter values as in the initial state after the last count is reached.

0 = Disables repeat mode. Corresponding DE bit in DMAI is reset. Channel stopped after last count.

1 = Enables repeat mode. Corresponding DE bit in DMAI will not reset. Channel ready for next request after the last count

RQ[2:0] — Transfer Bytes Assignment on Each Request

RQ2	RQ1	RQ0	Bytes Transferred
0	0	0	1 byte per request
0	0	1	2 bytes per request
0	1	0	One round of source address wrap around per request. Byte count determined by DMAW register.
0	1	1	Bytes per request determined by DMAT register.
1	1	0	One round of the destination address wrap around per request. Byte count determined by DMAW register.

Bit 2 — Not Implemented

Always reads zero

RS[1:0] — DMA Channel Request Source

Determines source of DMA channel request. Sources of DMA requests differ for each DMA channel.

RS1	RS0	DMA Request Source
CHANNEL 1		
0	0	Receiver Data Available on SPI 1
0	1	Interval Timer Completion
1	0	Real-Time Interrupt
1	1	I4/O5 Interrupt
CHANNEL 2		
0	0	Transmitter Buffer Empty on SPI 1
0	1	Interval Timer Completion
1	0	Channel 1 Completion
1	1	I4/O5 Interrupt
CHANNEL 3		
0	0	Receiver Data Available on SPI 2
0	1	Interval Timer Completion
1	0	Real-Time Interrupt
1	1	ALU Operation Completed
CHANNEL 4		
0	0	Transmitter Buffer Empty on SPI 2
0	1	Interval Timer Completion
1	0	Real-Time Interrupt
1	1	Channel 3 Completion

DMAW — DMA Wrap Around

	Bit 7	6	5	4	3	2	1	Bit 0
	DSW	SW2	SW1	SW0	DDW	DW2	DW1	DW0
RESET:	1	0	0	0	1	0	0	0

DSW — Disable Source Address Wrap Around
   Source address counter reloaded with content of DMAS register when it reaches the last value of the round. When wrap around is enabled, the content of some peripheral control registers or a fixed data block can be transferred several times.
      0 = Enable source address wrap around
      1 = Disable source address wrap around

SW[2:0] — Source Address Wrap Around Byte Count
   Determines number of bytes for one round of source address during wrap around

DSW	SW2	SW1	SW0	Wrap Around Byte Count
1	X	X	X	Disable Wrap Around
0	0	0	0	8 Bytes
0	0	0	1	1 Byte
0	0	1	0	2 Bytes
0	0	1	1	3 Bytes
0	1	0	0	4 Bytes
0	1	0	1	5 Bytes
0	1	1	0	6 Bytes
0	1	1	1	7 Bytes

DDW — Disable Destination Address Wrap Around
      0 = Enable destination address wrap around
      1 = Disable destination address wrap around

DW[2:0] — Destination Address Wrap Around Byte Count
   Determine number of bytes for one round of the destination address when wrap around is performed. During wrap around, destination address counter reloaded with content of DMAD register when it reaches the last value of the round.

DDW	DW2	DW1	DW0	Destination Address Byte Count
1	X	X	X	Disable Wrap Around
0	0	0	0	8 Bytes
0	0	0	1	1 Byte
0	0	1	0	2 Bytes
0	0	1	1	3 Bytes
0	1	0	0	4 Bytes
0	1	0	1	5 Bytes
0	1	1	0	6 Bytes
0	1	1	1	7 Bytes

DMAS — DMA Source Address $00B5, $00B6

Bit 7	6	5	4	3	2	1	Bit 0
A15	A14	A13	A12	A11	A10	A9	A8
A7	A6	A5	A4	A3	A2	A1	A0

DMAS holds the starting source address of the data block being transferred.

DMAD — DMA Destination Address $00B7, $00B8

Bit 7	6	5	4	3	2	1	Bit 0
A15	A14	A13	A12	A11	A10	A9	A8
A7	A6	A5	A4	A3	A2	A1	A0

DMAD holds the starting destination address of the data block being transferred.

DMAT — Transfer Byte Count $00B9

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

RESET: U   U   U   U   U   U   U   U

DMAT contains the number of bytes to be transferred. Maximum number of bytes to be transferred is 256 (indicated by $00) for this 8-bit counter. DMAT indicates current value of the byte counter if it is read while the corresponding channel is enabled. If DMAT is read while the channel is disabled, then it indicates the number of bytes to be transferred when the DMA channel is enabled.

Analog-to-Digital Converter

The analog-to-digital (A/D) converter system uses an all-capacitive charge-redistribution technique to convert analog signals to digital values. The MC68HC11M2 A/D converter system, an 8-channel multiplexed-input, successive-approximation converter, is accurate to ±1 least significant bit (LSB). It does not require external sample and hold circuits because of the type of charge-redistribution technique used.

Dedicated lines V_{RH} and V_{RL} provide the reference supply voltage inputs.

A multiplexer allows the single A/D converter to select one of 16 analog signals.
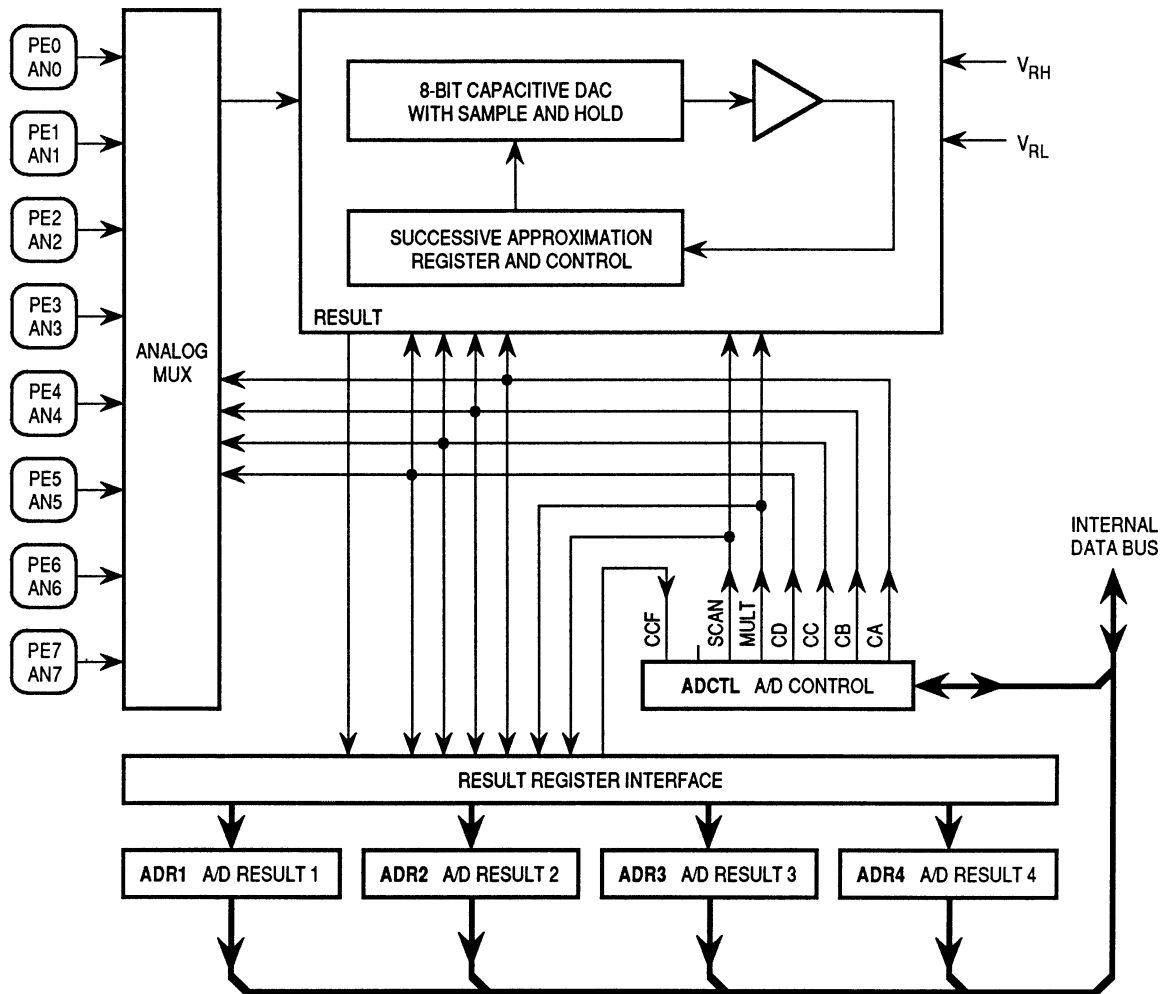
A/D Converter Block Diagram

E CLOCK

WRITE TO ADCTL

12 E CYCLES

SAMPLE ANALOG INPUT

| MSB 4 CYCLES | BIT 6 2 CYC | BIT 5 2 CYC | BIT 4 2 CYC | BIT 3 2 CYC | BIT 2 2 CYC | BIT 1 2 CYC | LSB 2 CYC | 2 CYC END |

SUCCESSIVE APPROXIMATION SEQUENCE

SET CCF FLAG

REPEAT SEQUENCE IF SCAN = 1

CONVERT FIRST CHANNEL AND UPDATE ADR1

CONVERT SECOND CHANNEL AND UPDATE ADR2

CONVERT THIRD CHANNEL AND UPDATE ADR3

CONVERT FOURTH CHANNEL AND UPDATE ADR4

0   32   64   96   128   E CYCLES

A/D CONVERSION TIM

Timing Diagram for a Sequence of Four A/D Conversions

INPUT PROTECTION DEVICE

DIFFUSION AND POLY COUPLER

ANALOG INPUT PIN

< 2pF

+ ~20V
− ~0.7V

≤ 4 KΩ

400 nA JUNCTION LEAKAGE

*

~20 pF   DAC CAPACITANCE

V_{RL}
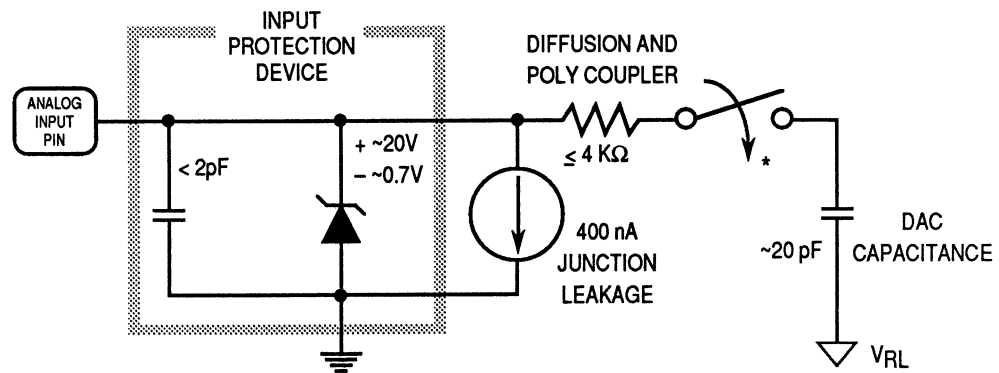
*THIS ANALOG SWITCH IS CLOSED ONLY DURING THE 12-CYCLE SAMPLE TIME.

ANALOG INPUT PIN

Electrical Model of an Analog Input Pin (Sample Mode)

Bit 7	6	5	4	3	2	1	Bit 0
CCF	—	SCAN	MULT	CD	CC	CB	CA
RESET: U	0	U	U	U	U	U	U

CCF — Conversions Complete Flag
    CCF is set after an A/D conversion cycle and cleared when ADCTL is written.

Bit 6 — Not implemented
    Always reads zero

SCAN — Continuous Scan Control
    0 = Do four conversions and stop
    1 = Convert four channels in selected group continuously

MULT — Multiple Channel/Single Channel Control
    0 = Convert single channel selected
    1 = Convert four channels in selected group

CD–CA — Channel Select D through A

A/D Converter Channel Assignments

Channel Select Control Bits				Channel Signal	Result in ADRx if MULT = 1	Result in ADRx if MULT = 0
CD	CC	CB	CA			
0	0	0	0	AD0	ADR1	ADR[4:1]
0	0	0	1	AD1	ADR2	ADR[4:1]
0	0	1	0	AD2	ADR3	ADR[4:1]
0	0	1	1	AD3	ADR4	ADR[4:1]
0	1	0	0	AD4	ADR1	ADR[4:1]
0	1	0	1	AD5	ADR2	ADR[4:1]
0	1	1	0	AD6	ADR3	ADR[4:1]
0	1	1	1	AD7	ADR4	ADR[4:1]
1	0	X	X	Reserved		
1	1	0	0	V_{RH}	ADR1	ADR[4:1]
1	0	1		V_{RL}	ADR2	ADR[4:1]
1	1	0	0	$(V_{RH})/2$	ADR3	ADR[4:1]
1	1	0	1	Test/Reserved*	ADR4	ADR[4:1]

*Used for factory testing

ADR[4:1] — A/D Results   **$0031–$0034**

$0031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$0032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$0033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$0034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4

Analog Input to 8-Bit Result Translation Table

	Bit 7	6	5	4	3	2	1	Bit 0
% [1]	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
Volts [2]	2.500	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195

[1] % of $V_{RH}–V_{RL}$ [2] Volts for $V_{RL} = 0$; $V_{RH} = 5.0$ V

OPTION — System Configuration Options   **$0039**

Bit 7	6	5	4	3	2	1	Bit 0
ADPU	CSEL	IRQE*	DLY*	CME	FCME*	CR1*	CR0*

RESET: 0   0   0   1   0   0   0   0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

ADPU — A/D Converter Power-Up
    0 = A/D converter powered down
    1 = A/D converter powered up

CSEL — Clock Select
    0 = A/D and ROM/EPROM use system E clock
    1 = A/D and ROM/EPROM use internal RC clock

IRQE — IRQ Select Edge Sensitive Only
    Refer to **Resets and Interrupts**.

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
    Refer to **Resets and Interrupts**.

CME — Clock Monitor Enable
    Refer to **Resets and Interrupts**.

FCME — Force Clock Monitor Enable
    Refer to **Resets and Interrupts**.

CR[1:0] — COP Timer Rate Select
    Refer to **Main Timer**.

Math Coprocessor

The arithmetic logic unit available on the MC68HC11M2 computes integer multiplication and division as a coprocessor. Because the arithmetic operations are executed independently, the CPU is free to perform other operations. The five registers of the coprocessor are mapped in the peripheral register area and can be read from or written to by the CPU. Refer to the following diagram for the coprocessor structure.
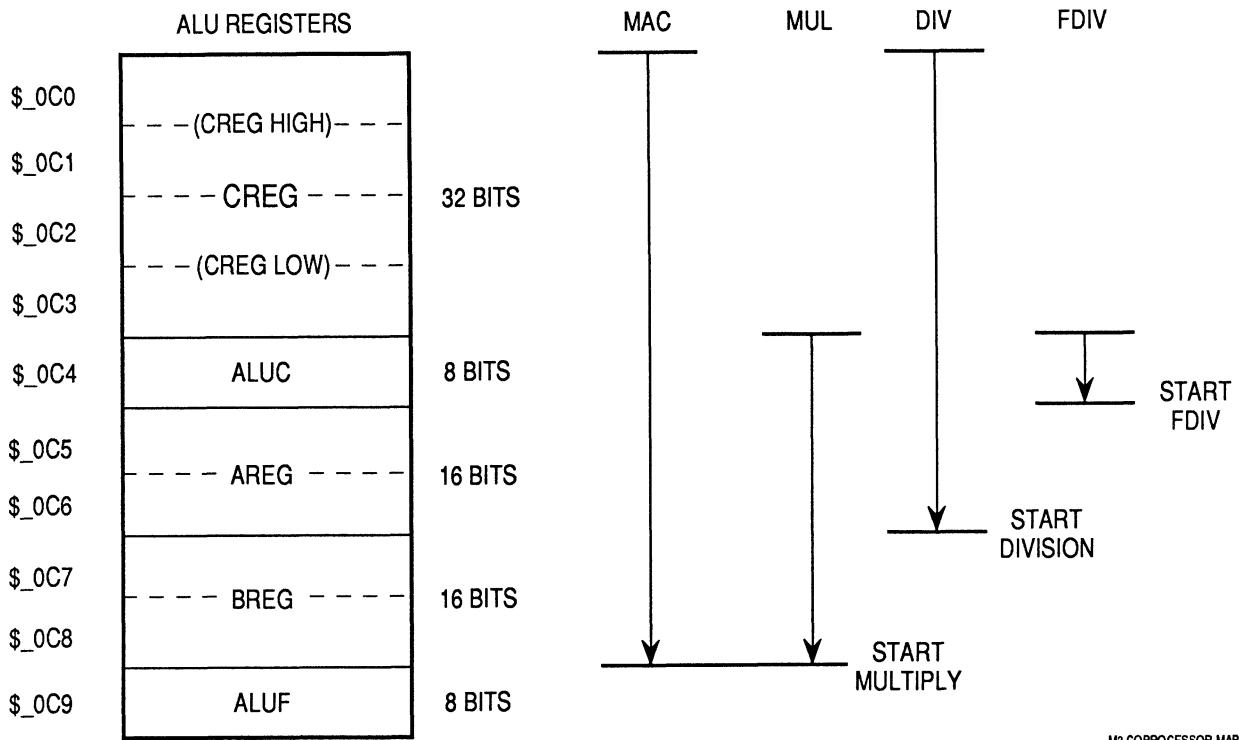
M2 COPROCESSOR MAP

Math Coprocessor Map

The following data registers hold the value of signed or unsigned integer with an implied fixed radix point at the right of bit 0. The 16-bit AREG register holds the value of the multiplicand or the divisor. The 16-bit BREG register holds the value of the multiplier or the remainder after the division. CREG, considered two 16-bit registers (CREG High and CREG Low), holds the value of the product or accumulated product after the multiplication, or the numerator before division and the quotient after division.

In the case of fractional division, the fractional number in CREG Low does not include the sign bit. The quotient is placed in CREG Low and the remainder is placed in BREG. The previous contents of CREG Low are moved into CREG High after the fractional division. Refer to the Coprocessor Register Formats Diagram. The signed data that is used for both inputs or outputs is two's complement binary integer format.

Control of the coprocessor is provided by the ALUC register. The ALUF register indicates the status of the operation just performed.

Refer to the Coprocessor Register Formats Diagram on the following page for a more detailed description of the ALU registers and their associated data formats.

32-BIT SIGNED INTEGER NUMBER

31	16,15	0
S	CREG HIGH	CREG LOW

↑ SIGN BIT

—————— INTEGER ——————

↑ RADIX POINT

-2147483648
TO
+2147483647

CREG

16-BIT SIGNED INTEGER NUMBER

15	0
S	INTEGER

↑ SIGN BIT   ↑ RADIX POINT

-32768
TO
32767

AREG or BREG
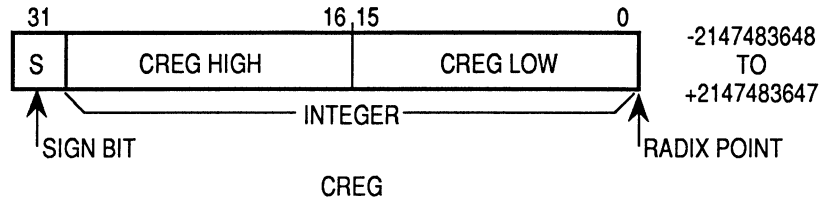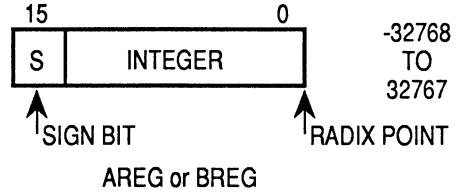
16-BIT FRACTION NUMBER AFTER FDIV

-1	-16
FRACTION	

CREG LOW

↑ ↑ RADIX POINT

SIGN BIT IS IN INTEGER PART OR NEG FLAG

0.00000
TO
0.99998
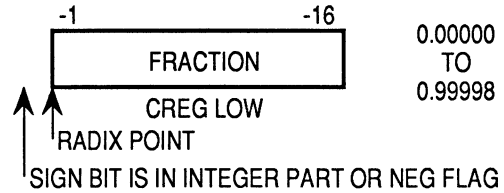
32-BIT SIGNED INTEGER AND FRACTION FOLLOWING AN FDIV

15	0	-1	-16
S	INTEGER	FRACTION	

↑ SIGN BIT   CREG HIGH   ↑ RADIX POINT   CREG LOW

-32768.99998
TO
+32767.99998

CREG
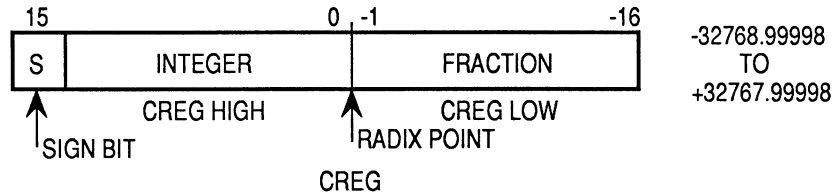
LONG WORD SIGNED RESULT AFTER FDIV FOLLOWING AN IDIV

31	16,15	0
S	CREG HIGH AFTER IDIV	CREG LOW AFTER IDIV

↑ SIGN BIT

—————— INTEGER ——————

↑ RADIX POINT

CREG

15	0	-1	-16
S	CREG HIGH AFTER FDIV	CREG LOW AFTER FDIV	

↑ SIGN BIT   —— INTEGER ——   ↑ RADIX POINT   —— FRACTION ——

CREG
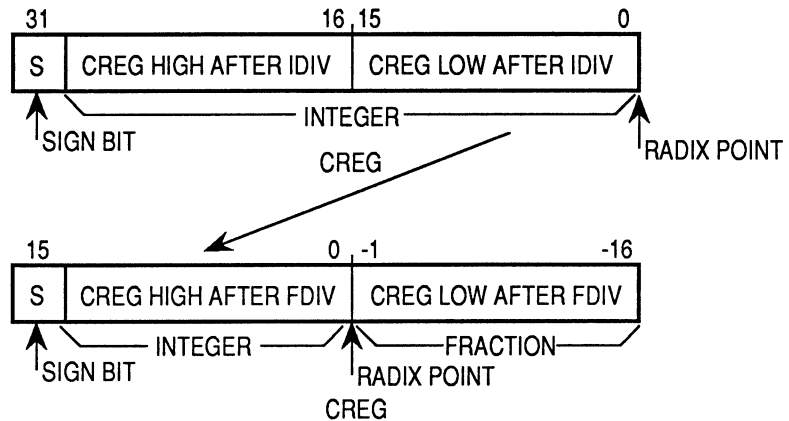
COPROCESSOR
REG FORMAT

Coprocessor Register Formats

The ALU performs 16-bit integer multiplication and division and signed or unsigned multiplication, with or without accumulated product, as well as signed or unsigned division. Below are the times in which the ALU performs its functions.

Signed or unsigned Multiplication without accumulated product:

AREG • BREG → CREG (product)
20 E clock cycles (5 µs at 4 MHz)

Signed or unsigned Multiplication with accumulated product:

AREG • BREG + CREG → CREG
20 E clock cycles (5 µs at 4 MHz)

Signed or unsigned division:

CREG ÷ AREG → CREG (quotient), BREG (remainder)
Unsigned — 33 E clock cycles (8.25 µs at 4 MHz)
Signed — 35 E clock cycles (8.75 µs at 4 MHz)

Signed or unsigned fractional division:

CREG (CREG Low) → CREG (CREG High)
BREG ÷ AREG → CREG (CREG Low) (fractional quotient), BREG (remainder)
Unsigned — 17 E clock cycles (4.25 µs at 4 MHz)
Signed — 18 E clock cycles (4.5 µs at 4 MHz)

CREG — CREG Data   **$00C0–$00C3**

$00C0	Bit 31	30	29	28	27	26	25	Bit 24	CREG (High)
$00C1	Bit 23	22	21	20	19	18	17	Bit 16	CREG (High)
$00C2	Bit 15	14	13	12	11	10	9	Bit 8	CREG (Low)
$00C3	Bit 7	6	5	4	3	2	1	Bit 0	CREG (Low)

ALUC — Arithmetic Logic Unit Control   **$00C4**

	Bit 7	6	5	4	3	2	1	Bit 0
	SIG	DIV	MAC	DCC	TRG	OVE	DZE	ACE
RESET:	0	0	0	1	0	0	0	0

SIG — Signed Number Enable
0 = AREG, BREG, and CREG contents are unsigned numbers.
1 = AREG, BREG, and CREG contents are signed numbers.

DIV — Division Enable
0 = DIV disabled
1 = DIV enabled

MAC — Multiply with Accumulated Product Enable
    During a MAC operation, the accumulated product is held in CREG and is added to subsequent multiplications.
        0 = MAC disabled
        1 = MAC enabled

DCC — Division Compensation for Concatenated Quotient Enable
    For signed IDIV and signed FDIV, causes CREG to contain both integer result plus fractional amount to right of radix point. Radix point is to the left of bit 15 in CREG.
        0 = DCC disabled
        1 = DCC enabled

DIV	MAC	DCC	Function	Start Triggers
0	0	X	MUL	Write BREG or set TRG
0	0	X	MUL	Write BREG or set TRG
0	1	X	MAC	Write BREG or set TRG
0	1	X	MAC	Write BREG or set TRG
1	0	X	DIV	Write AREG or set TRG
1	0	0	DIV	Write AREG or set TRG
1	0	1	DIV DCC	Write AREG or set TRG
1	1	X	FDIV	Set TRG
1	1	0	FDIV	Set TRG
1	1	1	FDIV DCC	Set TRG

TRG — Function Start Trigger Bit
    This bit works only for divide operations.
        0 = No effect, this bit always reads zero.
        1 = Writing this bit to one starts the function.

OVE — Overflow Interrupt
        0 = Interrupt disabled
        1 = Interrupt enabled

DZE — Divide Interrupt
        0 = Interrupt disabled
        1 = Interrupt enabled

ACE — Arithmetic Operation Completion Interrupt
        0 = Interrupt disabled
        1 = Interrupt enabled

AREG — AREG Data $00C5–$00C6

	Bit 7	6	5	4	3	2	1	Bit 0	
$00C5	Bit 15	14	13	12	11	10	9	Bit 8	AREG (High)
$00C6	Bit 7	6	5	4	3	2	1	Bit 0	AREG (Low)

BREG — BREG Data $00C7–$00C8

	Bit 7	6	5	4	3	2	1	Bit 0	
$00C7	Bit 15	14	13	12	11	10	9	Bit 8	BREG (High)
$00C8	Bit 7	6	5	4	3	2	1	Bit 0	BREG (Low)

ALUF — Arithmetic Logic Unit Status Flag $00C9

	Bit 7	6	5	4	3	2	1	Bit 0
	NEG	RZF	—	—	—	OVF	DZF	ACF
RESET:	0	0	0	1	0	0	0	0

NEG — Negative Result
Read only bit. Writes to this bit do not affect the value. Valid until next write to AREG or until start of next arithmetic operation.
0 = Result is positive value
1 = Result is negative value

RZF — Remainder Zero
Read only bit. Writes to this bit do not affect the value. Valid until next write to AREG or until start of next arithmetic operation.
0 = Remainder in BREG after FDIV or IDIV is not zero
1 = Remainder in BREG after FDIV or IDIV is zero

Bits [5:3] — Not implemented
Always read zero

OVF — Overflow Flag
Cleared automatically by write to this register if bit 2 is set.
0 = Overflow from MSB on CREG not detected
1 = Overflow from MSB on CREG detected

DZF — Divide by Zero Flag
Cleared automatically by a write to this register with bit 1 set.
0 = Divide by zero condition not detected
1 = Divide by zero condition detected

ACF — Arithmetic Completion Flag
Cleared automatically by write to this register with bit 0 set.
0 = Arithmetic operation not completed
1 = Arithmetic operation completed

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MC68HC11M2TS/D