XA9500XL High-Performance CPLD Automotive XA Product Family

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Preliminary Product Specification

Features

- AEC-Q100 device qualification and full PPAP support available in both extended temperature Q-grade and I-grade.
- Guaranteed to meet full electrical specifications over T_A = –40°C to +125°C
- System frequency up to 100 MHz (10 ns)
- Available in small footprint packages
- Optimized for high-performance 3.3V systems
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals — ideal for multi-voltage system interfacing and level shifting
  - Technology: 0.35µm CMOS process
- Advanced system features
  - In-system programmable enabling higher system reliability through reduced handling and reducing production programming times
  - Superior pin-locking and routability with FastCONNECT™ **II** switch matrix allowing for multiple design iterations without board re-spins
  - Input hysteresis on all user and boundary-scan pin inputs to reduce noise on input signals
  - Bus-hold circuitry on all user pin inputs which reduces cost associated with pull-up resistors and reduces bus loading
  - Full IEEE Standard 1149.1 boundary-scan (JTAG) for in-system device testing
    - Fast concurrent programming
- Slew rate control on individual outputs for reducing EMI generation
- Refer to XC9500XL Family data sheet (DS054) for architecture description
- Refer to XC9536XL data sheet (DS058) and XC9572XL data sheet (DS057) for pin tables
- Additionally, Xilinx and all of our production partners are qualified to QS-9000, moving to TS16949 in 2005.

Description

The XA9500XL 3.3V CPLD Automotive XA product family is targeted for leading-edge, high-performance automotive applications that require either automotive industrial (–40°C to +85°C ambient) or extended (–40°C to +125°C ambient) temperature reconfigurable devices.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in the XA9500XL device can be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

$$I_{CC}\ (mA) = MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$$

where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Table 1: **XA9500XL Device Family**

Device	Macrocells	Usable Gates	Registers	f_{SYSTEM} (MHz)
XA9536XL	36	800	36	100
XA9572XL	72	1,600	72	100
XA95144XL	144	3,200	144	100

Table 2: **XA9500XL Packages and User I/O Pins (not including four dedicated JTAG pins)**

Device	VQ44	TQ144
XA9536XL	34	--
XA9572XL	34	--
XA95144XL	--	117

Absolute Maximum Ratings(1)

Symbol	Description	Min.	Max.	Units
V_{CC}	Supply voltage relative to GND	–0.5	4.0	V
V_{IN}	Input voltage relative to GND(2)	–0.5	5.5	V
V_{TS}	Voltage applied to 3-state output(2)	–0.5	5.5	V
T_{STG}	Storage temperature (ambient)	–65	+150	ºC
T_J	Junction temperature	-	+150	ºC

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
3. For soldering guidelines, see the Package Infomation on the Xilinx website.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
T_A	Ambient temperature	–40	+125	°C
V_{CCINT}	Supply voltage for internal logic and input buffers	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers for 3.3V operation	3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation	2.3	2.7	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	5.5	V
V_O	Output voltage	0	V_{CCIO}	V

Quality and Reliability Characteristics

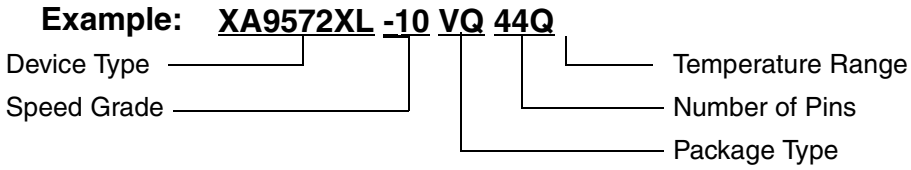
Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance) @ T_A = 70°C	10,000	-	Cycles

Component Availability

Pins		44	144
Type		Plastic VQFP	Plastic TQFP
Code		VQ44	TQ144
XA9536XL	-10	I,Q	--
XA9572XL	-10	I,Q	--
XA95144XL	-10	--	I

Notes:
1. Q = Automotive Extended Temperature (T_A = –40°C to +125°C).
2. I= Automotive Industrial Temperature (T_A = –40°C to +85°C).

Ordering Information



Device Ordering Options

Device	Speed		Package		Temperature	
XA9536XL	-10	10 ns pin-to-pin delay	VQ44	44-pin Quad Flat Pack (VQFP)	Q = Automotive Extended	T_A = –40°C to +125°C
XA9572XL			TQ144	144-pin Thin Quad Flat Pack (TQFP)	I = Automotive Industrial	T_A = –40°C to +85°C
XA95144 XL						

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/17/02	1.0	Initial Xilinx release.
07/17/02	1.1	Updated NPE Quality and Reliability specification.
02/03/03	1.2	Added reference to XC9500XL, XC9536XL, and XC9572XL data sheets.
05/21/04	1.3	Updated the VQ44 column of Table 2 and the Component Availability table on page 2.
10/18/04	1.4	Extensive edits to update family from IQ to XA