Before beginning any new design with this device, please contact Cirrus Logic, Inc., for the latest errata information. See the back cover of this document for sales office locations and phone numbers.

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Supply voltage (V_{CC}) ..... +7.0 V (volts)
Input voltages, with respect to ground ..... –0.5 V to V_{CC} +0.5 V
Operating temperature (T_A) ..... 0°C to 70°C
Storage temperature ..... –65°C to 150°C
Power dissipation ..... 0.25 W (watt)

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the recommended operating conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 Recommended Operating Conditions

Supply voltage (V_{CC}) ..... 5 V ± 5%
Operating free air ambient temperature ..... 0°C < T_A < 70°C
System clock ..... 25 MHz

6.3 DC Characteristics

(@ V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	MIN	MAX	Units	Test Conditions
V_{IL}	Input low voltage	–0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC}	V	(see Note 1)
V_{OL}	Output low voltage		0.4	V	I_{OL} = 2.4 mA (see Note 2)
V_{OH}	Output high voltage	2.4		V	I_{OH} = –400 µA
I_{IL}	Input leakage current	–10	10	µA	0 < V_{IN} < V_{CC}
I_{LL}	Data bus tristate leakage current	–10	10	µA	0 < V_{OUT} < V_{CC}
I_{OC}	Open-drain output leakage current	–10	10	µA	0 < V_{OUT} < V_{CC}
I_{CC}	Power supply current		50	mA	CLK = 25 MHz
C_{IN}	Input capacitance		10	pF	
C_{OUT}	Output capacitance		10	pF	

The signals specific to the parallel port meet all requirements of the IEEE STD 1284 specification except for input signal protection (–2.0 to + 7.0 V); external circuitry is required to meet this specification:

- Symmetrical input/output drive: ±12 mA
- Controlled voltage slew rate: 0.4 V/µs
- Input hysteresis: 0.8 V

NOTES:

1) V_{IH} is 2.7 V minimum on RESET* and CLK.
2) V_{OL} for open drain signals is 0.5 V @ 10 mA sinking.
3) While the CL-CD1283 is a highly dependable device, there are a few guidelines which will help to ensure that the maximum possible level of overall system reliability is achieved. First, the PC board should be designed to provide maximum isolation of noise. A four-layer board is preferable, but a two-layer board will work if proper power and ground distribution is implemented. In either case, decoupling capacitors mounted close to the CL-CD1283 are strongly recommended. Noise typically occurs when either the CL-CD1283's data bus drivers come out of tristate to drive the bus during a read, or when an external bus buffer turns on during a write cycle. This noise, a rapid rate-of-change of supply current, causes 'ground bounce' in the power-distribution traces. This ground bounce, a rise in the voltage of the ground pins, effectively raises the input logic thresholds of all devices in the vicinity, resulting in the possibility of a '1' being interpreted as a '0.'

   To reduce the possibility of ground-bounce affecting the operation of the CL-CD1283, we have specified the input-high voltage (V_{IH}) of the CLOCK and RESET pins is specified at 2.7 V, instead of the TTL-standard 2.0 V. This eliminates any sensitivity to ground bounce, even in very noisy systems.

   Although 2.7 V is higher than the industry-standard 2.4-V output (V_{OH}) specified for TTL, there are several simple ways to meet this specification. One choice is to use any of the available advanced-CMOS logic families (FACT, ACL, etc.). These CMOS output buffers will pull-up close to V_{CC} when not heavily loaded. In addition, AS and ALS TTL may be used if the output of the TTL device is only driving one or two CMOS loads. As noted in the Texas Instruments *ALS/AS Logic Data Book* (1986), pages 4-18 and 4-19, the V_{OH} output of these families exceeds 3.0 V at low current loading. Other manufacturers publish similar data. Cirrus Logic recommends the use of one of these two options for the CLK input, to ensure fast, clean edges. Note that the RESET pin may, if desired, be pulled up passively with a 1-kΩ (or less) resistor.

6.4 AC Characteristics

6.4.1 Asynchronous Timing

Refer to the Figures 6-1 through 6-7 for the reference numbers in the following table.

(@ V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)

Ref. #	Figure	Parameter	MIN	MAX	Unit
t_1	6-1	RESET* low pulse width	10		T_{CLK}
t_2	6-3	Address setup time to CS* or DS*		–20	ns
t_3	6-3	R/W* setup time to CS* or DS*		–10	ns
t_4	6-3	Address hold time after CS*	0		ns
t_5	6-3	R/W* hold time after CS*	0		ns
t_6	6-3	DTACK* low to read data valid		10	ns
t_7	6-3	DTACK* low from CS* or DS[2]	2 T_{CLK}	4 T_{CLK} + 40	ns
t_8	6-3	Data Bus tristate after CS* or DS* high	0	30	ns
t_9	6-3	CS* or DGRANT* high from DTACK* low	0		ns
t_{10}	6-3	DTACK* inactive from CS* or DGRANT* and DS* high		40	ns
t_{11}	6-3	DS* high pulse width	10		ns
t_{12}	6-4	Write data valid from CS* and DS* low		1T_{CLK}	ns
t_{13}	6-4	Write data hold time after DS* high	0		ns
t_{14}	6-2	Clock period (T_{CLK})[1, 3]	40.0	1000	ns
t_{15}	6-2	Clock low time[1]	0.3 T_{CLK}	0.7 T_{CLK}	ns
t_{16}	6-2	Clock high time[1]	0.3 T_{CLK}	0.7 T_{CLK}	ns
t_{17}	6-5	Setup time, SVCACK* to DS* and DGRANT*	10		ns
t_{18}	6-6	Setup time, DMAACK* to rising edge of CLK	10		ns
t_{19}	6-6	Hold time, read data after rising edge of DMAACK	20		ns
t_{20}	6-7	Setup time, write data to rising edge of CLK		–10	ns
t_{21}	6-3	DTACK* active pull-up time[4]			

NOTES:

1) Timing numbers for RESET* and CLK in this table are valid for both asynchronous and synchronous specifications. The device will operate on any clock with a 40–60 duty cycle or better.

2) On host-I/O cycles immediately following SVCACK* cycles and writes to EOSRR, DTACK* will be delayed by 20 CLKs (1 µs @ 20 MHz, 800 ns @ 25 MHz). On systems that do not use DTACK* to signal the end of the I/O cycle, wait states or some other form of delay generation must be used to assure that the CL-CD1283 will not be accessed until after this time period.

3) As T_{CLK} increases, device performance decreases. A minimum clock frequency of 25 MHz is required to guarantee performance as specified. The recommended maximum TCLK is 1000 ns.

4) DTACK* sources current (drives 'high') until the voltage on the DTACK* line is approximately 1.5 V; then DTACK* goes to the 'open-drain' (high-impedance) state.

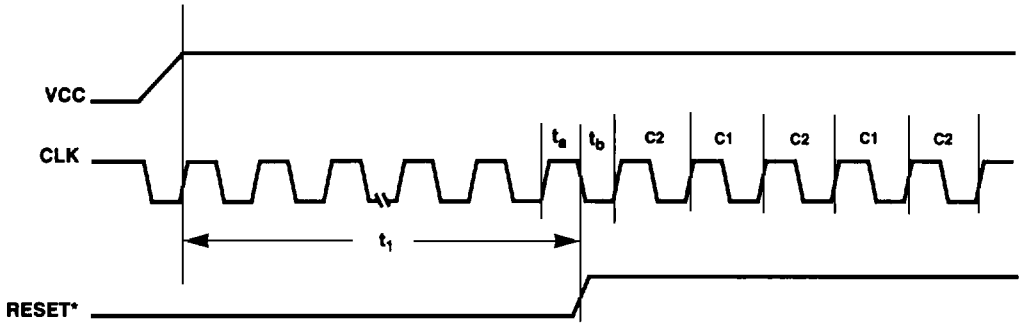


Figure 6-1. Reset Timing

NOTE: For synchronous systems, it is necessary to determine the clock cycle number so that interface circuitry can stay in lock-step with the device. CLK numbers can be determined if RESET* is released within the range $t_a - t_b$; t_a is defined as 10 ns, minimum, after the rising edge of the clock; t_b is defined as 5 ns, minimum, before the next rising edge of the clock. If these conditions are met, the cycle starting after the second rising edge will be C1. See the synchronous timing diagrams for additional information. Clock numbers are not important in asynchronous systems.

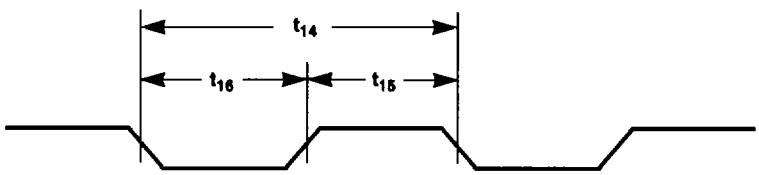


Figure 6-2. Clock Timing

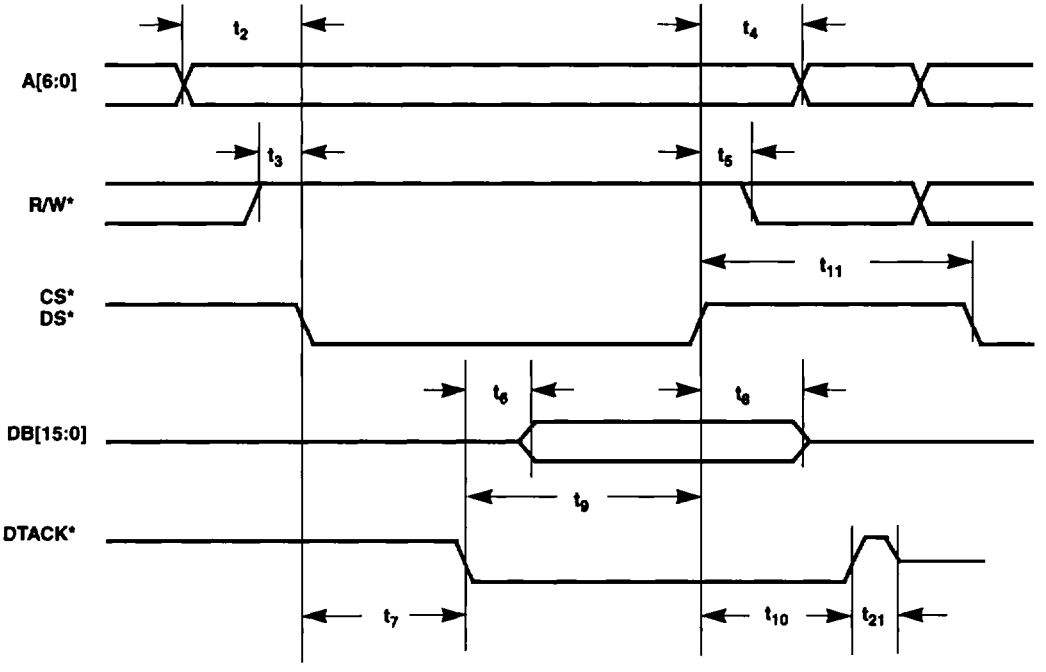


Figure 6-3. Asynchronous Read Cycle Timing

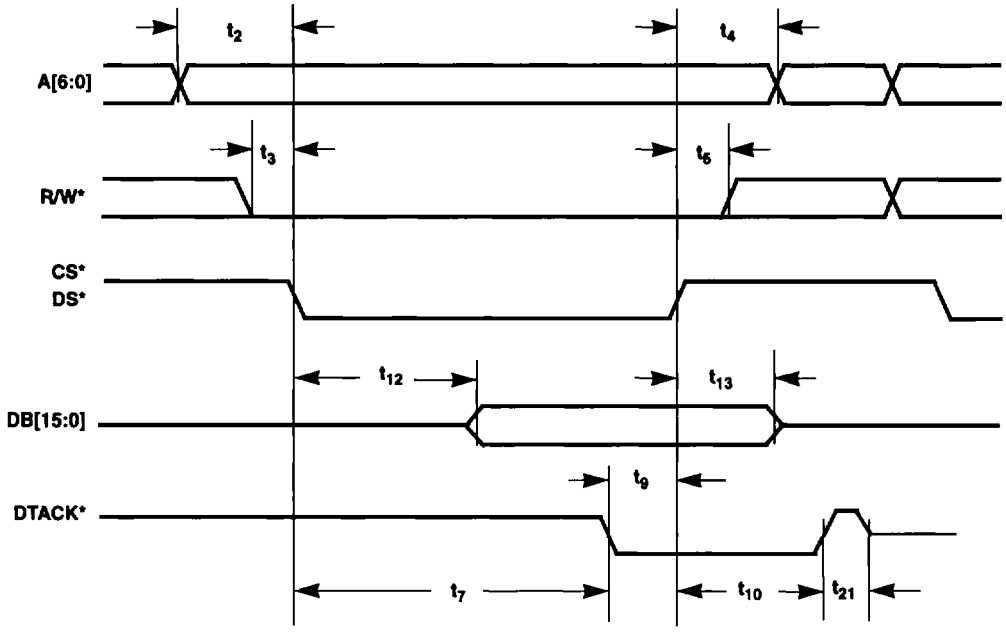


Figure 6-4. Asynchronous Write Cycle Timing

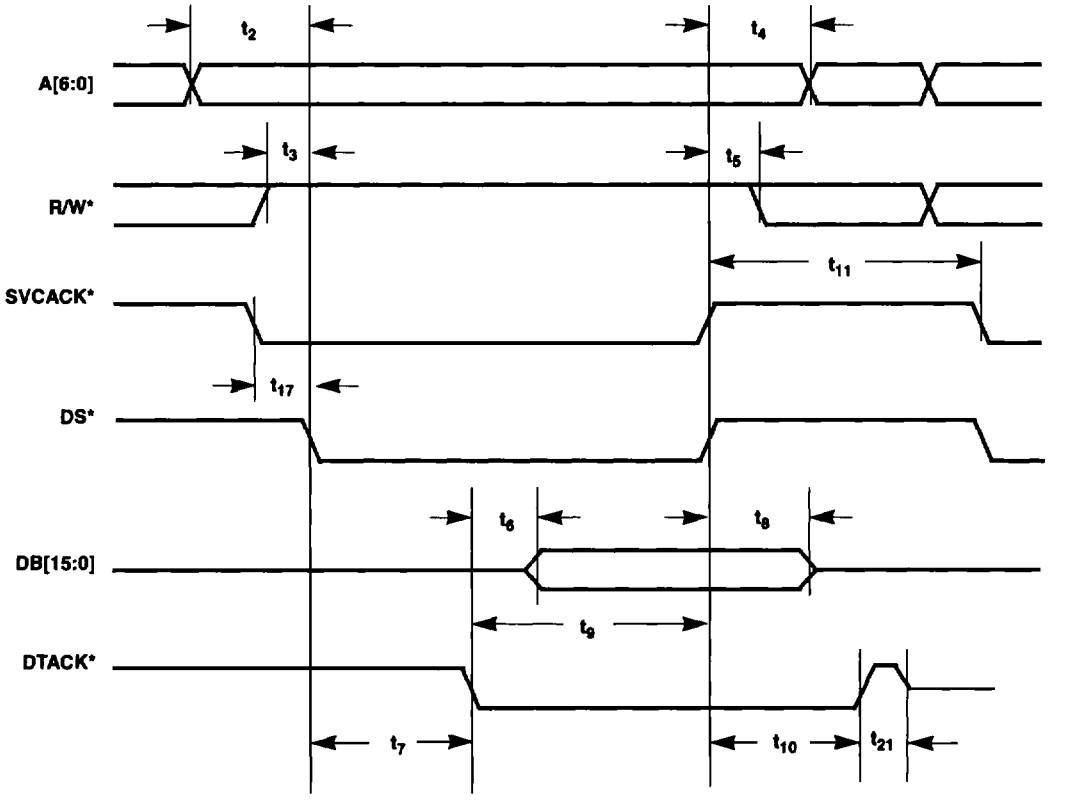
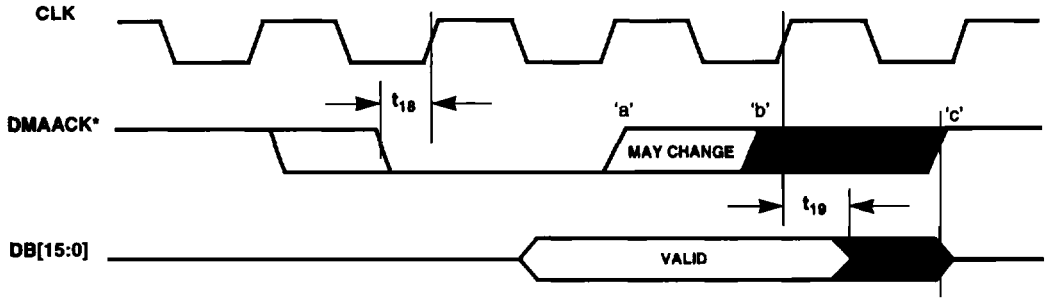


Figure 6-5. Asynchronous Service Acknowledge Cycle Timing



NOTES:

1) The DMA handshake operates in asynchronous mode only if the AsyncDMA bit is set in PACR.
2) If DMAACK* is released after point 'a,' but before point 'b' (before the rising edge of the third full CLK cycle), DB[15:0] will be released at t_{HX} following the rising edge of CLK. If DMAACK* is held past this edge, it controls the release of DB[15:0]; the data bus will remain active until DMAACK* becomes inactive (point 'c').

Figure 6-6. Asynchronous DMA Read Cycle Timing

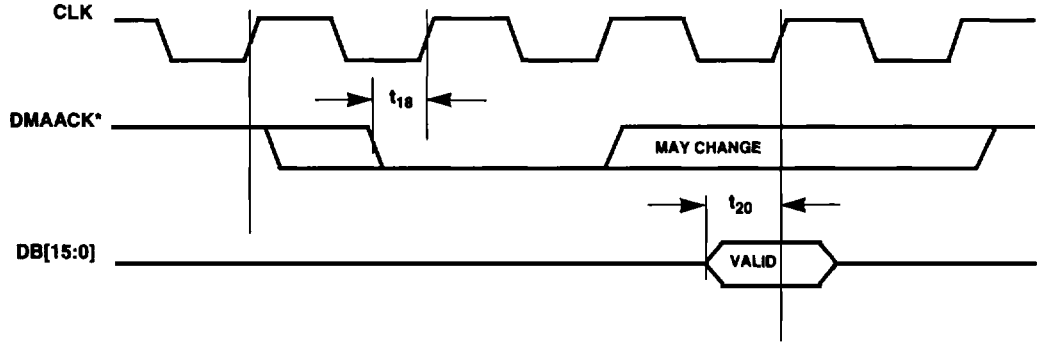


Figure 6-7. Asynchronous DMA Write Cycle Timing

6.4.2 Synchronous Timing

Use the following table as a reference to timing parameters of figures in this section.

Ref. #	Figure	Parameter	MIN	MAX	Unit
t_1	6-8	Setup time, CS* and DS* to C1 rising edge	15		ns
t_2	6-8	Setup time, R/W* to C1 rising edge	15		ns
t_3	6-8	Setup time, address valid to C1 rising edge	20		ns
t_4	6-8	C3 rising edge to data valid		60	ns
t_5	6-8	DTACK* low from C3 rising edge		30	ns
t_6	6-8	CS* and DS* trailing edge to data bus high-impedance		30	ns
t_7	6-8	CS* and DS* inactive between host accesses	10		ns
t_8	6-8	Hold time, R/W* after C3 rising edge	20		ns
t_9	6-8	Hold time, address valid after C3 rising edge	0		ns
t_{10}	6-9	Setup time, write data valid to C3 rising edge	0		ns
t_{11}	6-10	Setup time, DS* and DGRANT* to C1 rising edge	20		ns
t_{12}	6-10	Setup time, SVCACK* to DS* and DGRANT*	10		ns
t_{13}	6-9	Hold time, write data valid after C3 rising edge	0		ns
t_{14}	6-11	Rising edge CLK to falling edge DMAREQ*		20	ns
t_{15}	6-11	Hold time, DMAREQ* after DMAACK* falling edge, last DMA cycle	15		ns
t_{16}	6-12	Setup time, write data to rising edge C3		–10	ns
t_{17}	6-12	Setup time, falling edge DMAACK* to C1 falling edge	10		
t_{18}	6-12	Data valid before falling edge of C2 (read cycle)		20	
t_{19}	6-12	Data hold time, after rising edge DMAACK*		20	
t_{20}	6-8	DTACK* active pull-up time (see Note 2)			

NOTES:

1) On host I/O cycles immediately following SVCACK* cycles and writes to EOSRR, DTACK* will be delayed by 20 CLKs (1 µs @ 20 MHz, 800 ns @ 25 MHz). On systems that do not use DTACK* to signal the end of the I/O cycle, wait states or some other form of delay generation must be used to assure that the CL-CD1283 will not be accessed until after this time period.

2) DTACK* sources current (drives 'high') until the voltage on the DTACK* line is approximately 1.5 V; then DTACK* enters the 'open-drain' (high-impedance) state.

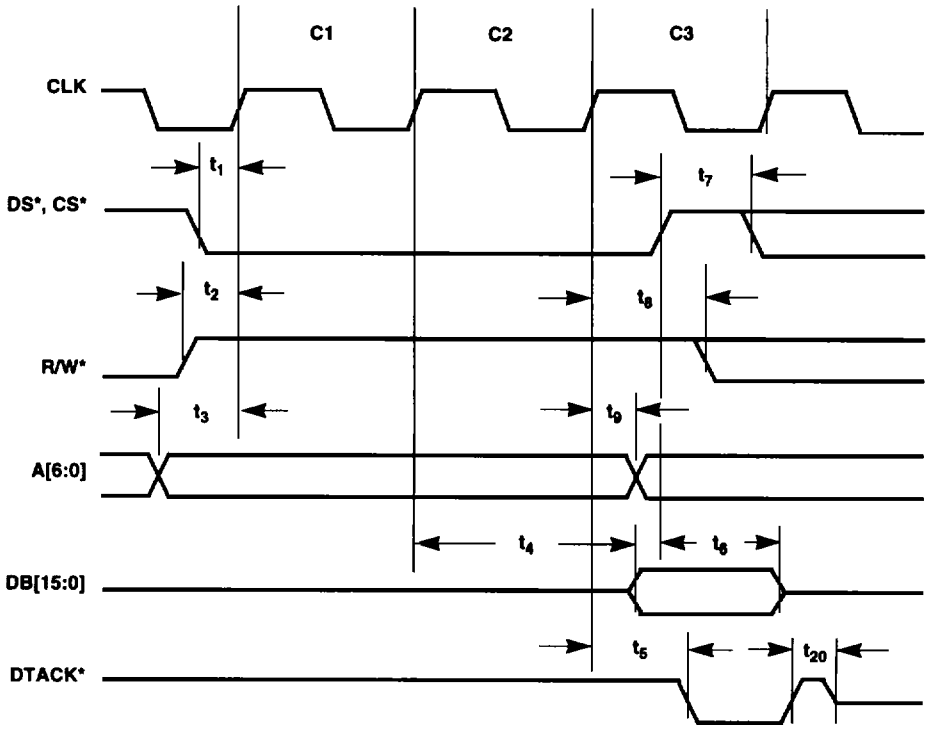


Figure 6-8. Synchronous Read Cycle Timing

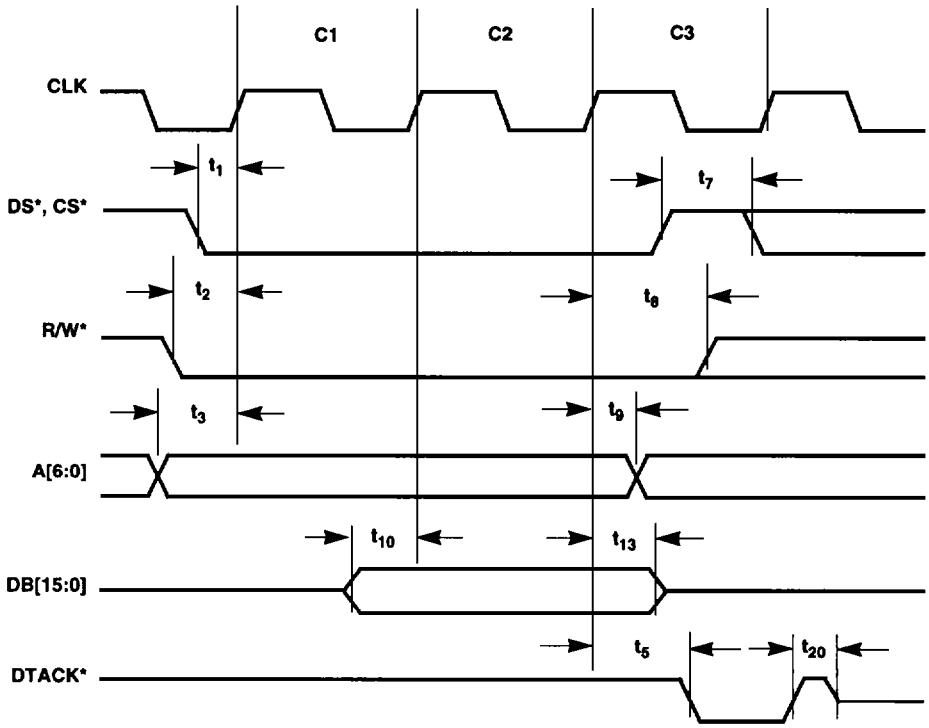


Figure 6-9. Synchronous Write Cycle Timing

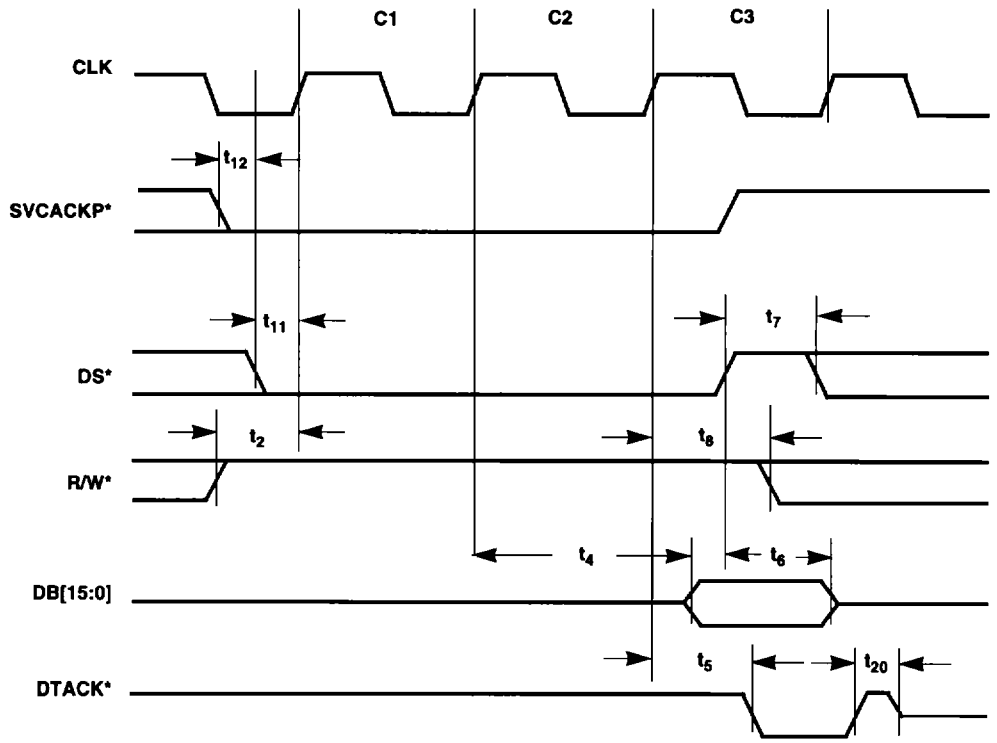


Figure 6-10. Synchronous Service Acknowledge Cycle Timing

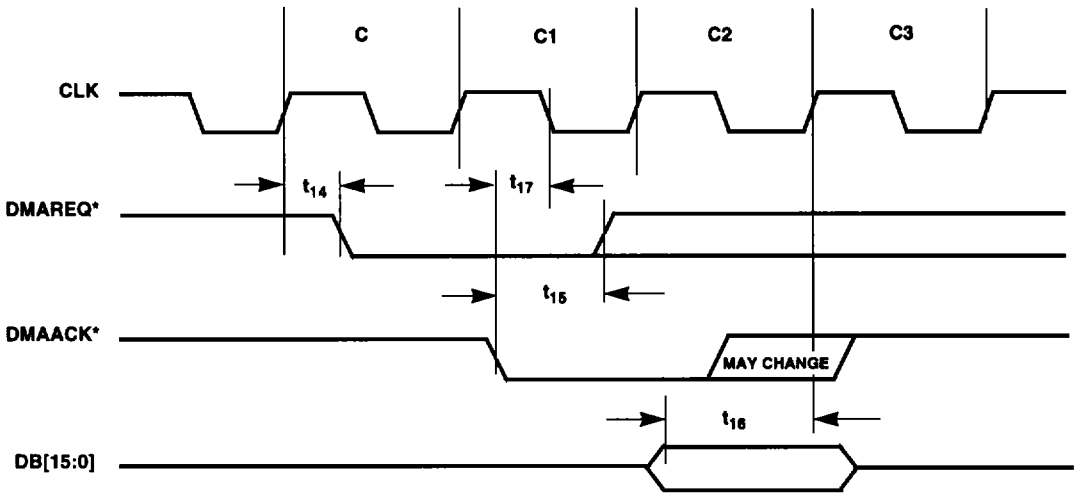


Figure 6-11. Synchronous DMA Write Cycle Timing

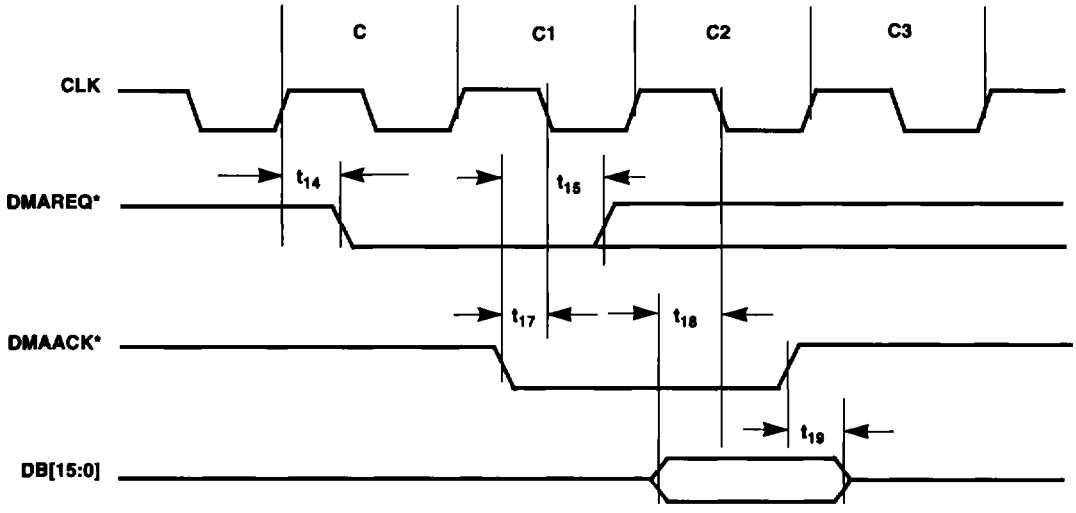


Figure 6-12. Synchronous DMA Read Cycle Timing