KM44S32030

8M x 4Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)

GENERAL DESCRIPTION

The KM44S32030 is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 4 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

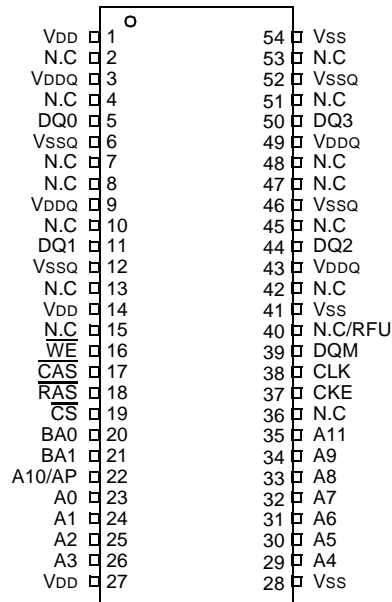| Part No.	Max Freq.	Interface	Package
KM44S32030T-G/F8	125MHz		
KM44S32030T-G/FH	100MHz	LVTTL	54pin TSOP(II)
KM44S32030T-G/FL	100MHz		
KM44S32030T-G/F10	100MHz		

FUNCTIONAL BLOCK DIAGRAM
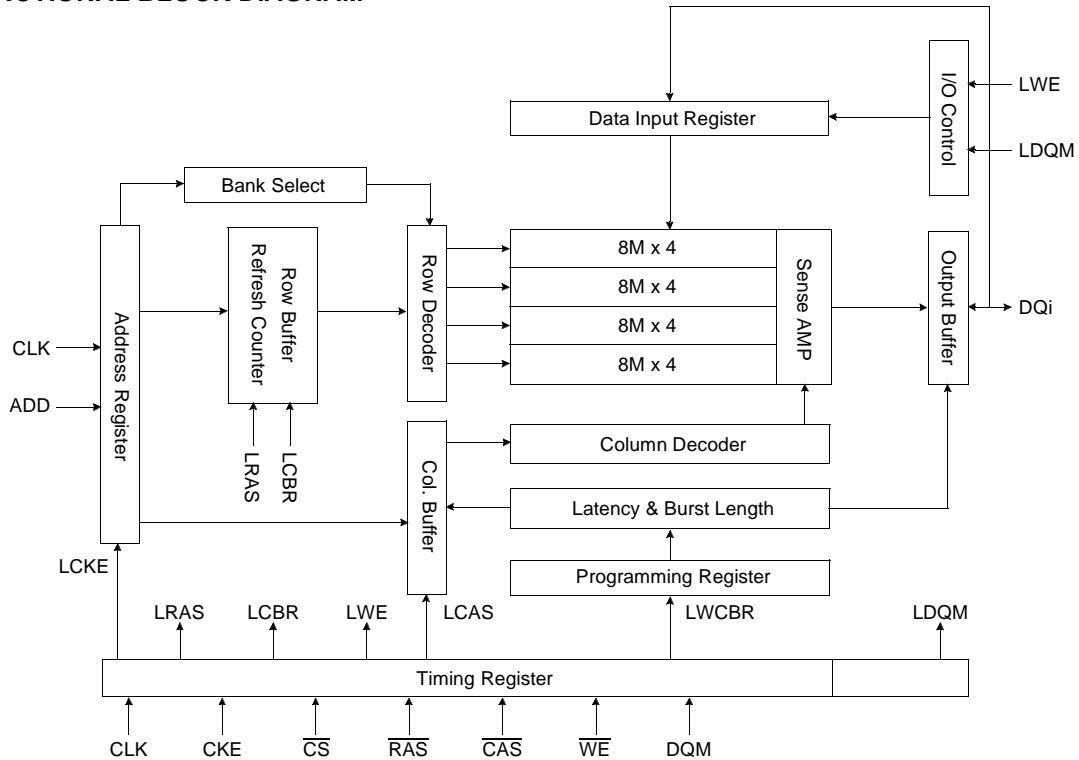
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PIN CONFIGURATION (Top view)

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                    ○
         VDD  ▯ 1        54 ▯ VSS
         N.C  ▯ 2        53 ▯ N.C
        VDDQ  ▯ 3        52 ▯ VSSQ
         N.C  ▯ 4        51 ▯ N.C
         DQ0  ▯ 5        50 ▯ DQ3
        VSSQ  ▯ 6        49 ▯ VDDQ
         N.C  ▯ 7        48 ▯ N.C
         N.C  ▯ 8        47 ▯ N.C
        VDDQ  ▯ 9        46 ▯ VSSQ
         N.C  ▯ 10       45 ▯ N.C
         DQ1  ▯ 11       44 ▯ DQ2
        VSSQ  ▯ 12       43 ▯ VDDQ
         N.C  ▯ 13       42 ▯ N.C
         VDD  ▯ 14       41 ▯ VSS
         N.C  ▯ 15       40 ▯ N.C/RFU
          WE  ▯ 16       39 ▯ DQM
         CAS  ▯ 17       38 ▯ CLK
         RAS  ▯ 18       37 ▯ CKE
          CS  ▯ 19       36 ▯ N.C
         BA0  ▯ 20       35 ▯ A11
         BA1  ▯ 21       34 ▯ A9
      A10/AP  ▯ 22       33 ▯ A8
          A0  ▯ 23       32 ▯ A7
          A1  ▯ 24       31 ▯ A6
          A2  ▯ 25       30 ▯ A5
          A3  ▯ 26       29 ▯ A4
         VDD  ▯ 27       28 ▯ VSS
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54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
$A_0 \sim A_{11}$	*Address*	Row/column addresses are multiplexed on the same pins. Row address : $RA_0 \sim RA_{11}$, Column address : $CA_0 \sim CA_9$, CA_{11}
$BA_0 \sim BA_1$	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_0 \sim 3$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

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REV. 2 Mar. '98

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	1	W
Short circuit current	IOS	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS
Recommended operating conditions (voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	VIH	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	VIL	-0.3	0	0.8	V	2
Output logic high voltage	VOH	2.4	-	-	V	IOH = -2mA
Output logic low voltage	VOL	-	-	0.4	V	IOL = 2mA
Input leakage current (Inputs)	IIL	-1	-	1	uA	3
Input leakage current (I/O pins)	IIL	-1.5	-	1.5	uA	3,4

Notes : 1. VIH (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. VIL (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ,
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ VOUT ≤ VDDQ.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Clock	CCLK	2.5	4	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	CIN	2.5	5	pF
Address	CADD	2.5	5	pF
DQ0 ~ DQ3	COUT	4	6.5	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

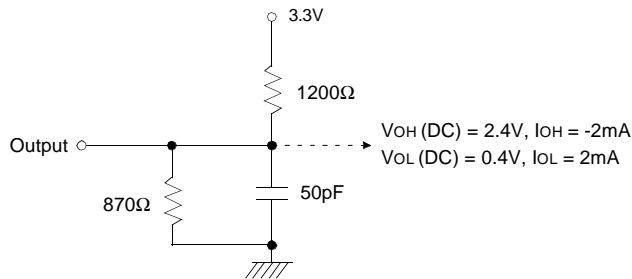| Parameter	Symbol	Test Condition	CAS Latency	Version -8	-H	-L	-10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		120	110	110	105	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE $\leq V_{IL}$(max), t_{CC} = 15ns		1				mA	
	I_{CC2PS}	CKE & CLK $\leq V_{IL}$(max), t_{CC} = ∞		1					
Precharge standby current in non power-down mode	I_{CC2N}	CKE $\geq V_{IH}$(min),$\overline{CS} \geq V_{IH}$(min),$t_{CC}$=15ns Input signals are changed one time during 30ns		15				mA	
	I_{CC2NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), t_{CC} = ∞ Input signals are stable		7					
Active standby current in power-down mode	I_{CC3P}	CKE $\leq V_{IL}$(max), t_{CC} = 15ns		5				mA	
	I_{CC3PS}	CKE & CLK $\leq V_{IL}$(max), t_{CC} = ∞		5					
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 15ns Input signals are changed one time during 30ns.		30				mA	
	I_{CC3NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), t_{CC} = ∞ Input signals are stable		20				mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst t_{CCD} = 2CLKs	3	140	115	115	115	mA	1
			2	105	115	105	105		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		200			165	mA	2
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V		1.5				mA	3
				800				uA	4

Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM44S32030T-G**
4. KM44S32030T-F**

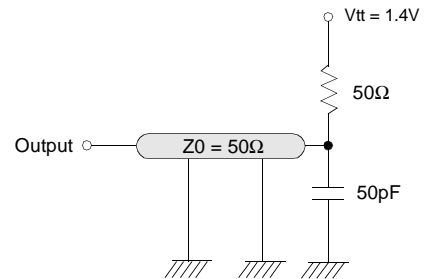## AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

 (V$_{DD}$ = 3.3V $\pm$ 0.3V, T$_A$ = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	

3.3V
1200Ω
Output
870Ω
50pF
V_{OH} (DC) = 2.4V, I_{OH} = -2mA
V_{OL} (DC) = 0.4V, I_{OL} = 2mA

(Fig. 1) DC output load circuit

Vtt = 1.4V
50Ω
Output
Z0 = 50Ω
50pF

(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-8	-H	-L	-10		
Row active to row active delay		t_{RRD}(min)	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	20	20	20	24	ns	1
Row precharge time		t_{RP}(min)	20	20	20	24	ns	1
Row active time		t_{RAS}(min)	48	50	50	50	ns	1
		t_{RAS}(max)	100				us	
Row cycle time		t_{RC}(min)	68	70	70	80	ns	1
Last data in to row precharge		t_{RDL}(min)	8	10	10	12	ns	2
Last data in to new col. address delay		t_{CDL}(min)	1				CLK	2
Last data in to burst stop		t_{BDL}(min)	1				CLK	2
Col. address to col. address delay		t_{CCD}(min)	1				CLK	3
Number of valid output data	CAS latency=3		2				ea	4
	CAS latency=2		1					

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

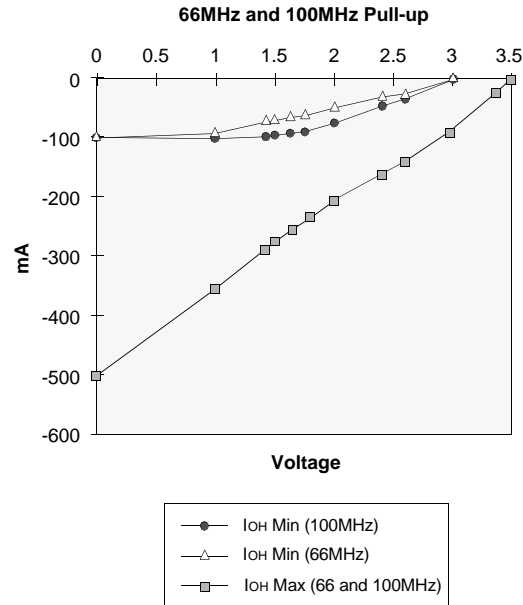**AC CHARACTERISTICS** (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-H		-L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6		7	ns	1,2
	CAS latency=2			6		6		7		7		
Output data hold time	CAS latency=3	tOH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
CLK high pulse width		tCH	3		3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3		3.5		ns	3
Input setup time		tSS	2		2		2		2.5		ns	3
Input hold time		tSH	1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6		7	ns	
	CAS latency=2			6		6		7		7		

Notes : 1. Parameters depend on programmed CAS latency.
       2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
       3. Assumed input rise and fall time (tr & tf) = 1ns.
          If tr & tf is longer than 1ns, transient time compensation should be considered,
          i.e., [(tr + tf)/2-1]ns should be added to the parameter.
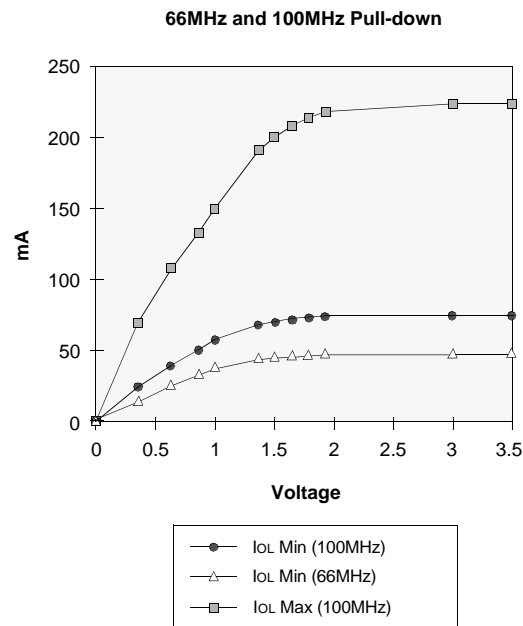
IBIS SPECIFICATION

I$_{OH}$ Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

66MHz and 100MHz Pull-up

- I$_{OH}$ Min (100MHz)
- I$_{OH}$ Min (66MHz)
- I$_{OH}$ Max (66 and 100MHz)

I$_{OL}$ Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

66MHz and 100MHz Pull-down

- I$_{OL}$ Min (100MHz)
- I$_{OL}$ Min (66MHz)
- I$_{OL}$ Max (100MHz)

V_DD Clamp @ CLK, CKE, CS, DQM & DQ

V_DD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

Minimum V_DD clamp current (Referenced to V_DD)
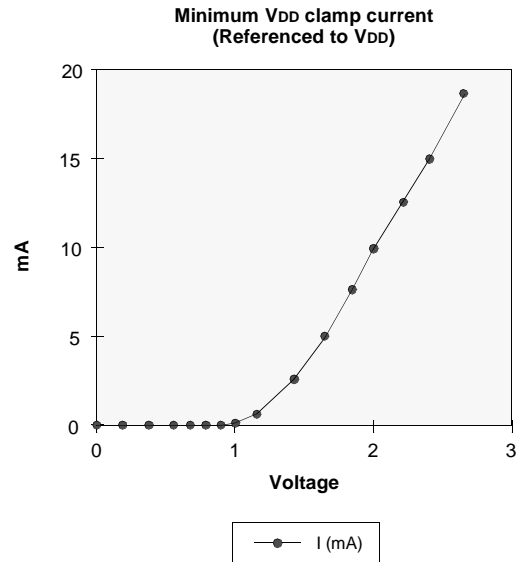
Vss Clamp @ CLK, CKE, CS, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum Vss clamp current

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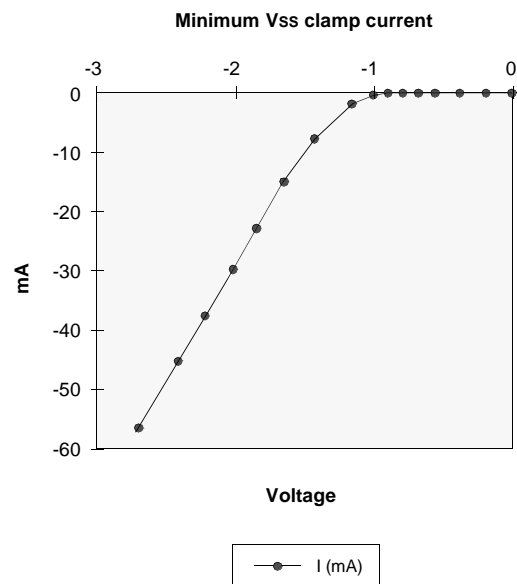
FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM44S32030T-8   (Unit : Number of clock)

Frequency	CAS Latency	t_{RC} 68ns	t_{RAS} 48ns	t_{RP} 20ns	t_{RRD} 16ns	t_{RCD} 20ns	t_{CCD} 8ns	t_{CDL} 8ns	t_{RDL} 8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM44S32030T-H   (Unit : Number of clock)

Frequency	CAS Latency	t_{RC} 70ns	t_{RAS} 50ns	t_{RP} 20ns	t_{RRD} 20ns	t_{RCD} 20ns	t_{CCD} 10ns	t_{CDL} 10ns	t_{RDL} 10ns
100MHz (10.0ns)	2	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM44S32030T-L   (Unit : Number of clock)

Frequency	CAS Latency	t_{RC} 70ns	t_{RAS} 50ns	t_{RP} 20ns	t_{RRD} 20ns	t_{RCD} 20ns	t_{CCD} 10ns	t_{CDL} 10ns	t_{RDL} 10ns
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM44S32030T-10   (Unit : Number of clock)

Frequency	CAS Latency	t_{RC} 80ns	t_{RAS} 50ns	t_{RP} 24ns	t_{RRD} 20ns	t_{RCD} 24ns	t_{CCD} 10ns	t_{CDL} 10ns	t_{RDL} 12ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	2
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	7	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge power down mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X	X			
					L	V	V	V					
DQM			H		X				V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :
1. OP Code : Operand code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

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