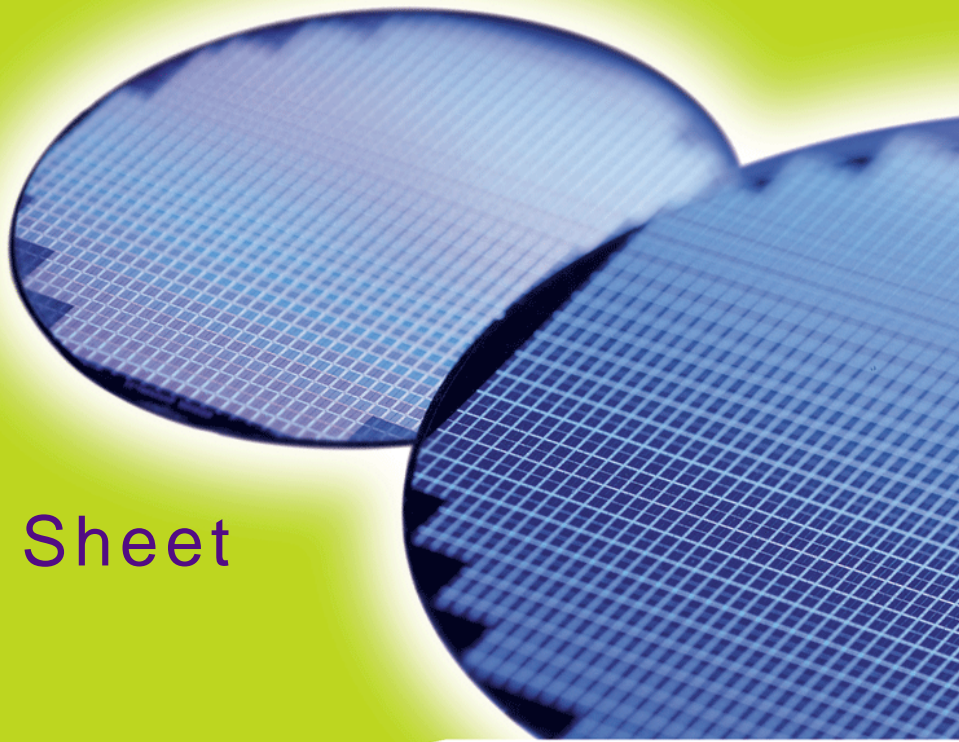


HYS64D[32/64]0x0EDL-5-D HYS64D[32/64]0x0EDL-6-D

*200-Pin Small-Outline Dual-In-Line Memory Modules
SO-DIMM
DDR SDRAM*



Internet Data Sheet

Rev. 1.00



| | |
|---|---|
| HYS64D[32/64]0x0EDL-5-D, HYS64D[32/64]0x0EDL-6-D | |
| Revision History: 2009-01, Rev. 1.00 | |
| Page | Subjects (major changes since last revision) |
| All | Metadata change and document adapted to internet edition. |
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| All | New Document. |

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1 Overview

This chapter contains features and the description.

1.1 Features

- Non-parity 200-Pin Small-Outline Dual-In-Line Memory Modules
- One rank 32M × 64, two ranks 64M × 64 module organization and 32M × 64 chip organization
- Industry standard Double-Data-Rate Synchronous DRAMs (DDR SDRAM)
- Single +2.5 V (± 0.2 V) power supply and +2.6 V (± 0.1 V) for DDR400
- Built with 512-Mbit DDR SDRAMs organised as ×16 in packages P-TSOPII-66
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E²PROM
- Industry standard form factor: 67.60 mm × 31.75 mm × 3.80 mm
- Industry standard reference layout Raw Cards 'A'
- DDR400 speed grade supported
- Gold plated contacts

TABLE 1
Performance for -5 and -6

| Part Number Speed Code | | -5 | -6 | Unit | |
|------------------------|-----------|-------------|-------------|------|-----|
| Speed Grade | Component | DDR400B | DDR333B | — | |
| | Module | PC3200-3033 | PC2700-2533 | | |
| max. Clock Frequency | @CL3 | f_{CK3} | 200 | 166 | MHz |
| | @CL2.5 | $f_{CK2.5}$ | 166 | 166 | MHz |
| | @CL2 | f_{CK2} | 133 | 133 | MHz |

1.2 Description

The HYS64D[32/64]0x0EDL-5-D and HYS64D[32/64]0x0EDL-6-D are industry standard 200-Pin Small-Outline Dual-In-Line Memory Modules (SO-DIMMs) organized as 32M × 64 and 64M × 64. The memory array is designed with Double-Data-Rate Synchronous DRAMs (DDR SDRAM). A variety of decoupling capacitors are mounted on the PCB. The DIMMs feature serial presence detect based on

a serial E²PROM device using the 2-pin I²C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.





HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

TABLE 2
Ordering Information for Lead-Free (RoHS Compliant Products)

| Product Type | Compliance Code | Description | SDRAM Technology | Note ¹⁾ |
|------------------------|-------------------|-------------------------|------------------|--------------------|
| PC3200 (CL=3.0) | | | | |
| HYS64D32000EDL-5-D | PC3200S-3033-1-C1 | one rank 256MB SO-DIMM | 512 MBit (×16) | |
| HYS64D64020EDL-5-D | PC3200S-3033-1-A1 | two ranks 512MB SO-DIMM | 512 MBit (×16) | |
| PC2700 (CL=2.5) | | | | |
| HYS64D32000EDL-6-D | PC2700S-2533-1-C1 | one rank 256MB SO-DIMM | 512 MBit (×16) | |
| HYS64D64020EDL-6-D | PC2700S-2533-1-A1 | two ranks 512MB SO-DIMM | 512 MBit (×16) | |

1) RoHS: Restriction of the use of certain hazardous substances in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Note: All product types end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS64D64020EDL-5-D, indicating Rev.B die are used for SDRAM components. The Compliance Code is printed on the module labels and describes the speed sort (for example “PC3200”), the latencies (for example “30330” means CAS latency of 3.0 clocks, Row-Column-Delay (RCD) latency of 3 clocks and Row Precharge latency of 3 clocks), JEDEC SPD code definition version 1, and the Raw Card used for this module.

TABLE 3
Address Format

| Density | Organization | Memory Ranks | SDRAMs | # of SDRAMs | # of row/bank/ columns bits | Refresh | Period | Interval |
|---------|--------------|--------------|---------|-------------|-----------------------------|---------|--------|----------|
| 512MB | 64M ×64 | 2 | 32M ×16 | 8 | 13/2/10 | 8K | 64 ms | 7.8 μs |
| 256MB | 32M ×64 | 1 | 32M ×16 | 4 | 13/2/10 | 8K | 64 ms | 7.8 μs |



2 Pin Configuration

2.1 Pin Configuration

The pin configuration of the Unbuffered Small Outline DDR SDRAM DIMM is listed by function in **Table 4** (200 pins). The abbreviations used in columns Pin and Buffer Type are

explained in **Table 5** and **Table 6** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 4
Pin Configuration of SO-DIMM

| Pin# | Name | Pin Type | Buffer Type | Function |
|------------------------|-------------------------|----------|-------------|--|
| Clock Signals | | | | |
| 35 | CK0 | I | SSTL | Clock Signal |
| 160 | CK1 | I | SSTL | Clock Signal |
| 89 | CK2 | I | SSTL | Clock Signal <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: non-ECC type module</i> |
| 37 | $\overline{\text{CK0}}$ | I | SSTL | Complement Clock |
| 158 | $\overline{\text{CK1}}$ | I | SSTL | Complement Clock |
| 91 | $\overline{\text{CK2}}$ | I | SSTL | Complement Clock <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: non-ECC type module</i> |
| 96 | CKE0 | I | SSTL | Clock Enable Rank 0 |
| 95 | CKE1 | I | SSTL | Clock Enable Rank 1 <i>Note: 2-rank module</i> |
| | NC | NC | – | <i>Note: 1-rank module</i> |
| Control Signals | | | | |
| 121 | $\overline{\text{S0}}$ | I | SSTL | Chip Select Rank 0 |
| 122 | $\overline{\text{S1}}$ | I | SSTL | Chip Select Rank 1 <i>Note: 2-ranks module</i> |
| | NC | NC | – | <i>Note: 1-rank module</i> |
| 118 | $\overline{\text{RAS}}$ | I | SSTL | Row Address Strobe |
| 120 | $\overline{\text{CAS}}$ | I | SSTL | Column Address Strobe |
| 119 | $\overline{\text{WE}}$ | I | SSTL | Write Enable |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

| Pin# | Name | Pin Type | Buffer Type | Function |
|------------------------|------|----------|-------------|--|
| Address Signals | | | | |
| 117 | BA0 | I | SSTL | Bank Address Bus 1:0 |
| 116 | BA1 | I | SSTL | |
| 112 | A0 | I | SSTL | Address Bus 11:0 |
| 111 | A1 | I | SSTL | |
| 110 | A2 | I | SSTL | |
| 109 | A3 | I | SSTL | |
| 108 | A4 | I | SSTL | |
| 107 | A5 | I | SSTL | |
| 106 | A6 | I | SSTL | |
| 105 | A7 | I | SSTL | |
| 102 | A8 | I | SSTL | |
| 101 | A9 | I | SSTL | |
| 115 | A10 | I | SSTL | |
| | AP | I | SSTL | |
| 100 | A11 | I | SSTL | |
| 99 | A12 | I | SSTL | Address Signal 12 <i>Note: Module based on 256 Mbit or larger dies</i> |
| | NC | NC | - | <i>Note: 128 Mbit based module</i> |
| 123 | A13 | I | SSTL | Address Signal 13 <i>Note: 1 Gbit based module</i> |
| | NC | NC | - | <i>Note: Module based on 512 Mbit or smaller dies</i> |
| Data Signals | | | | |
| 5 | DQ0 | I/O | SSTL | Data Bus 63:0 |
| 7 | DQ1 | I/O | SSTL | |
| 13 | DQ2 | I/O | SSTL | |
| 17 | DQ3 | I/O | SSTL | |
| 6 | DQ4 | I/O | SSTL | |
| 8 | DQ5 | I/O | SSTL | |
| 14 | DQ6 | I/O | SSTL | |
| 18 | DQ7 | I/O | SSTL | |
| 19 | DQ8 | I/O | SSTL | |
| 23 | DQ9 | I/O | SSTL | |
| 29 | DQ10 | I/O | SSTL | |
| 31 | DQ11 | I/O | SSTL | |
| 20 | DQ12 | I/O | SSTL | |
| 24 | DQ13 | I/O | SSTL | |

HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

| Pin# | Name | Pin Type | Buffer Type | Function |
|------|------|----------|-------------|---------------|
| 30 | DQ14 | I/O | SSTL | Data Bus 63:0 |
| 32 | DQ15 | I/O | SSTL | |
| 41 | DQ16 | I/O | SSTL | |
| 43 | DQ17 | I/O | SSTL | |
| 49 | DQ18 | I/O | SSTL | |
| 53 | DQ19 | I/O | SSTL | |
| 42 | DQ20 | I/O | SSTL | |
| 44 | DQ21 | I/O | SSTL | |
| 50 | DQ22 | I/O | SSTL | |
| 54 | DQ23 | I/O | SSTL | |
| 55 | DQ24 | I/O | SSTL | |
| 59 | DQ25 | I/O | SSTL | |
| 65 | DQ26 | I/O | SSTL | |
| 67 | DQ27 | I/O | SSTL | |
| 56 | DQ28 | I/O | SSTL | |
| 60 | DQ29 | I/O | SSTL | |
| 66 | DQ30 | I/O | SSTL | |
| 68 | DQ31 | I/O | SSTL | |
| 127 | DQ32 | I/O | SSTL | |
| 129 | DQ33 | I/O | SSTL | |
| 135 | DQ34 | I/O | SSTL | |
| 139 | DQ35 | I/O | SSTL | |
| 128 | DQ36 | I/O | SSTL | |
| 130 | DQ37 | I/O | SSTL | |
| 136 | DQ38 | I/O | SSTL | |
| 140 | DQ39 | I/O | SSTL | |
| 141 | DQ40 | I/O | SSTL | |
| 145 | DQ41 | I/O | SSTL | |
| 151 | DQ42 | I/O | SSTL | |
| 153 | DQ43 | I/O | SSTL | |
| 142 | DQ44 | I/O | SSTL | |
| 146 | DQ45 | I/O | SSTL | |
| 152 | DQ46 | I/O | SSTL | |
| 154 | DQ47 | I/O | SSTL | |
| 163 | DQ48 | I/O | SSTL | |
| 165 | DQ49 | I/O | SSTL | |
| 171 | DQ50 | I/O | SSTL | |
| 175 | DQ51 | I/O | SSTL | |
| 164 | DQ52 | I/O | SSTL | |
| 166 | DQ53 | I/O | SSTL | |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

| Pin# | Name | Pin Type | Buffer Type | Function |
|------|------|----------|-------------|--|
| 172 | DQ54 | I/O | SSTL | Data Bus 63:0 |
| 176 | DQ55 | I/O | SSTL | |
| 177 | DQ56 | I/O | SSTL | |
| 181 | DQ57 | I/O | SSTL | |
| 187 | DQ58 | I/O | SSTL | |
| 189 | DQ59 | I/O | SSTL | |
| 178 | DQ60 | I/O | SSTL | |
| 182 | DQ61 | I/O | SSTL | |
| 188 | DQ62 | I/O | SSTL | |
| 190 | DQ63 | I/O | SSTL | |
| 71 | CB0 | I/O | SSTL | Check Bit 0 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| 73 | CB1 | I/O | SSTL | Check Bit 1 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| 79 | CB2 | I/O | SSTL | Check Bit 2 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| 83 | CB3 | I/O | SSTL | Check Bit 3 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| 72 | CB4 | I/O | SSTL | Check Bit 4 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| 74 | CB5 | I/O | SSTL | Check Bit 5 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| 80 | CB6 | I/O | SSTL | Check Bit 6 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| 84 | CB7 | I/O | SSTL | Check Bit 7 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

| Pin# | Name | Pin Type | Buffer Type | Function |
|---------------|------|----------|-------------|--|
| 11 | DQS0 | I/O | SSTL | Data Strobes 7:0 <i>Note: See block diagram for corresponding DQ signals</i> |
| 25 | DQS1 | I/O | SSTL | |
| 47 | DQS2 | I/O | SSTL | |
| 61 | DQS3 | I/O | SSTL | |
| 133 | DQS4 | I/O | SSTL | |
| 147 | DQS5 | I/O | SSTL | |
| 169 | DQS6 | I/O | SSTL | |
| 183 | DQS7 | I/O | SSTL | |
| 77 | DQS8 | I/O | SSTL | Data Strobe 8 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| 12 | DM0 | I | SSTL | Data Mask 7:0 |
| 26 | DM1 | I | SSTL | |
| 48 | DM2 | I | SSTL | |
| 62 | DM3 | I | SSTL | |
| 134 | DM4 | I | SSTL | |
| 148 | DM5 | I | SSTL | |
| 170 | DM6 | I | SSTL | |
| 184 | DM7 | I | SSTL | |
| 78 | DM8 | I | SSTL | Data Mask 8 <i>Note: ECC type module</i> |
| | NC | NC | – | <i>Note: Non-ECC module</i> |
| EEPROM | | | | |
| 195 | SCL | I | CMOS | Serial Bus Clock |
| 193 | SDA | I/O | OD | Serial Bus Data |
| 194 | SA0 | I | CMOS | Slave Address Select Bus 2:0 |
| 196 | SA1 | I | CMOS | |
| 198 | SA2 | I | CMOS | |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

| Pin# | Name | Pin Type | Buffer Type | Function |
|--|-------------|----------|-------------|------------------------------|
| Power Supplies | | | | |
| 1,2 | V_{REF} | AI | – | I/O Reference Voltage |
| 197 | V_{DDSPD} | PWR | – | EEPROM Power Supply |
| 9,10,21, 22, 33, 34, 36, 45, 46, 57, 58, 69, 70, 81, 82, 92, 93, 94, 113, 114, 131, 132, 143, 144, 155, 156, 157, 167, 168, 179, 180, 191, 192 | V_{DD} | PWR | – | Power Supply |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|-------------------|----------|-------------|---|
| 3,4, 15, 16, 27, 28, 38, 39, 40, 51, 52, 63, 64, 75, 76, 87, 88, 90, 103, 104, 125, 126, 137, 138, 149, 150, 159, 161, 162, 173, 174, 185, 186 | V _{SS} | GND | – | Ground Plane |
| Other Pins | | | | |
| 199 | V _{DDID} | O | OD | V _{DD} Identification <i>Note: Pin in tristate, indicating V_{DD} and V_{DDQ} nets connected on PCB</i> |
| 85, 86, 97, 98, 124, 200 | NC | NC | – | Not connected <i>Note: Pins not connected on Infineon SO DIMMs</i> |

HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules**TABLE 5**
Abbreviations for Pin Type

| Abbreviation | Description |
|--------------|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NC | Not Connected |

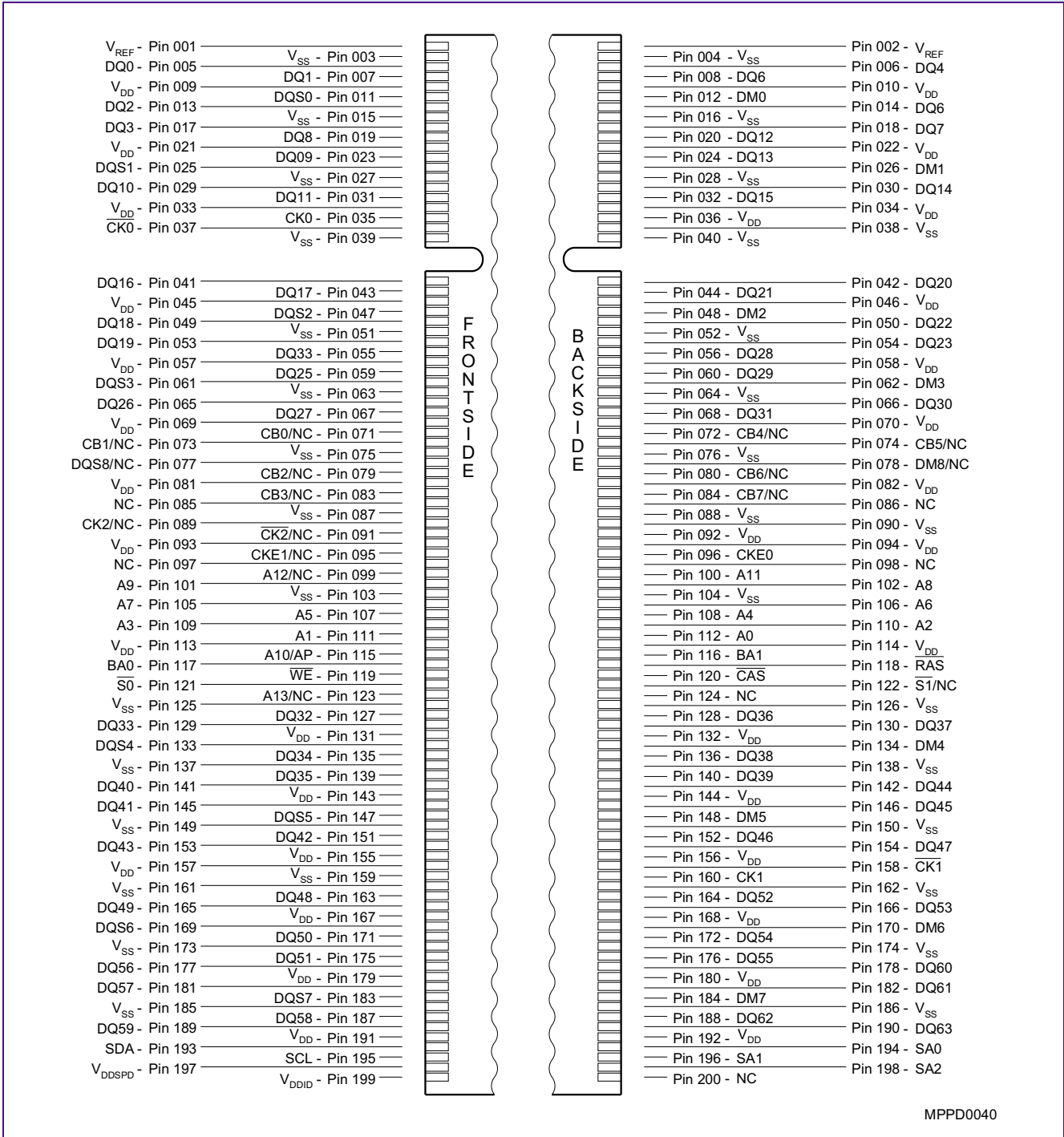
TABLE 6
Abbreviations for Buffer Type

| Abbreviation | Description |
|--------------|---|
| SSTL | Serial Stub Terminated Logic (SSTL2) |
| LV-CMOS | Low Voltage CMOS |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

FIGURE 1
Pin Configuration Diagram 200-Pin SO-DIMM



MPPD0040



3 Electrical Characteristics

This chapter lists the electrical characteristics.

3.1 Operating Conditions

This chapter contains the operating conditions tables.

TABLE 7
Absolute Maximum Ratings

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--|-------------------|--------|------|-----------------|------|----------------------|
| | | min. | typ. | max. | | |
| Voltage on I/O pins relative to V_{SS} | V_{IN}, V_{OUT} | -0.5 | — | $V_{DDQ} + 0.5$ | V | — |
| Voltage on inputs relative to V_{SS} | V_{IN} | -1 | — | +3.6 | V | — |
| Voltage on V_{DD} supply relative to V_{SS} | V_{DD} | -1 | — | +3.6 | V | — |
| Voltage on V_{DDQ} supply relative to V_{SS} | V_{DDQ} | -1 | — | +3.6 | V | — |
| Operating temperature (ambient) | T_A | 0 | — | +70 | °C | — |
| Storage temperature (plastic) | T_{STG} | -55 | — | +150 | °C | — |
| Power dissipation (per SDRAM component) | P_D | — | 1 | — | W | — |
| Short circuit output current | I_{OUT} | — | 50 | — | mA | — |

Attention: Permanent damage to the device may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

TABLE 8
Electrical Characteristics and DC Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note/Test Condition ¹⁾ |
|------------------------------------|-------------------|-----------------------|----------------------|-----------------------|------|-------------------------------------|
| | | Min. | Typ. | Max. | | |
| Device Supply Voltage | V_{DD} | 2.3 | 2.5 | 2.7 | V | $f_{CK} \leq 166$ MHz |
| Device Supply Voltage | V_{DD} | 2.5 | 2.6 | 2.7 | V | $f_{CK} > 166$ MHz ²⁾ |
| Output Supply Voltage | V_{DDQ} | 2.3 | 2.5 | 2.7 | V | $f_{CK} \leq 166$ MHz ³⁾ |
| Output Supply Voltage | V_{DDQ} | 2.5 | 2.6 | 2.7 | V | $f_{CK} > 166$ MHz ²⁾³⁾ |
| EEPROM supply voltage | V_{DDSPD} | 2.3 | 2.5 | 3.6 | V | — |
| Supply Voltage, I/O Supply Voltage | V_{SS}, V_{SSQ} | 0 | | 0 | V | — |
| Input Reference Voltage | V_{REF} | $0.49 \times V_{DDQ}$ | $0.5 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V | ⁴⁾ |
| I/O Termination Voltage (System) | V_{TT} | $V_{REF} - 0.04$ | | $V_{REF} + 0.04$ | V | ⁵⁾ |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

| Parameter | Symbol | Values | | | Unit | Note/Test Condition ¹⁾ |
|---|-----------------|------------------|------|------------------|---------|---|
| | | Min. | Typ. | Max. | | |
| Input High (Logic1) Voltage | $V_{IH(DC)}$ | $V_{REF} + 0.15$ | | $V_{DDQ} + 0.3$ | V | 6) |
| Input Low (Logic0) Voltage | $V_{IL(DC)}$ | -0.3 | | $V_{REF} - 0.15$ | V | 6) |
| Input Voltage Level, CK and \overline{CK} Inputs | $V_{IN(DC)}$ | -0.3 | | $V_{DDQ} + 0.3$ | V | 6) |
| Input Differential Voltage, CK and \overline{CK} Inputs | $V_{ID(DC)}$ | 0.36 | | $V_{DDQ} + 0.6$ | V | 6)7) |
| VI-Matching Pull-up Current to Pull-down Current | $V_{I_{Ratio}}$ | 0.71 | | 1.4 | — | 8) |
| Input Leakage Current | I_I | -2 | | 2 | μA | Any input $0 V \leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V ⁹⁾ |
| Output Leakage Current | I_{OZ} | -5 | | 5 | μA | DQs are disabled; $0 V \leq V_{OUT} \leq V_{DDQ}$ ⁹⁾ |
| Output High Current, Normal Strength Driver | I_{OH} | -16.2 | | — | mA | $V_{OUT} = 1.95 V$ |
| Output Low Current, Normal Strength Driver | I_{OL} | 16.2 | | — | mA | $V_{OUT} = 0.35 V$ |

- 1) $0^\circ C \leq T_A \leq 70^\circ C$; $V_{DDQ} = 2.5 V \pm 0.2 V$, $V_{DD} = +2.5 V \pm 0.2 V$;
- 2) DDR400 conditions apply for all clock frequencies above 166 MHz
- 3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD} .
- 4) Peak to peak AC noise on V_{REF} may not exceed $\pm 2\% V_{REF(DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ} .
- 5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .
- 6) Inputs are not recognized as valid until V_{REF} stabilizes.
- 7) V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .
- 8) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- 9) Values are shown per pin.



3.2 Current Specification and Conditions

This chapter describes the Specifications and Conditions.

TABLE 9
 I_{DD} Conditions

| Parameter | Symbol |
|---|------------|
| Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles. | I_{DD0} |
| Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet. | I_{DD1} |
| Precharge Power-Down Standby Current all banks idle; power-down mode; $CKE \leq V_{IL,MAX}$ | I_{DD2P} |
| Precharge Floating Standby Current $\overline{CS} \geq V_{IH,MIN}$, all banks idle; $CKE \geq V_{IH,MIN}$; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM. | I_{DD2F} |
| Precharge Quiet Standby Current $\overline{CS} \geq V_{IH,MIN}$, all banks idle; $CKE \geq V_{IH,MIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM; address and other control inputs stable at $\geq V_{IH,MIN}$ or $\leq V_{IL,MAX}$. | I_{DD2Q} |
| Active Power-Down Standby Current one bank active; power-down mode; $CKE \leq V_{IL,MAX}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM. | I_{DD3P} |
| Active Standby Current one bank active; $\overline{CS} \geq V_{IH,MIN}$; $CKE \geq V_{IH,MIN}$; $t_{RC} = t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle. | I_{DD3N} |
| Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; $I_{OUT} = 0$ mA | I_{DD4R} |
| Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B | I_{DD4W} |
| Auto-Refresh Current $t_{RC} = t_{RFCMIN}$, burst refresh | I_{DD5} |
| Self-Refresh Current $CKE \leq 0.2$ V; external clock on | I_{DD6} |
| Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet. | I_{DD7} |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

TABLE 10
 I_{DD} Specification for HYS64D64020EDL-[5/6]-D

| Product Type | HYS64D64020EDL-5-D | | HYS64D64020EDL-6-D | | Unit | Note ¹⁾²⁾ |
|--------------|--------------------|---------|--------------------|---------|------|----------------------|
| | 512MB | 512MB | 512MB | 512MB | | |
| | ×64 | ×64 | ×64 | ×64 | | |
| | 2 Ranks | 2 Ranks | 2 Ranks | 2 Ranks | | |
| | -5 | -5 | -6 | -6 | | |
| Symbol | Typ. | Max. | Typ. | Max. | | |
| I_{DD0} | 228 | 294 | 196 | 258 | mA | 3) |
| I_{DD1} | 260 | 330 | 224 | 290 | mA | 3)4) |
| I_{DD2P} | 8 | 37 | 8 | 37 | mA | 5) |
| I_{DD2F} | 176 | 240 | 160 | 216 | mA | 5) |
| I_{DD2Q} | 120 | 176 | 112 | 160 | mA | 5) |
| I_{DD3P} | 64 | 112 | 64 | 112 | mA | 5) |
| I_{DD3N} | 232 | 296 | 208 | 272 | mA | 5) |
| I_{DD4R} | 296 | 370 | 256 | 326 | mA | 3)4) |
| I_{DD4W} | 284 | 358 | 248 | 314 | mA | 3) |
| I_{DD5} | 496 | 602 | 444 | 522 | mA | 5) |
| I_{DD6} | 12 | 32 | 12 | 32 | mA | 5) |
| I_{DD7} | 712 | 870 | 600 | 686 | mA | 3)4) |

- 1) Module I_{DD} values are calculated on the basis of component I_{DD} and can be measured differently according to DQ loading capacity.
- 2) Test condition for maximum values: $V_{DD} = 2.7\text{ V}$, $T_A = 10\text{ °C}$
- 3) The module I_{DDx} values are calculated from the I_{DDx} values of the component data sheet as follows:
 $m \times I_{DDx}[\text{component}] + n \times I_{DD2P}[\text{component}]$ with **m** and **n** number of components of rank 1 and 2; **n=0** for 1 rank modules
- 4) DQ I/O (I_{DDQ}) currents are not included in the calculations (see note¹⁾)
- 5) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: $(m + n) \times I_{DDx}[\text{component}]$



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

TABLE 11
 I_{DD} Specification for HYS64D32000EDL-[5/6]-D

| Product Type | HYS64D32000EDL-5-D | | HYS64D32000EDL-6-D | | Unit | Note ¹⁾²⁾ |
|--------------|--------------------|--------|--------------------|--------|------|----------------------|
| | 256MB | 256MB | 256MB | 256MB | | |
| | ×64 | ×64 | ×64 | ×64 | | |
| | 1 Rank | 1 Rank | 1 Rank | 1 Rank | | |
| | -5 | -5 | -6 | -6 | | |
| Symbol | Typ. | Max. | Typ. | Max. | | |
| I_{DD0} | 224 | 276 | 192 | 240 | mA | 3) |
| I_{DD1} | 256 | 312 | 220 | 272 | mA | 3)4) |
| I_{DD2P} | 4 | 18 | 4 | 18 | mA | 5) |
| I_{DD2F} | 88 | 120 | 80 | 108 | mA | 5) |
| I_{DD2Q} | 60 | 88 | 56 | 80 | mA | 5) |
| I_{DD3P} | 32 | 56 | 32 | 56 | mA | 5) |
| I_{DD3N} | 116 | 148 | 104 | 136 | mA | 5) |
| I_{DD4R} | 292 | 352 | 252 | 308 | mA | 3)4) |
| I_{DD4W} | 280 | 340 | 244 | 296 | mA | 3) |
| I_{DD5} | 492 | 584 | 440 | 504 | mA | 5) |
| I_{DD6} | 6 | 16 | 6 | 16 | mA | 5) |
| I_{DD7} | 708 | 852 | 596 | 668 | mA | 3)4) |

- 1) Module I_{DD} values are calculated on the basis of component I_{DD} and can be measured differently according to DQ loading capacity.
- 2) Test condition for maximum values: $V_{DD} = 2.7\text{ V}$, $T_A = 10\text{ °C}$
- 3) The module I_{DDx} values are calculated from the I_{DDx} values of the component data sheet as follows:
 $m \times I_{DDx}[\text{component}] + n \times I_{DD2P}[\text{component}]$ with **m** and **n** number of components of rank 1 and 2; **n=0** for 1 rank modules
- 4) DQ I/O (I_{DDQ}) currents are not included in the calculations (see note¹⁾)
- 5) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: $(m + n) \times I_{DDx}[\text{component}]$



3.3 AC Characteristics

This chapter describes the AC characteristics.

TABLE 12

AC Timing - Absolute Specifications for PC3200 and PC2700

| Parameter | Symbol | -5 | | -6 | | Unit | Note/ Test Condition ¹⁾ |
|--|--------------|-------------------------------------|-------|---------------------------|-------|----------|------------------------------------|
| | | DDR400B | | DDR333 | | | |
| | | Min. | Max. | Min. | Max. | | |
| DQ output access time from $\overline{\text{CK}}/\text{CK}$ | t_{AC} | -0.7 | +0.7 | -0.7 | +0.7 | ns | 2)3)4)5) |
| CK high-level width | t_{CH} | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | 2)3)4)5) |
| Clock cycle time | t_{CK} | 5 | 12 | 6 | 12 | ns | CL = 3.0 2)3)4)5) |
| | | 6 | 12 | 6 | 12 | ns | CL = 2.5 2)3)4)5) |
| | | 7 | 12 | 7.5 | 12 | ns | CL = 2.0 2)3)4)5) |
| CK low-level width | t_{CL} | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | 2)3)4)5) |
| Auto precharge write recovery + precharge time | t_{DAL} | $(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$ | | | | t_{CK} | 2)3)4)5)6) |
| DQ and DM input hold time | t_{DH} | 0.4 | — | 0.45 | — | ns | 2)3)4)5) |
| DQ and DM input pulse width (each input) | t_{DIPW} | 1.75 | — | 1.75 | — | ns | 2)3)4)5)6) |
| DQS output access time from $\overline{\text{CK}}/\text{CK}$ | t_{DQSCK} | -0.6 | +0.6 | -0.6 | +0.6 | ns | 2)3)4)5) |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | 0.35 | — | t_{CK} | 2)3)4)5) |
| DQS-DQ skew (DQS and associated DQ signals) | t_{DQSQ} | — | +0.40 | — | +0.45 | ns | TSOPII 2)3)4)5) |
| Write command to 1 st DQS latching transition | t_{DQSS} | 0.72 | 1.25 | 0.75 | 1.25 | t_{CK} | 2)3)4)5) |
| DQ and DM input setup time | t_{DS} | 0.4 | — | 0.45 | — | ns | 2)3)4)5) |
| DQS falling edge hold time from $\overline{\text{CK}}$ (write cycle) | t_{DSH} | 0.2 | — | 0.2 | — | t_{CK} | 2)3)4)5) |
| DQS falling edge to $\overline{\text{CK}}$ setup time (write cycle) | t_{DSS} | 0.2 | — | 0.2 | — | t_{CK} | 2)3)4)5) |
| Clock Half Period | t_{HP} | Min. (t_{CL}, t_{CH}) | | Min. (t_{CL}, t_{CH}) | | ns | 2)3)4)5) |
| Data-out high-impedance time from $\overline{\text{CK}}/\text{CK}$ | t_{HZ} | | +0.7 | -0.7 | +0.7 | ns | 2)3)4)5)7) |
| Address and control input hold time | t_{IH} | 0.6 | — | 0.75 | — | ns | Fast slew rate 3)4)5)6)10) |
| | | 0.7 | — | 0.8 | — | ns | Slow slew rate 3)4)5)6)10) |
| Control and Addr. input pulse width (each input) | t_{IPW} | 2.2 | — | 2.2 | — | ns | 2)3)4)5)8) |



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| Parameter | Symbol | -5 | | -6 | | Unit | Note/ Test Condition ¹⁾ |
|--|-------------|--------------------|-------|--------------------|-------|----------|------------------------------------|
| | | DDR400B | | DDR333 | | | |
| | | Min. | Max. | Min. | Max. | | |
| Address and control input setup time | t_{IS} | 0.6 | — | 0.75 | — | ns | Fast slew rate 3)4)5)6)9) |
| | | 0.7 | — | 0.8 | — | ns | Slow slew rate 3)4)5)6)10) |
| Data-out low-impedance time from CK/CK | t_{LZ} | -0.7 | +0.7 | -0.7 | +0.7 | ns | 2)3)4)5)7) |
| Mode register set command cycle time | t_{MRD} | 2 | — | 2 | — | t_{CK} | 2)3)4)5) |
| DQ/DQS output hold time | t_{QH} | $t_{HP} - t_{QHS}$ | — | $t_{HP} - t_{QHS}$ | — | ns | 2)3)4)5) |
| Data hold skew factor | t_{QHS} | — | +0.50 | — | +0.55 | ns | TSOPII 2)3)4)5) |
| Active to Autoprecharge delay | t_{RAP} | t_{RCD} | — | t_{RCD} | — | ns | 2)3)4)5) |
| Active to Precharge command | t_{RAS} | 40 | 70E+3 | 42 | 70E+3 | ns | 2)3)4)5) |
| Active to Active/Auto-refresh command period | t_{RC} | 55 | — | 60 | — | ns | 2)3)4)5) |
| Active to Read or Write delay | t_{RCD} | 15 | — | 18 | — | ns | 2)3)4)5) |
| Average Periodic Refresh Interval | t_{REFI} | — | 7.8 | — | 7.8 | μ s | 2)3)4)5)10) |
| Auto-refresh to Active/Auto-refresh command period | t_{RFC} | 70 | — | 72 | — | ns | 2)3)4)5) |
| Precharge command period | t_{RP} | 15 | — | 18 | — | ns | 2)3)4)5) |
| Read preamble | t_{RPRE} | 0.9 | 1.1 | 0.9 | 1.1 | t_{CK} | 2)3)4)5) |
| Read postamble | t_{RPST} | 0.40 | 0.60 | 0.40 | 0.60 | t_{CK} | 2)3)4)5) |
| Active bank A to Active bank B command | t_{RRD} | 10 | — | 12 | — | ns | 2)3)4)5) |
| Write preamble | t_{WPRE} | 0.25 | — | 0.25 | — | t_{CK} | 2)3)4)5) |
| Write preamble setup time | t_{WPRES} | 0 | — | 0 | — | ns | 2)3)4)5)11) |
| Write postamble | t_{WPST} | 0.40 | 0.60 | 0.40 | 0.60 | t_{CK} | 2)3)4)5)12) |
| Write recovery time | t_{WR} | 15 | — | 15 | — | ns | 2)3)4)5) |
| Internal write to read command delay | t_{WTR} | 2 | — | 1 | — | t_{CK} | 2)3)4)5) |
| Exit self-refresh to non-read command | t_{XSNR} | 75 | — | 75 | — | ns | 2)3)4)5) |
| Exit self-refresh to read command | t_{XSRD} | 200 | — | 200 | — | t_{CK} | 2)3)4)5) |

- 1) $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; $V_{DDQ} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{DD} = +2.5\text{ V} \pm 0.2\text{ V}$ (DDR333); $V_{DDQ} = 2.6\text{ V} \pm 0.1\text{ V}$, $V_{DD} = +2.6\text{ V} \pm 0.1\text{ V}$ (DDR400)
- 2) Input slew rate $\geq 1\text{ V/ns}$ for DDR400, DDR333
- 3) The CK/ $\overline{\text{CK}}$ input reference level (for timing reference to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross: the input reference level for signals other than CK/ $\overline{\text{CK}}$, is V_{REF} . CK/ $\overline{\text{CK}}$ slew rate are $\geq 1.0\text{ V/ns}$.
- 4) Inputs are not recognized as valid until V_{REF} stabilizes.
- 5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT} .
- 6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.
- 7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

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- 8) These parameters guarantee device timing, but they are not necessarily tested on each device.
- 9) Fast slew rate ≥ 1.0 V/ns, slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{\text{CK}}$ slew rate > 1.0 V/ns, measured between $V_{\text{OH(ac)}}$ and $V_{\text{OL(ac)}}$.
- 10) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
- 11) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS} .
- 12) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.



4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- [Table 13 “HYS64D\[32/64\]3x0EDL-\[5/6\]-D” on Page 22](#)

TABLE 13
HYS64D[32/64]3x0EDL-[5/6]-D

| Product Type | | HYS64D32000EDL-5-D | HYS64D32000EDL-6-D | HYS64D64020EDL-5-D | HYS64D64020EDL-6-D |
|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| Organization | | 256MB | 256MB | 512MB | 512MB |
| | | ×64 | ×64 | ×64 | ×64 |
| | | 1 Rank (×16) | 1 Rank (×16) | 2 Ranks (×16) | 2 Ranks (×16) |
| Label Code | | PC3200S-30331 | PC2700S-25331 | PC3200S-30331 | PC2700S-25331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 0 | Programmed SPD Bytes in E2PROM | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in E2PROM | 08 | 08 | 08 | 08 |
| 2 | Memory Type (DDR = 07h) | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 0A | 0A | 0A | 0A |
| 5 | Number of DIMM Ranks | 01 | 01 | 02 | 02 |
| 6 | Data Width (LSB) | 40 | 40 | 40 | 40 |
| 7 | Data Width (MSB) | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 | 04 | 04 |
| 9 | t _{CK} @ CL _{max} (Byte 18) [ns] | 50 | 60 | 50 | 60 |
| 10 | t _{AC} SDRAM @ CL _{max} (Byte 18) [ns] | 70 | 70 | 70 | 70 |
| 11 | Error Correction Support | 00 | 00 | 00 | 00 |
| 12 | Refresh Rate | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM Width | 10 | 10 | 10 | 10 |



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| Product Type | | HYS64D32000EDL-5-D | HYS64D32000EDL-6-D | HYS64D64020EDL-5-D | HYS64D64020EDL-6-D |
|--------------------|---|--------------------|--------------------|--------------------|--------------------|
| Organization | | 256MB | 256MB | 512MB | 512MB |
| | | ×64 | ×64 | ×64 | ×64 |
| | | 1 Rank (×16) | 1 Rank (×16) | 2 Ranks (×16) | 2 Ranks (×16) |
| Label Code | | PC3200S-30331 | PC2700S-25331 | PC3200S-30331 | PC2700S-25331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 14 | Error Checking SDRAM Width | 00 | 00 | 00 | 00 |
| 15 | t _{CCD} [cycles] | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E | 0E | 0E |
| 17 | Number of Banks on SDRAM Device | 04 | 04 | 04 | 04 |
| 18 | CAS Latency | 1C | 0C | 1C | 0C |
| 19 | CS Latency | 01 | 01 | 01 | 01 |
| 20 | Write Latency | 02 | 02 | 02 | 02 |
| 21 | DIMM Attributes | 20 | 20 | 20 | 20 |
| 22 | Component Attributes | C1 | C1 | C1 | C1 |
| 23 | t _{CK} @ CL _{max} -0.5 (Byte 18) [ns] | 60 | 75 | 60 | 75 |
| 24 | t _{AC} SDRAM @ CL _{max} -0.5 [ns] | 70 | 70 | 70 | 70 |
| 25 | t _{CK} @ CL _{max} -1 (Byte 18) [ns] | 75 | 00 | 75 | 00 |
| 26 | t _{AC} SDRAM @ CL _{max} -1 [ns] | 70 | 00 | 70 | 00 |
| 27 | t _{RPmin} [ns] | 3C | 48 | 3C | 48 |
| 28 | t _{RRDmin} [ns] | 28 | 30 | 28 | 30 |
| 29 | t _{RCDmin} [ns] | 3C | 48 | 3C | 48 |
| 30 | t _{RASmin} [ns] | 28 | 2A | 28 | 2A |
| 31 | Module Density per Rank | 40 | 40 | 40 | 40 |
| 32 | t _{AS} , t _{CS} [ns] | 60 | 75 | 60 | 75 |
| 33 | t _{AH} , t _{CH} [ns] | 60 | 75 | 60 | 75 |
| 34 | t _{DS} [ns] | 40 | 45 | 40 | 45 |
| 35 | t _{DH} [ns] | 40 | 45 | 40 | 45 |
| 36 - 40 | Not used | 00 | 00 | 00 | 00 |
| 41 | t _{RCmin} [ns] | 37 | 3C | 37 | 3C |
| 42 | t _{RFCmin} [ns] | 41 | 48 | 41 | 48 |



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

| Product Type | | HYS64D32000EDL-5-D | HYS64D32000EDL-6-D | HYS64D64020EDL-5-D | HYS64D64020EDL-6-D |
|--------------------|----------------------------------|--------------------|--------------------|--------------------|--------------------|
| Organization | | 256MB | 256MB | 512MB | 512MB |
| | | ×64 | ×64 | ×64 | ×64 |
| | | 1 Rank (×16) | 1 Rank (×16) | 2 Ranks (×16) | 2 Ranks (×16) |
| Label Code | | PC3200S-30331 | PC2700S-25331 | PC3200S-30331 | PC2700S-25331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 43 | t _{CKmax} [ns] | 28 | 30 | 28 | 30 |
| 44 | t _{BQSQmax} [ns] | 28 | 2D | 28 | 2D |
| 45 | t _{QHSmax} [ns] | 50 | 55 | 50 | 55 |
| 46 | not used | 00 | 00 | 00 | 00 |
| 47 | DIMM PCB Height | 01 | 01 | 01 | 01 |
| 48 - 61 | Not used | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | 10 | 10 | 10 | 10 |
| 63 | Checksum of Byte 0-62 | 76 | 1A | 77 | 1B |
| 64 | Manufacturer's JEDEC ID Code (1) | 7F | 7F | 7F | 7F |
| 65 | Manufacturer's JEDEC ID Code (2) | 7F | 7F | 7F | 7F |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx | xx | xx |
| 73 | Part Number, Char 1 | 36 | 36 | 36 | 36 |
| 74 | Part Number, Char 2 | 34 | 34 | 34 | 34 |
| 75 | Part Number, Char 3 | 44 | 44 | 44 | 44 |
| 76 | Part Number, Char 4 | 33 | 33 | 36 | 36 |
| 77 | Part Number, Char 5 | 32 | 32 | 34 | 34 |
| 78 | Part Number, Char 6 | 30 | 30 | 30 | 30 |
| 79 | Part Number, Char 7 | 30 | 30 | 32 | 32 |
| 80 | Part Number, Char 8 | 30 | 30 | 30 | 30 |



HYS64D[32/64]0x0EDL-[5/6]-D
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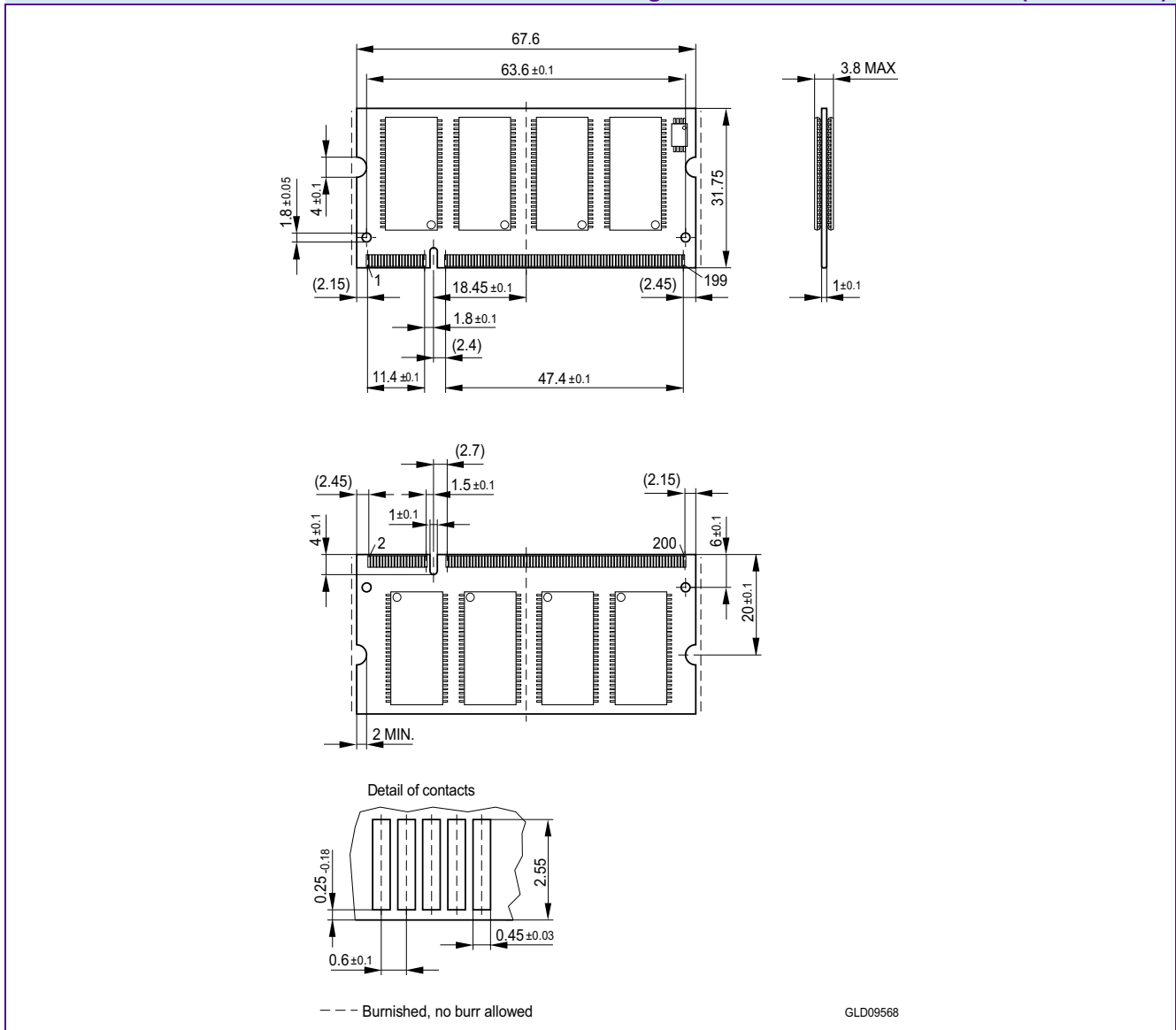
| Product Type | | HYS64D32000EDL-5-D | HYS64D32000EDL-6-D | HYS64D64020EDL-5-D | HYS64D64020EDL-6-D |
|--------------------|--------------------------------|------------------------------|------------------------------|-------------------------------|-------------------------------|
| Organization | | 256MB ×64 1 Rank (×16) | 256MB ×64 1 Rank (×16) | 512MB ×64 2 Ranks (×16) | 512MB ×64 2 Ranks (×16) |
| Label Code | | PC3200S-30331 | PC2700S-25331 | PC3200S-30331 | PC2700S-25331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 81 | Part Number, Char 9 | 45 | 45 | 45 | 45 |
| 82 | Part Number, Char 10 | 44 | 44 | 44 | 44 |
| 83 | Part Number, Char 11 | 4C | 4C | 4C | 4C |
| 84 | Part Number, Char 12 | 35 | 36 | 35 | 36 |
| 85 | Part Number, Char 13 | 44 | 44 | 44 | 44 |
| 86 | Part Number, Char 14 | 20 | 20 | 20 | 20 |
| 87 | Part Number, Char 15 | 20 | 20 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 | 20 | 20 |
| 89 | Part Number, Char 17 | 20 | 20 | 20 | 20 |
| 90 | Part Number, Char 18 | 20 | 20 | 20 | 20 |
| 91 | Module Revision Code | 0x | 0x | 0x | 0x |
| 92 | Test Program Revision Code | xx | xx | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx | xx | xx |
| 99 - 127 | Not used | 00 | 00 | 00 | 00 |



5 Package Outlines

This chapter contains the package outlines of the products.

FIGURE 2
Package Outline SO-DIMM Raw Card A (L-DIM-200-6)



Notes

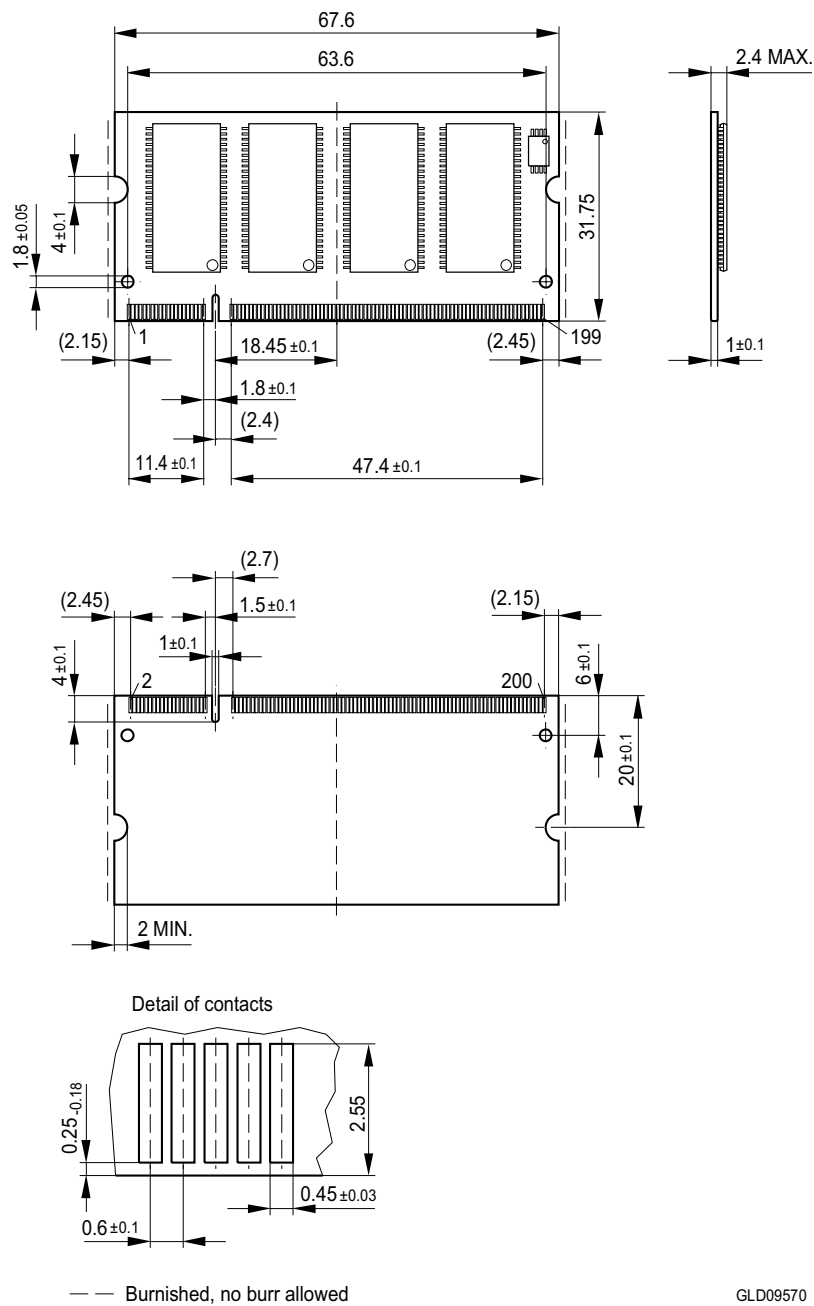
1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15



HYS64D[32/64]0x0EDL-[5/6]-D
Small-Outline DDR SDRAM Modules

FIGURE 3

Package Outline SO-DIMM Raw Card C (L-DIM-200-11)



GLD09570

Notes

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15



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